

Design Guidelines for Quasi-Resonant Flyback Converters Using HFC0100

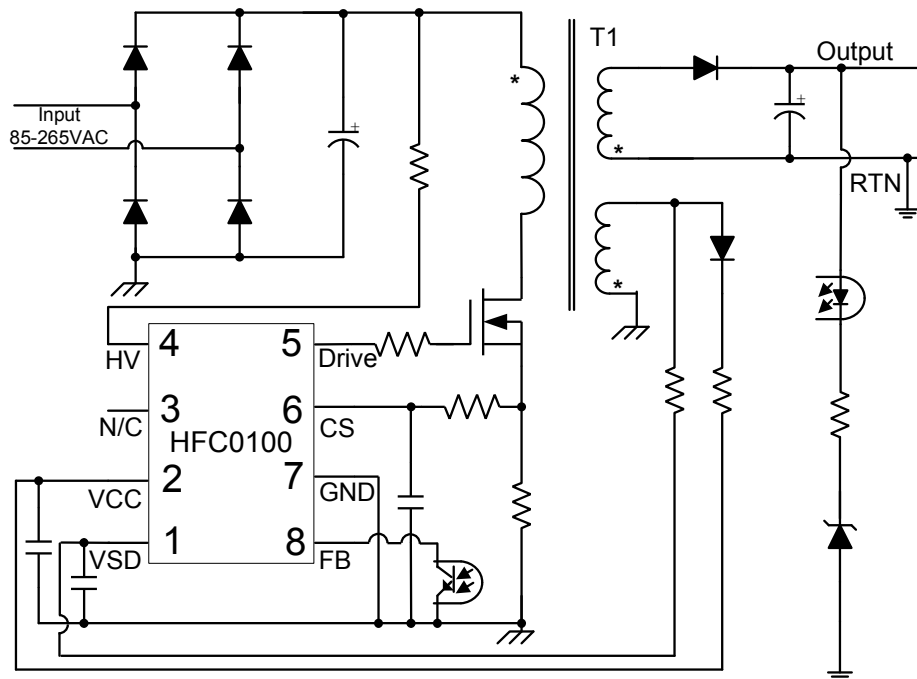
Application Note

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ABSTRACT

This paper presents design guidelines for quasi-resonant flyback converters with current mode controller-HFC0100 of MPS. Design of a quasi-resonant flyback converter with HFC0100 is made easier through use of this step-by-step design procedure from this paper. Experimental results based on the design example are presented in the last part.



Basic Quasi—Resonant Flyback Converter Using HFC0100

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1. HFC0100 INTRODUCTION

HFC0100 is a peak current mode controller that integrated with a high voltage current source; its internal valley detector ensures minimum Drain-Source voltage switching (Quasi-Resonant operation). When the output power falls below a given level, the controller enters the burst mode for lower power loss at no/light load condition. HFC0100 can be adopted in off-line, telecom and non-isolated applications. Internal Vcc Undervoltage Lockout (UVLO), Over Load Protection (OLP), Over Voltage Protection (OVP) are all provided to minimize the external component count. This paper presents practical design guidelines for a quasi-resonant flyback converter employing HFC0100. Step-by-step design procedure for quasi-resonant flyback converter using HFC0100 can be applied to various offline applications, mainly including transformer design, output filter design and component selection.

2. QUASI-RESONANT OPERATION INTRODUCTION

Quasi-resonant conversion works in quite a different way than the well-known resonant converter to cut losses. Figure 1 shows the drain-source voltage waveform of primary switch in a current-mode flyback converter operating in the discontinuous conduction mode (DCM). During the first time interval, the drain current ramps up until the desired current level is reached. The power MOSFET then turns off. The leakage inductance in the flyback transformer rings with the MOSFET parasitic capacitance and causes a high voltage spike, which is limited by a clamp circuit. After the inductive spike has damped, the drain voltage equals to the input voltage plus the reflected output voltage. The drain voltage would immediately drop to the bus voltage when the current in the output diode drops to zero if the parasitic ring of the primary inductance and the parasitic capacitance is ignored. However, the drain voltage rings down to this level as shown in Fig 1 due to the parasitic resonance by the primary inductance and parasitic capacitance.

For example the inductance is 1mH and the parasitic capacitance is 100pF, then the resonant frequency is 500 kHz. The resonant circuit is lightly damped and the resonant frequency given below is independent of the input voltage and load currents:

$$f_{\text{resonant}} = \frac{1}{2\pi \cdot \sqrt{L_m \cdot C_{\text{eqp}}}}$$

where L_m is the primary inductance; C_{eqp} is the equivalent primary side parasitic capacitance which including parasitic capacitance of the primary winding, the parasitic capacitance of the MOSFET and the parasitic capacitance of the secondary side (including the secondary winding and output rectifier diode) reflect to primary side.

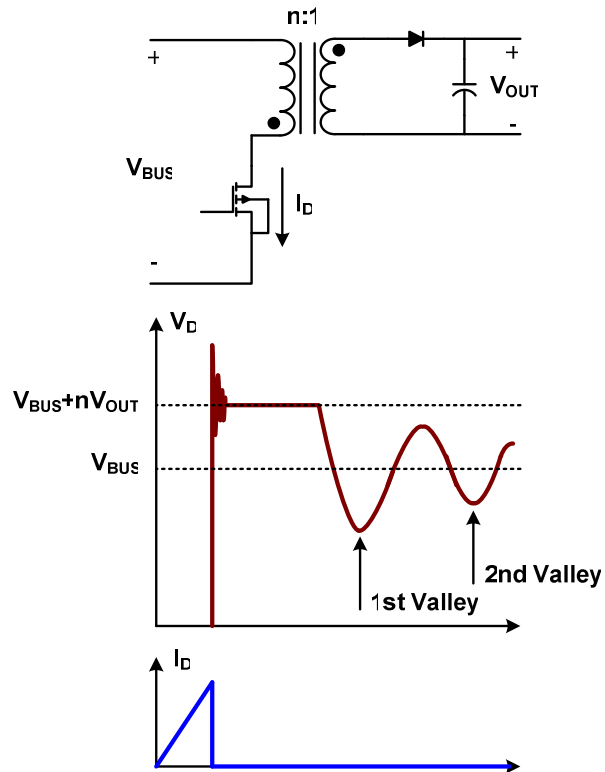


Figure 1 — Single-Pulsed Flyback Converter

In a conventional fix frequency flyback converter at DCM operation the primary switch (MOSFET) is turned on at a fixed frequency and turned off when the current reaches the desired level. The device's turn-on time may occur at any point during this parasitic resonance. In some cases the device may turn on when the drain voltage is lower than the bus voltage (means low switching losses and high efficiency), and in some cases the switch will turn on when the drain voltage is higher above the bus voltage (means high switching loss). This characteristic is often observed on the efficiency curves of a discontinuous flyback converters with a constant load, the efficiency fluctuated with the input voltage as the turn-on switching loss changes due to the variation of the drain voltage at the turn on point.

In quasi-resonant (QR) operation, the switch does not have a fixed switching frequency. Instead, the switch will always turn on by the controller when the drain voltage reaches its minimum value (valley point, refer to Fig.2). The time period T_w is half the resonant period determined by the transformer magnetizing inductance and parasitic capacitance. The switch on time (T_1 in Fig 2) is determined by the output feedback loop as conventional peak current mode control. The energy stored in the magnetizing inductor is fully transferred to the output. For light load condition, the time T_1 is small as less energy is required by the load, resulting in small peak current, and also a shorter output diode conduction time. Therefore, the switching frequency increases in the QR flyback as load decreasing, which may deteriorate the light load efficiency and challenges the EMI design. In order to eliminate these problems, a frequency-clamp function is usually added into the controller to limit the maximum switching frequency when load decreasing, which further improves the light load efficiency and simplifies the converter design.

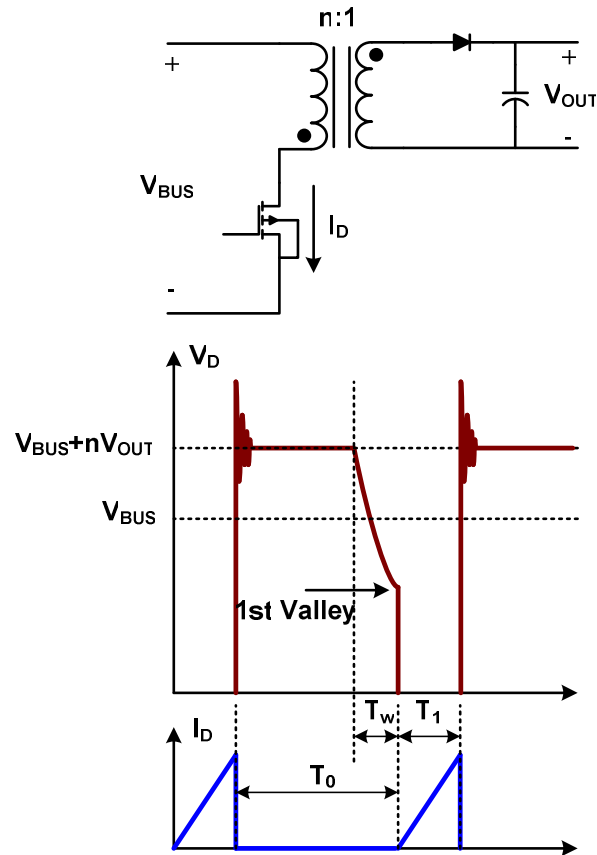


Figure 2 — Quasi-Resonant Flyback Converter

Compared to the traditional flyback under CCM and DCM operation, the Quasi-resonant operation can minimize the turn on switching loss of the switch by switching at the valley point, thus increasing efficiency and lowering device temperature rise. Its main disadvantage that of higher switching frequency at light load is eliminated by the frequency-clamp function in controllers. Also, by switching at low voltages and currents, the EMI generated by quasi-resonant operation is relatively low.

MPS provides HFC0100 for the quasi-resonant flyback solution, the internal valley detector ensures valley switching for high efficiency and low EMI. The minimum 8 μ s off time limits the maximum switching frequency when load decreases. When the load is fairly light, HFC0100 will force the system into burst mode operation to further reduce the equivalent switching frequency.

3. DESIGN PROCEDURE

A. Predetermine the Input and Output Specifications.

- Input AC voltage range: $V_{ac(min)}$, $V_{ac(max)}$, for example $90V_{ac} \sim 265V_{ac}$ RMS
- DC bus voltage range: $V_{in(max)}$, $V_{in(min)}$.
- Output: V_{out} , $I_{out(min)}$, $I_{out(max)}$, P_{out}
- Estimated efficiency: η , It is used to estimate the power conversion efficiency to calculate the maximum input power. Generally, η is set to be 0.8~0.9 according to different output applications.

Then the maximum input power can be given as:

$$P_{in} = \frac{P_{out}}{\eta} \quad (1)$$

Fig.3 shows the typical DC bus voltage waveform. The DC input capacitor C_{in} is usually set as $2\mu F/W$ of input power P_{in} for the universal input condition. For 230V single range application, the capacitance can be half the value.

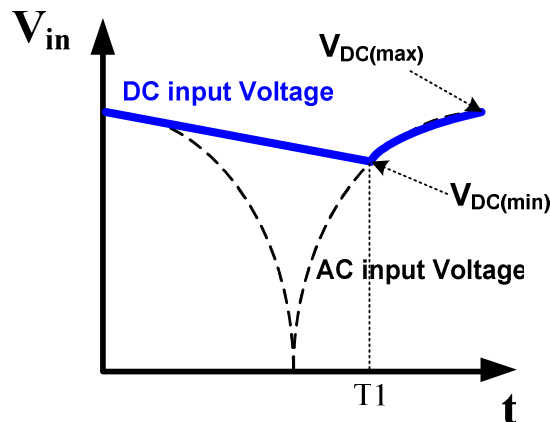


Figure 3 — Input Voltage Waveform

From the waveform above, the AC input Voltage V_{AC} and DC input Voltage V_{DC} can be got as:

$$V_{AC}(V_{ac}, t) = \sqrt{2} \cdot V_{ac} \cdot \cos(2 \cdot \pi \cdot f \cdot t) \quad (2)$$

$$V_{DC}(V_{ac}, t) = \sqrt{2 \times V_{ac}^2 - \frac{2 \times P_{in}}{C_{in}} \times t} \quad (3)$$

By setting $V_{AC}=V_{DC}$, $T1$ where DC input voltage had reached to its minimum $V_{DC(min)}$ can be calculated.

$$V_{DC(min)} = V_{DC}(V_{ac(min)}, T1) \quad (4)$$

Then, the minimum average DC input voltage $V_{in(min)}$ can be got as:

$$V_{in(min)} = \frac{\sqrt{2} \cdot V_{ac(min)} + V_{DC(min)}}{2} \quad (5)$$

The maximum average DC input voltage $V_{in(max)}$ can be got as:

$$V_{in(max)} = \sqrt{2} \cdot V_{ac(max)} \quad (6)$$

B. Determine the Startup Circuitry

Fig.4 shows the startup circuit, when power is on, the internal 2mA current charges C1 through R1 connected on HV pin of HFC0100. Once VCC voltage reaches 12V, the internal high voltage current source (2mA) turned off and IC start switching, then the auxiliary winding take over the power supply. If VCC dropped below 8V before the auxiliary winding take over the power supply, the switching is stopped

and the internal high voltage current source turned on again, re-charge the VCC external capacitor C1 (see Fig.5).

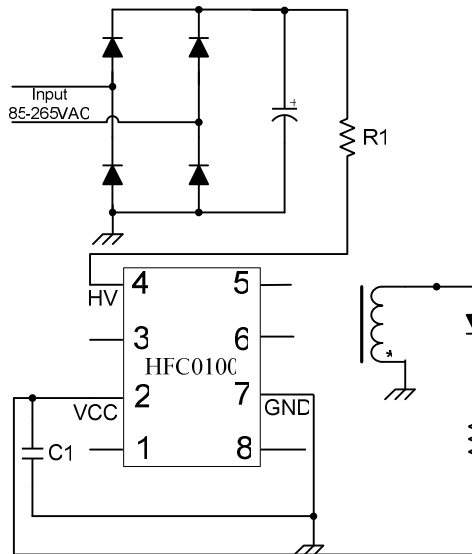


Figure 4 — The Startup Circuit with HFC0100

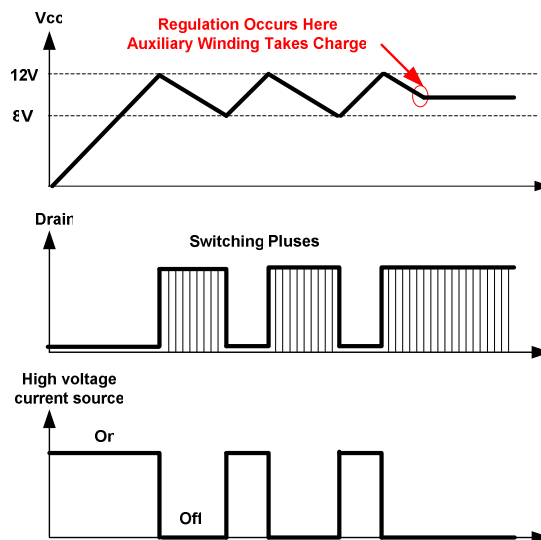


Figure 5 — The Startup and VCC UVLO of HFC0100

C. Valley Switching Detector and OVP Circuitry

Fig.6 shows the VSD pin circuitry. The VSD pin is connected to the auxiliary winding by R_{VSD} . The VSD pin is used for two functions:

- Detects the valley voltage of the switching waveform to achieve the valley voltage switching, which ensures QR operation to minimize the switching losses and reduces EMI.
- An internal voltage comparator and 6V reference voltage provide an output OVP

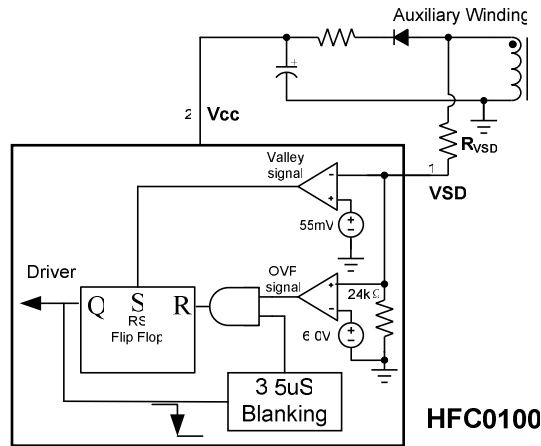


Figure 6 — The VSD Pin Circuitry of HFC0100 to Ensure Valley Switching

The internal valley switching signal occurs when the VSD pin voltage reaches:

$$(V_{DS} - V_{in}) \cdot \frac{N_{aux}}{N_{pri}} \cdot \frac{24k\Omega}{24k\Omega + R_{VSD}} < 55mV$$

where V_{DS} is the Drain-Source Voltage of the primary FET; N_{aux} is the auxiliary winding Turns of the transformer and N_{pri} is primary winding turns of the transformer.

The output OVP is achieved by detecting the positive plateau of auxiliary winding voltage which is proportional to the output voltage (see Fig.7). The output OVP setting point can be calculated as:

$$V_{out-p} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{24k\Omega}{24k\Omega + R_{VSD}} > 6V$$

where V_{out-p} is the output OVP setting voltage; N_{aux} is the auxiliary winding Turns of the transformer and N_{sec} is secondary winding turns of the transformer.

To avoid the mis-trigger due to the oscillation of the leakage inductance and the parasitic capacitance (see Fig.7) after primary switch turns off, the OVP sampling has a T_{OVPS} blanking period, typical 3.5us.

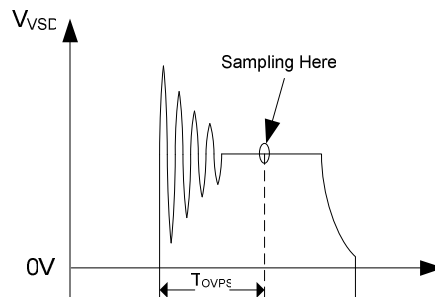


Figure 7— The OVP Sampling and T_{OVPS} Blanking

D. Turns Ratio-N, Primary MOSFET and Secondary Rectifier Diode Selection

Fig.8 shows the typical Drain-Source voltage waveform of the primary MOSFET and secondary rectifier

diode in a quasi-resonant flyback converter. From the waveform, the primary MOSFET Drain-Source voltage rating V_{P-MOS} can be got as:

$$V_{P-MOS} = \frac{V_{in(max)} + V_{RO} + 60V}{k} \tag{7}$$

where k is the derating factor which is typically selected as 0.9. V_{RO} is the reflected output voltage: $V_{RO} = N \cdot V_{OUT}$, 60V spike voltage is assumed here.

The secondary rectifier diode voltage rating V_{DIODE} can be got as:

$$V_{DIODE} = \frac{V_{in(max)} / N + V_{OUT}}{k} \tag{8}$$

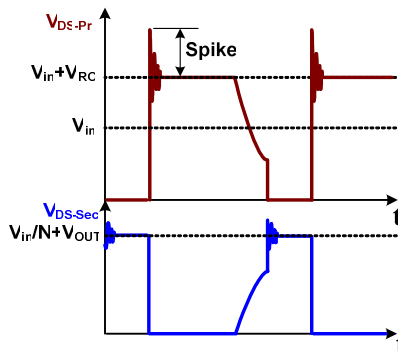


Figure 8 — Drain-Source Voltage of Primary MOSFET and Secondary Rectifier Diode

From (7) and (8), the voltage rating of primary MOSFET and secondary rectifier diode versus turns-ratio N can be shown in Fig 9. Then the turns-ratio N can be determined for the required MOSFET and Rectifier diode voltage rating. For example, in 24V output adapter application, 650V MOSFET and 100V rectifier diode is preferred for better performance. From Fig.9, $N=6$ is selected for the required voltage rating. Sometimes N can be selected within a range, then smaller N means larger duty on secondary and lower voltage stress on primary (more power loss on secondary and less power loss on primary); while larger N means smaller duty on secondary and higher voltage stress on primary (more power loss on primary and less power loss on secondary).

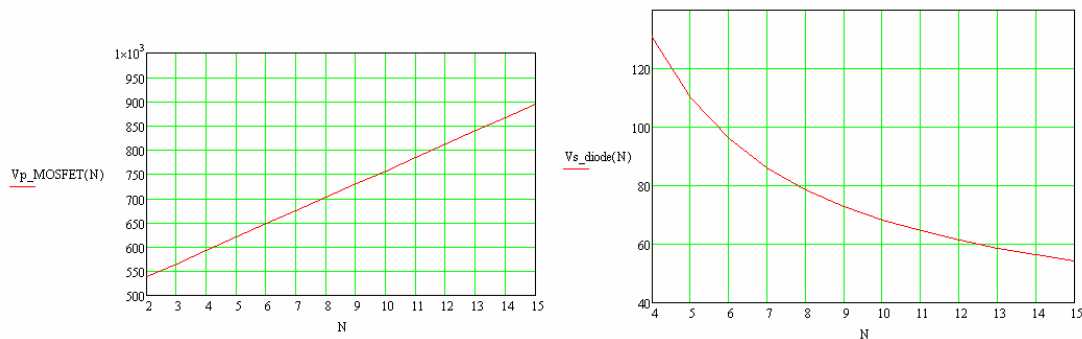


Figure 9—Voltage Rating of Primary MOSFET and Secondary Rectifier Diode vs. Turn Ratio-N

E. Primary Inductance L_m , Peak Current I_P and OLP Function

Primary inductance L_m and peak current I_P determines the power can be transferred to the output side:

$$P_{in} = \frac{1}{2} \cdot L_m \cdot I_P^2 \cdot f_s \tag{9}$$

Fig.10 shows the primary side MOSFET Drain-Source voltage and current waveform in a quasi-resonant flyback converter. It is preferred that the primary switch turns on at the first valley at heavy load condition to minimize the peak current. Each time period can be calculated as:

$$T_{on} = \frac{L_m \cdot I_P}{V_{in}} \tag{10}$$

$$T_{OFF} = \frac{L_m \cdot I_P}{N \cdot V_{OUT}} \tag{11}$$

$$T_w = \pi \cdot \sqrt{L_m \cdot C_{eqp}} \tag{12}$$

where C_{eqp} is the equivalent parasitic capacitance of the primary side, including parasitic capacitance of the primary winding and secondary winding, the parasitic capacitance of the MOSFET and the output rectifier.

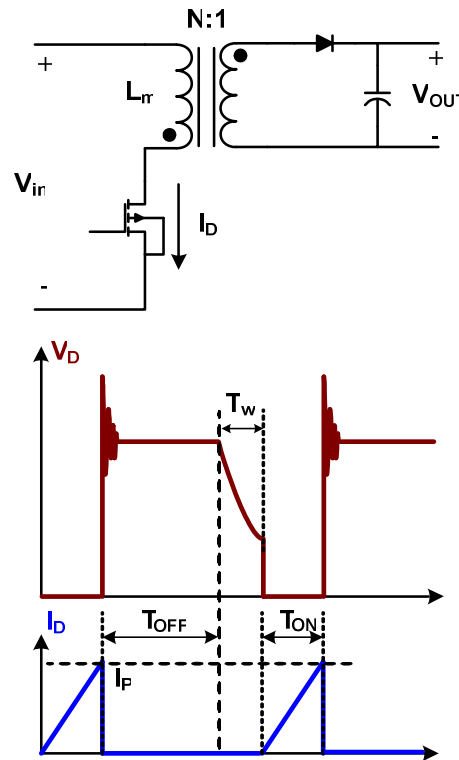


Figure 10 — Drain-Source voltage and current of Primary MOSFET in Quasi-Resonant Flyback Converter

From (10) (11) and (12), the switching frequency is given as:

$$f_s = \frac{1}{T_{ON} + T_{OFF} + T_w} \quad (13)$$

Take (1) (10) (11) (12) and (13) into equation (9), assume the power loss mainly is dominated by the secondary side:

$$\frac{P_{OUT}}{\eta} = \frac{1}{2} \cdot L_m \cdot I_P^2 \cdot \frac{1}{\frac{L_m \cdot I_P}{V_{in}} + \frac{L_m \cdot I_P}{N \cdot V_{OUT}} + \pi \cdot \sqrt{L_m \cdot C_{eqp}}} \quad (14)$$

Usually the T_w only has a small amount of the total switching period, which can be neglected for simplicity. Thus, (14) can be simplified as:

$$\frac{P_{OUT}}{\eta} = \frac{1}{2} \cdot L_m \cdot I_P^2 \cdot \frac{1}{\frac{L_m \cdot I_P}{V_{in}} + \frac{L_m \cdot I_P}{N \cdot V_{OUT}}} \quad (15)$$

From (15), the primary peak current I_P can be got as:

$$I_P(V_{in}) = \frac{2 \cdot P_{OUT}}{\eta} \cdot \left[\frac{1}{V_{in}} + \frac{1}{N \cdot V_{OUT}} \right] \quad (16)$$

Then, the maximum peak current I_P at the minimum input line is $I_{P(Vin(min))}$. So that the primary inductance L_m can be got from (9) as:

$$L_m = \frac{2 \cdot P_{OUT}}{\eta} \cdot \frac{1}{I_{P(Vin(min))}^2 \cdot f_{smin}} \quad (17)$$

Where f_{smin} is the expected minimum switching frequency at low line with full load condition, for example assume the f_{smin} as 60kHz, then I_P and L_m can be calculated according to (16) and (17).

As introduced in the previous section, in order to avoid the very high switching frequency at light load condition for quasi-resonant operation, the controller usually contains a frequency-clamp function to limit the maximum switching frequency. For HFC0100, it has 8us minimum-off time to limit the switching frequency.

Be sure that the off time at low line and full load does not fall below the allowed minimum-off time of HFC0100. The calculated inductance use (17) should be above the minimum inductance, which is given as:

$$L_m \geq \frac{N \cdot V_{OUT} \cdot (T_{off_min} - T_w)}{I_{p(Vin(min))}} \quad (18)$$

Where T_{off_min} is the minimum off time, i.e. 8us; and T_w is given in (12).

If the calculated inductance at low line and full load condition with (17) is above the minimum value, the design is OK. Otherwise, we need to adjust the transformer turns-ratio N or decrease f_{smin} to do the re-design

HFC0100 employs an external sense resistor R_{SENSE} to detect the load for primary current limiting. If the primary peak current I_P is high enough which causes the voltage on R_{SENSE} exceeds the internal current limiting reference voltage ($V_{ref}=1V$), the controller will shut off the switching cycle. To simply explain the design of R_{SENSE} , it is assumed that, the current limiting function is expected to be triggered when output current has reached 105% $I_{out(max)}$. Then the output power will be $\alpha \cdot P_{out}$ ($\alpha=105\%$), (15) changes to:

$$\frac{\alpha \cdot P_{OUT}}{\eta} = \frac{1}{2} \cdot L_m \cdot I_{P-L}^2 \cdot \frac{1}{\frac{L_m \cdot I_{P-L}}{V_{in(min)}} + \frac{L_m \cdot I_{P-L}}{N \cdot V_{OUT}}} \quad (19)$$

where I_{P-L} is the primary peak current limiting value, from (19) it can be got that:

$$I_{P-L} = \frac{2 \cdot \alpha \cdot P_{OUT}}{\eta} \cdot \left[\frac{1}{V_{in(min)}} + \frac{1}{N \cdot V_{OUT}} \right] \quad (20)$$

then the sense resistor R_{SENSE} can be calculated as:

$$R_{SENSE} = \frac{V_{ref}}{I_{P-L}} \quad (21)$$

where V_{ref} is the internal current limiting reference voltage, which is about 1V.

For HFC0100, it has internal OLP (Over Load Protection) function for safe operation. Because the maximum output power is limited by the maximum switching frequency and maximum primary peak current. If the output consumes more than the maximum output power, the output voltage will drop below the set point, the feedback loop will reduce the current through the optocoupler LED to try to keep the output voltage, and FB pin voltage will increase.

By continuously monitoring the FB pin voltage, when the feedback voltage exceeds the threshold $V_{OLP}=3.4V$, the gate drive signal is prohibited. The HFC0100 enters a safe low power operation that prevents from any thermal runaway or electrical over stress. As soon as the fault disappears, the power supply resumes operation.

During the start up or load transient, the FB voltage will be high enough temporarily to mis-trigger the OLP, to prevent this undesired protection, OLP circuit is designed to be triggered after V_{cc} is decreased below 8.5V.

F. Transformer Design

F-1. Transformer Core Selection

A core appropriate for certain output power at the operating frequency needs to be selected. Ferrite is widely adopted in flyback transformer. The core area product ($A_E A_W$) which is the core magnetic cross-section area multiplied by window area available for winding, is widely used for an initial estimate of core size for a given application. A rough indication of the required area product is given by following^[1]:

$$A_E \cdot A_W = \left(\frac{L_m \cdot I_P \cdot I_{rms} \times 10^4}{B_{max} \cdot K_u \cdot K_j \cdot f_{smin}} \right)^{4/3} \text{ cm}^4 \quad (22)$$

where K_u is winding factor which is usually 0.25~0.3 for an off-line transformer. K_j is the current-density coefficient (typically 400~450 for ferrite core). I_p and I_{rms} is the maximum peak current and RMS current of the primary inductance. B_{max} is the allowed maximum flux density in normal operation which is usually preset to be the saturation flux density of the core material (0.3T~0.4T). f_{smin} is the minimum switching frequency at low line with full load condition.

$$I_{rms} \approx \sqrt{\frac{L_m \cdot I_p^3}{3 \cdot V_{in(min)}} \cdot f_s} \quad (23)$$

Please refer to the manufacture's datasheet to select the proper core. For discontinuous mode operation, the winding area window is chosen as wide as possible to minimize AC winding losses. EC, ETD, EFD, LP cores are all E-E core shapes with large wide windows. Applications requiring low profile can benefit from using EFD cores.

F-2. Primary and Secondary Winding Turns

With a given core size, there is a minimum number of turns for the transformer primary side winding to avoid saturation. The normal saturation specification is E-T or volt-second rating. The E-T rating is the maximum voltage, E, which can be applied over a time of T seconds. (The E-T rating is identical to the product of inductance L and peak current) Equation (24) defines a minimum value of N_p for the transformer primary winding to avoid the core saturation:

$$N_p = \frac{L_m \cdot I_p}{B \cdot A_E} \times 10^6 \quad (24)$$

Where:

L_m = the primary inductance of the transformer

B = the maximum allowable flux density

A_E = the effective cross sectional core

I_p = the peak current in the primary side of the transformer, which is given in (16).

The maximum allowable flux density B should be smaller than the saturation flux density B_{sat} . Since B_{sat} decreases as the temperature goes high, the high temperature characteristics should be considered.

Secondary turn count is a function of turn ratio n and primary turn count N_p :

$$N_s = N_p / N \quad (25)$$

F-3. Wire Size

Once all the winding turns have been determined, wire size must be properly chosen to minimize the winding conduction loss and leakage inductance. The winding loss depends on the RMS current value, the length and the cross section of wire.

The wire size could be determined by the RMS current of the winding. For a flyback converter, the RMS current on secondary side is:

$$I_{sec-rms} \approx \sqrt{\frac{L_m \cdot I_p^3}{3 \cdot V_{OUT}} \cdot f_s \cdot N} \quad (26)$$

Then, the wire size required on secondary side is:

$$S = \frac{I_{\text{sec-rms}}}{J} \text{ (mm}^2\text{)} \quad (27)$$

Here J is the current density of the wire which is 5A/mm² typically.

Due to the skin effect and proximity effect of the conductor, the diameter of the wire selected is usually less than 2*Δd (Δd: skin effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_s \cdot \mu \cdot \sigma}} \quad (28)$$

where μ is the magnetic permeability of the conductor, which is usually equals to the permeability of vacuum for most conductor, i.e. $4\pi \times 10^{-7}$ H/m, σ is the conductivity of the wire (for copper, σ is typically 6×10^7 S/m at 0 deg, σ will be larger as temperature increases, which means the Δd will get smaller).

Therefore, multiple strands of thinner wire or Litz wire is usually adopted to minimize the AC resistance, the effective cross section area of multi-strands wire or Litz wire should large enough to meet the requirement set by the current density. Equation (23) and (27) can be used for primary wire size selection.

After the wire sizes have been determined, it is necessary to check whether the window area with selected core can accommodate the windings calculated in the previous steps. The window area required by each winding should be calculated respectively and added together, the area for interwinding insulation and spaces existing between the turns should also be taken into consideration. The fill factor, means the winding area to the whole window area of the core, should be well below 1 due to these interwinding insulation and spaces between turns. It is recommended that a fill factor no greater than about 30% be used. For transformers with multiple outputs this factor may need to be reduced further.

Based on these considerations, the total required window area is then compared to the available window area of a selected core. If the required window area is larger than the selected one, either wire size must be reduced, or a larger core must be chosen. Of course, a reduction in wire size increase the copper loss of the transformer.

F-4. Air Gap

With the selected core and winding turns, the air gap of the core is given as:

$$G = \mu_0 \cdot A_E \cdot \frac{N_P^2}{L_m} - \frac{l_c}{\mu_r} \quad (29)$$

where A_E is the cross sectional area of the selected core, μ_0 is the permeability of vacuum which equals $4\pi \times 10^{-7}$ H/m. L_m and N_P is the primary winding inductance and turns respectively, l_c is the core magnetic path length and μ_r is the relative magnetic permeability of the core material.

G. Design the RCD Snubber

In application, a small amount of energy is stored in the leakage inductance, which cannot be transferred to the output side in flyback converter. This amount of energy may result in a high voltage spike on the drain of the main switch, which should be well damped to protect the MOSFET.

The RCD snubber is usually adopted to clamp the drain voltage as shown in Fig 11. The value of the capacitor, C_{sn} , and resistor, R_{sn} , depend on the energy stored in the parasitic inductance, as the energy must be dissipated by the RC network during each cycle. The voltage across the capacitor and resistor sets the clamp voltage, V_{CLAMP} . Fig.12 shows the voltage of the primary MOSFET during turn-off phase with respect to V_{CLAMP} .

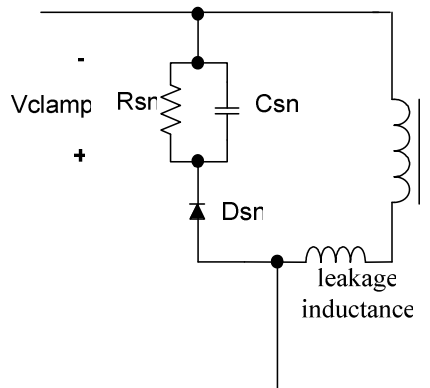


Figure 11 — RCD Snubber on Primary Side

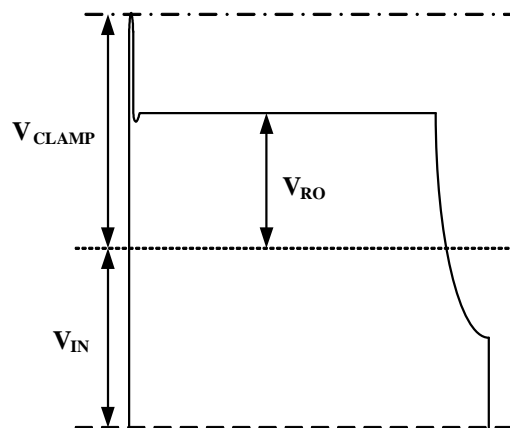


Figure 12 — MOSFET Drain Voltage and Snubber Capacitor Voltage

The energy stored in the leakage inductance can be obtained as:

$$P_{sn} = \frac{1}{2} \cdot L_{leakage} \cdot I_p^2 \cdot f_s \tag{30}$$

where I_p is the peak current in primary side.

For small leakage inductance application, the leakage energy given in (30) is partly dissipated in this RCD clamp circuit. For large leakage inductance application, the energy absorbed by the RCD clamp circuit is much larger than that given in (30) due to the long commutation time between the primary side and secondary side, thus part of the magnetizing energy is fed to the RCD clamp circuit instead of the

output side. The theoretical analysis is quite complex and will not be elaborated on here. Generally, we simply assume the energy stored in the leakage inductance is completely dissipated in the RCD clamp circuit. Typically, we can assume an acceptable clamp voltage V_{CLAMP} which is usually 50~100% higher than the reflected output voltage V_{RO} . The resistance can be calculated based on (31). In practice, this resistance can be adjusted based on the power loss and the acceptable clamp voltage, which usually is slightly higher than that calculated by (31).

$$V_{CLAMP} = \sqrt{P_{sn} \cdot R_{sn}} \quad (31)$$

The snubber capacitor C_{sn} should be selected considering the voltage ripple of V_{CLAMP} given in (32). Generally, a 5~10% ripple voltage is reasonable.

$$\Delta V_{sn} = \frac{V_{CLAMP}}{C_{sn} \cdot R_{sn} \cdot f_s} \quad (32)$$

H. Design the Output Filters

The RMS current of the output capacitor can be obtained as:

$$I_{cap-out} = \sqrt{I_{rms-sec}^2 - I_{out}^2} \quad (33)$$

where I_{out} is the output current and $I_{rms-sec}$ is the secondary RMS current in (26).

The RMS current should be smaller than the RMS current specification of the capacitor.

The voltage ripple on the output can be estimated by:

$$\Delta V_{out} = \frac{I_{out} \cdot (T_{OFF} + T_w)}{C_{out}} + (I_{sec-P} - I_{out}) \cdot R_{ESR} \quad (34)$$

where I_{sec-P} is the secondary side peak current; R_{ESR} is the ESR of output capacitor; T_{OFF} and T_w can be got from (11) (12).

Sometimes it is impossible to meet the ripple specification with a single electrolytic cap due to the high ESR. Then, additional LC filter or extra ceramic capacitor with low ESR paralleled with the electrolytic capacitor can be used.

4. DESIGN SUMMARY

- A detailed reference design of quasi-resonant flyback converter is shown in Fig 13. The input voltage is 90VAC to 265VAC with 24V/1.5A output capability. HFC0100 from MPS is adopted as the controller, which has valley switching to minimize the switching loss with improved efficiency and EMI.
- OCP function is achieved by the primary sense resistor connected with CS pin of HFC0100, when the primary current is high enough which caused the CS pin voltage exceeds 1V, the controller will turn off the switch to limit the current.
- By sensing the voltage on auxiliary winding into VSD pin of HFC0100, OVP function is achieved. When output voltage is too high which make the voltage on auxiliary winding trigger the OVP threshold of VSD pin, HFC0100 will latch off the switch until V_{CC} voltage restarted.
- The transformer used in this design has a turn ratio of 84:14:8 ($N_s: N_{p2}: N_{p1}$) turn ratio with 820uH

primary inductance. The auxiliary winding is used for powering the controller and detecting the V_{DS} to ensure DCM and valley switching.

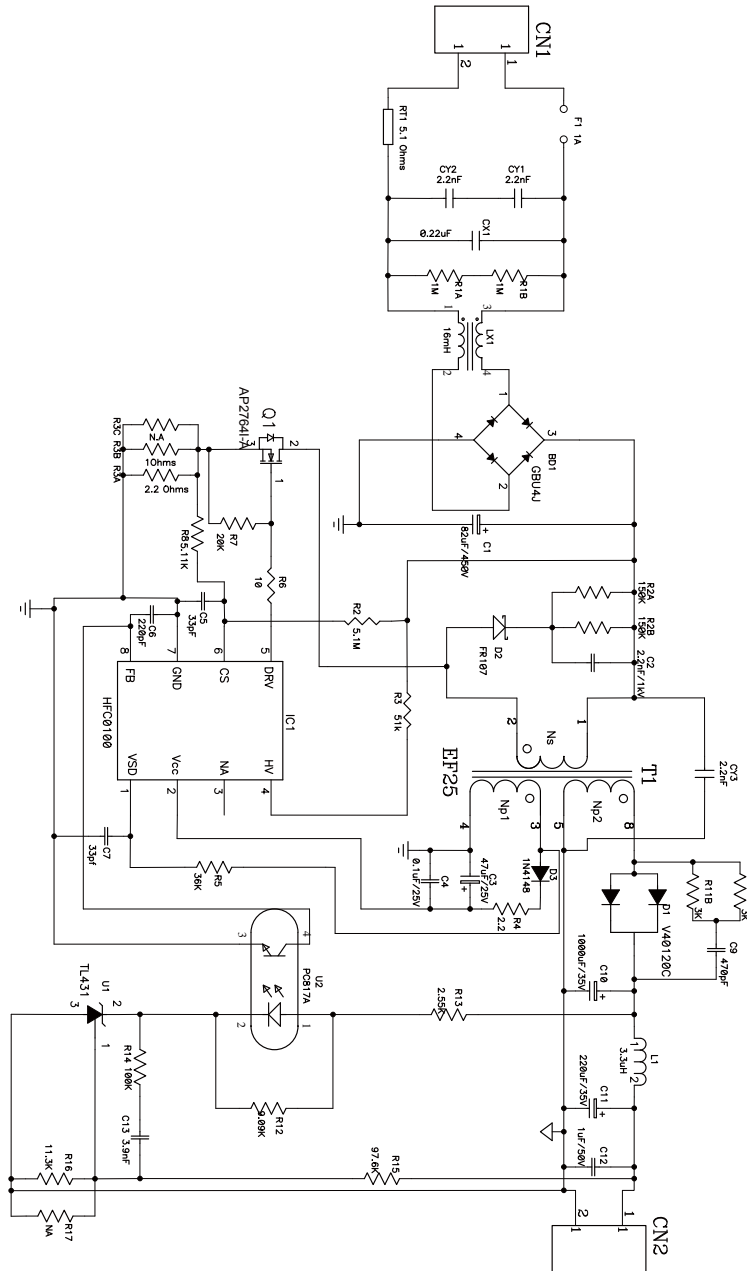


Figure 13 — Schematic of Quasi-Resonant Flyback Converter with HFC0100

5. EXPERIMENTAL VERIFICATION

In order to show the validity of the design procedure presented by this paper, the quasi-resonant flyback converter of the design example has been built and tested (Input: 90VAC~265VAC; Output: 24V/1.5A). All the components in the circuit are used as design example in Fig.13.

Fig.14 and Fig.15 shows the valley switching on primary side. At low line input in Fig.10, the switch is

turned on at the first valley point of Drain-Source voltage to minimize the turn-on loss; At high line input, because the time period between the switch turned off and the 1st valley point on drain-source voltage is smaller than the minimum-off-time (8us) of the controller, the switch is not turned off until the 2nd valley point on drain-source voltage is reached.

Fig.16 shows the Burst Mode function of the controller at light load. To minimize the power dissipation in no load or light load, HFC0100 enters the burst mode operation. As the load decreases, the FB voltage decreases, the HFC0100 stops the switching cycle when the FB voltage drops below the threshold V_{BRUL} —0.5V. And the output voltage starts to drop at a rate dependent on the load. This causes the FB voltage to rise again. Once the FB voltage exceeds the threshold V_{BRUH} —0.7V, switching resumes. The FB voltage then falls and rises periodically. The burst mode operation alternately enables and disables switching cycle of the MOSFET thereby reducing switching loss in the no load or light load conditions.

Fig.17 and Fig.18 shows the OCP and OVP function, when the output current or the output voltage exceeds the setting value, HFC0100 will latch off the switch to protect the whole system.

Fig.19 shows the measured efficiency versus output current. Benefit from valley switching, the efficiency exceeds 90% at full load condition. Also the power consumption at no load is very low (130mW at low line; 160mW at high line) because of the burst mode operation by HFC0100.

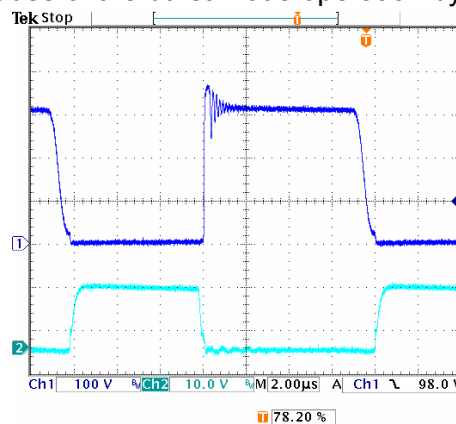


Figure 14 — Waveform of Valley Switching of Primary at Low Line Input (CH1: V_{GS} of Q1; CH2: V_{DS} of Q1)

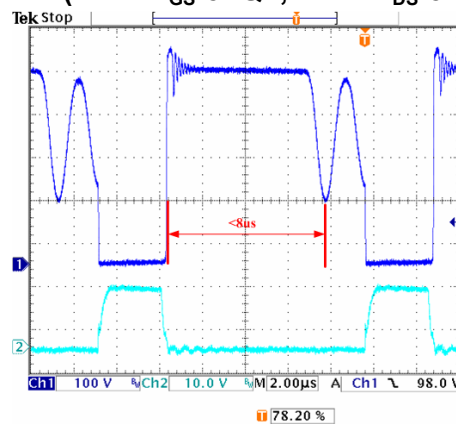


Figure 15 — Waveform of Valley Switching of Primary at High Line Input (CH1: V_{GS} of Q1; CH2: V_{DS} of Q1)

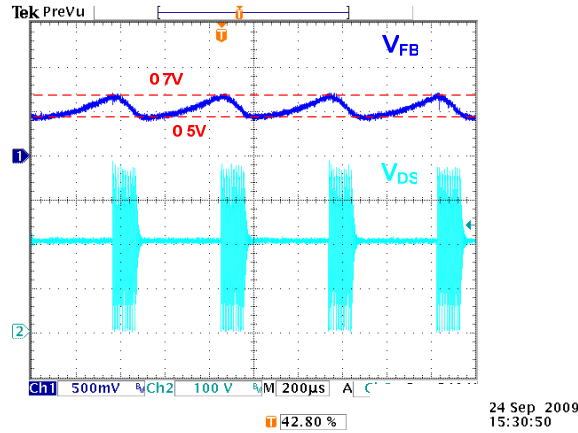


Figure 16 — The Burst Mode Function of HFC0100 (CH1: V_{FB}; CH2: V_{DS})

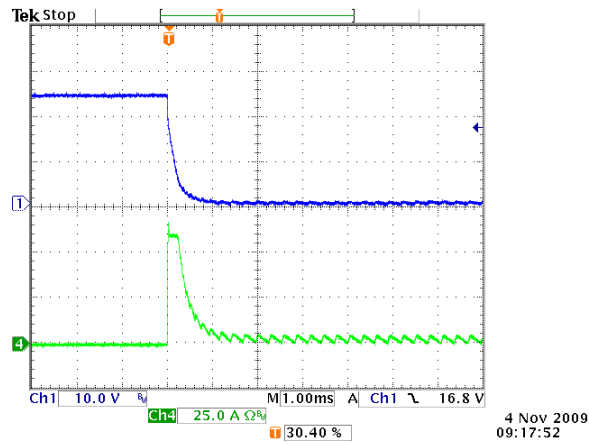


Figure 17 — The OCP Function of HFC0100 (CH1: V_{OUT}; CH4: I_{OUT})

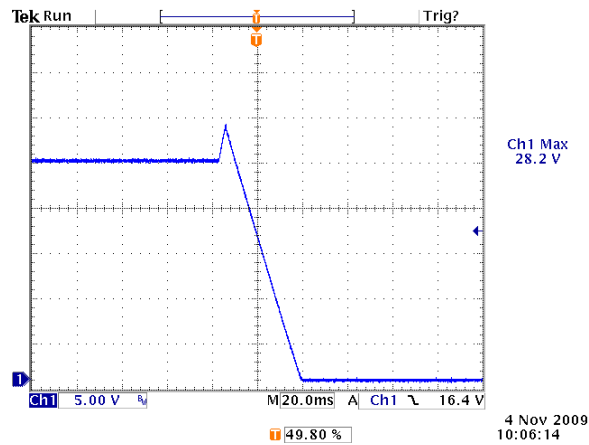


Figure 18 — The OVP Function of HFC0100 (CH1: V_{OUT})

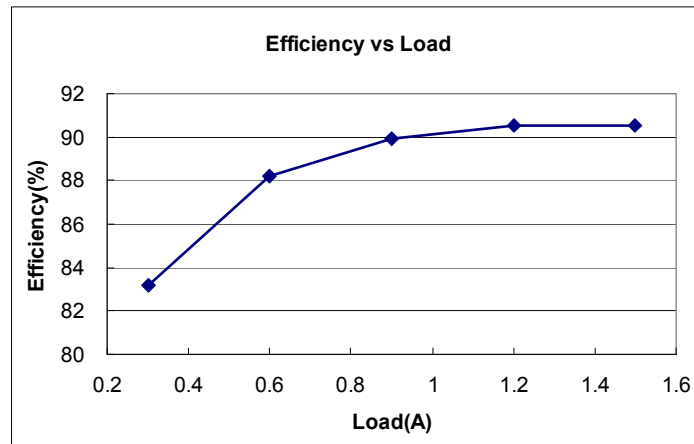


Figure 19 — The Efficiency of the System (220VAC Input)

6. REFERENCES

- [1]. Lloyd H. Dixon, "Magnetics Design for Switching Power Supplies," in Unitrode Magnetics Design Handbook, 1990.

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