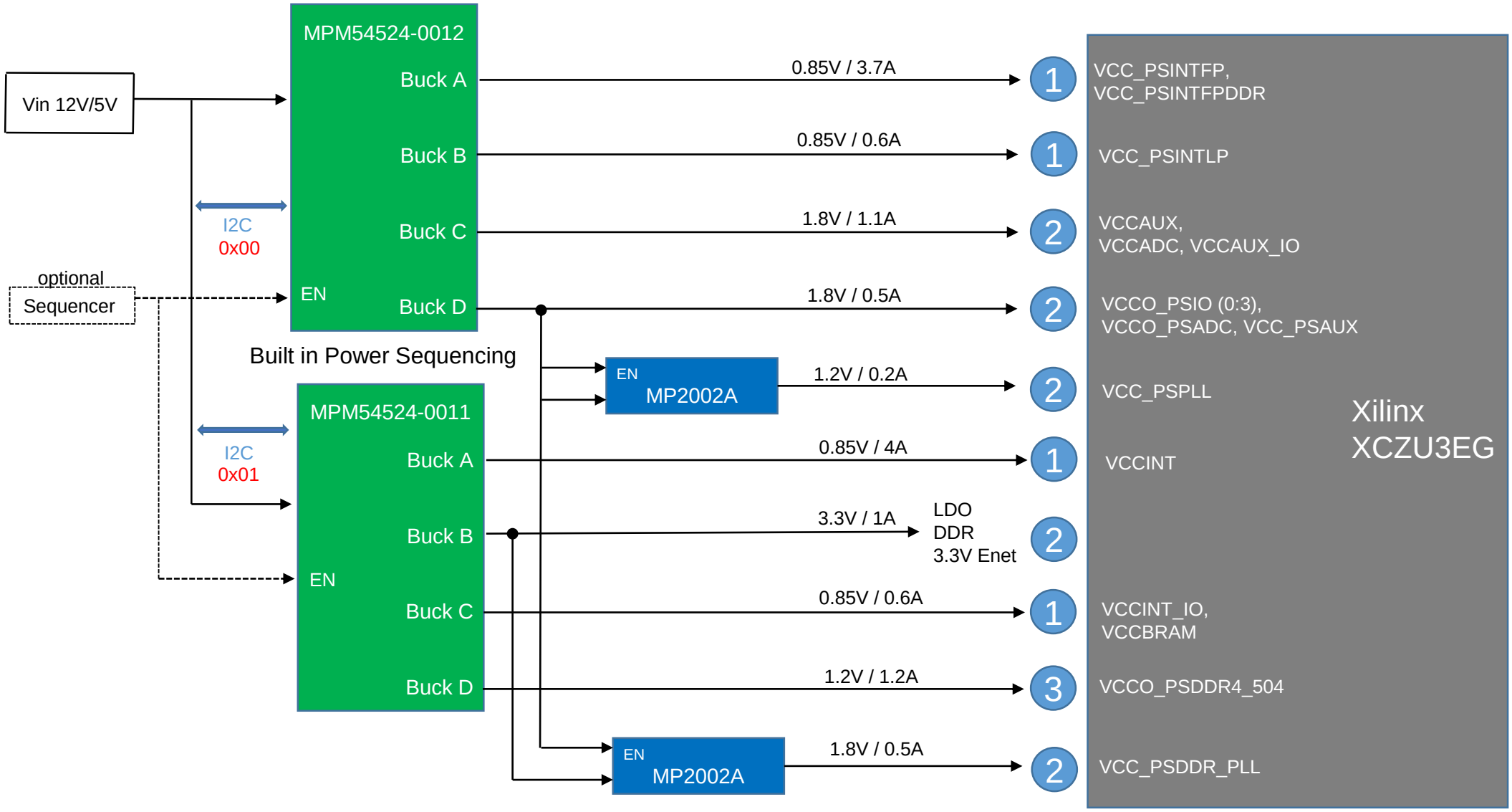
Xilinx XCZU3EG Test Report

MPM54524 Reference Design

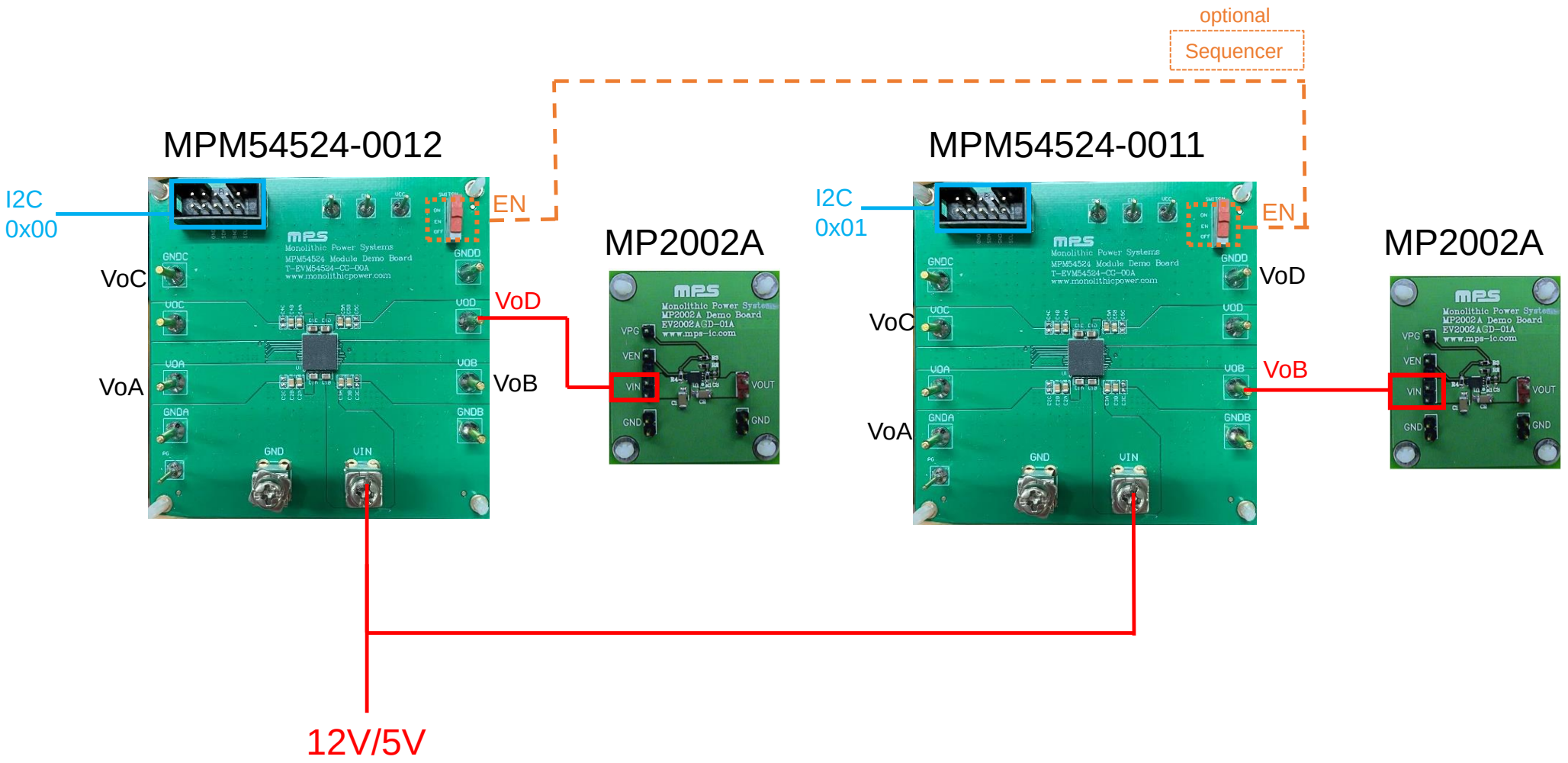
November 2022

MPM54524

Power Sequencing



MPM54524 EVB Connection

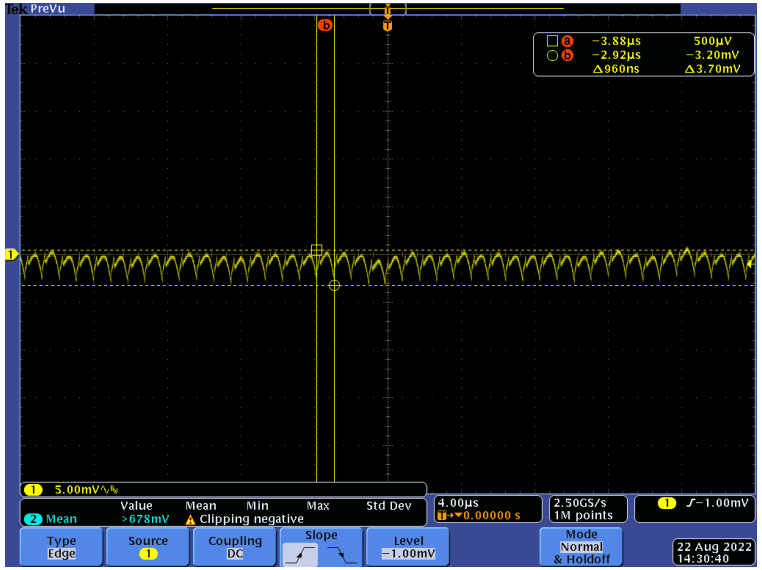


Design Targets

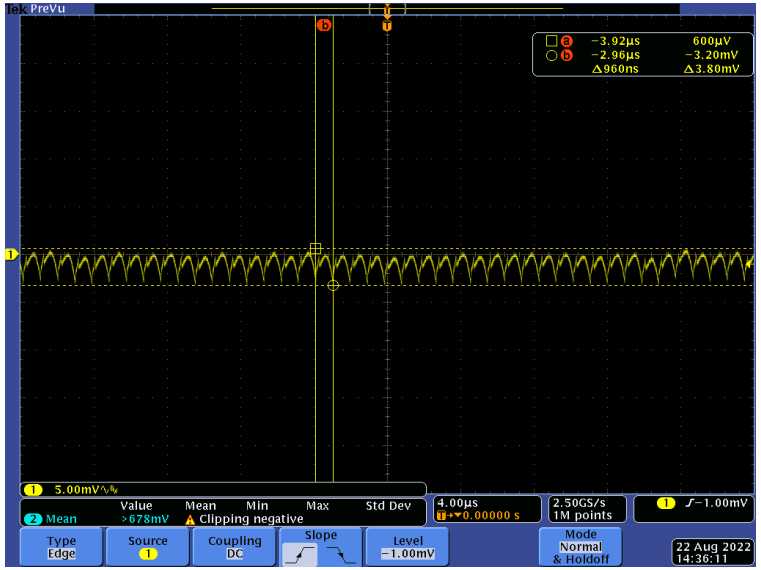
Rails	MPS Part #	Vin	Vo (V) No Load	AC + DC Tolerance	Max Current	Step Load	Slew Rate
VCC_PSINTFP	MPM54524	5	0.850	+/-3%	3.7A	0.93A→2.78A→0.93A	2.5A/us
VCC_PSINTLP	MPM54524	5	0.850	+/-3%	0.6A	N/A	N/A
VCCAUX	MPM54524	5	1.800	+/-3%	1.1A	N/A	N/A
VCCO_PSIO	MPM54524	5	1.800	+/-3%	0.5A	N/A	N/A
VCC_PSPLL	MP2002A	5	1.200	+/-3%	0.2A	N/A	N/A
VCCINT	MPM54524	5	0.850	+/-3%	4A	1A→3A→1A	2.5A/us
VCCINT_IO	MPM54524	5	0.850	+/-3%	0.6A	N/A	N/A
VCCO_PSDDR4	MPM54524	5	1.200	+/-3%	1.2A	N/A	N/A
VCC_PSDDR_PLL	MP2002A	5	1.800	+/-3%	0.5A	N/A	N/A

MPM54524 VCC_PSINTFP Ripple

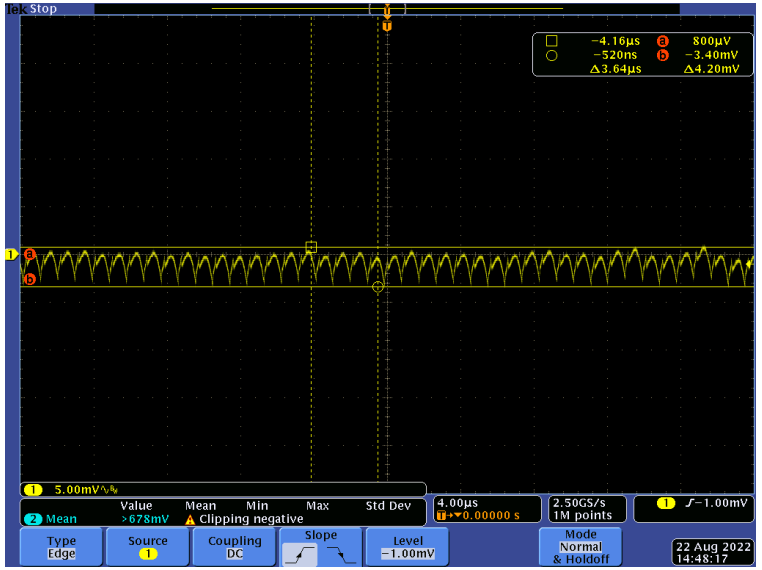
Standby



Half Load



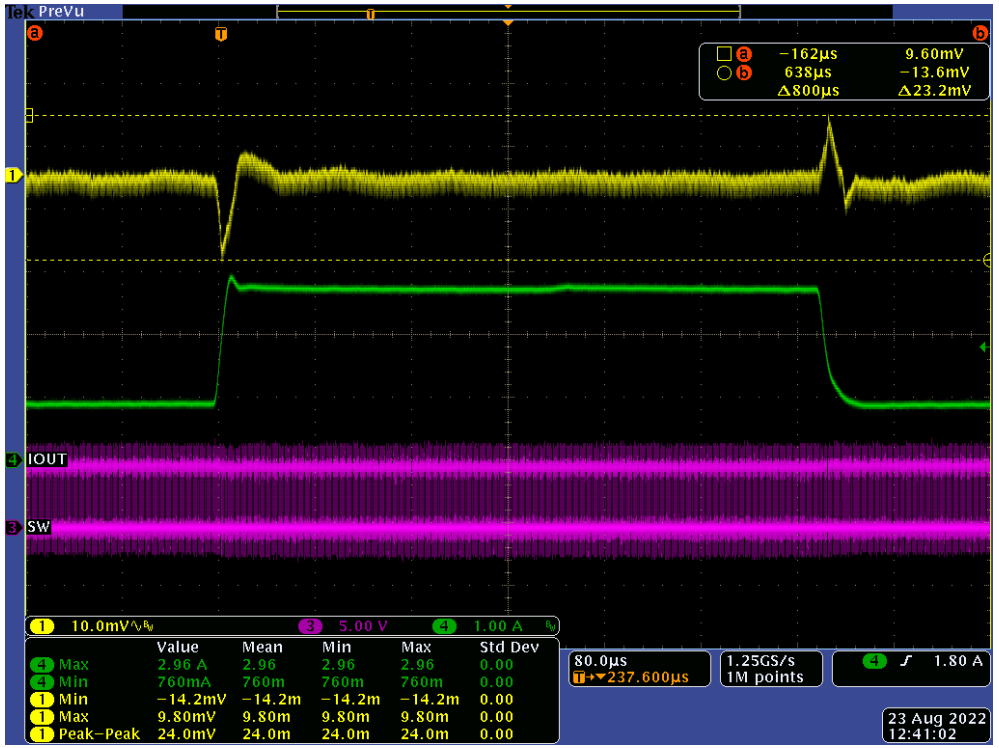
Max Load

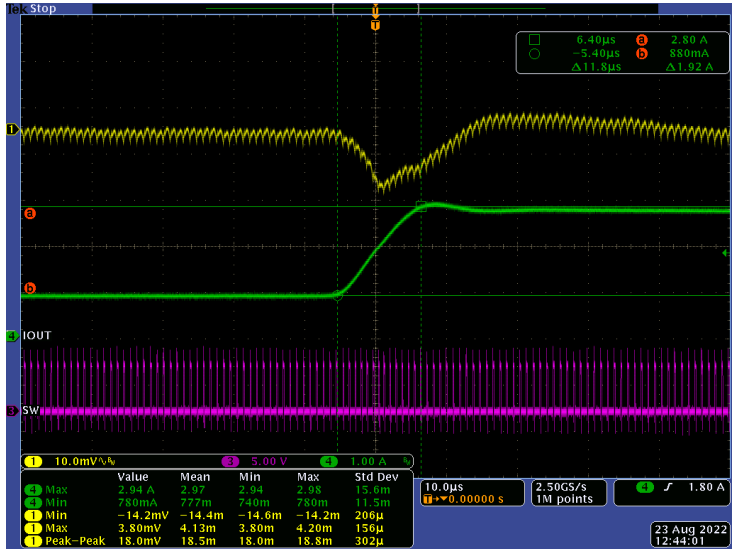


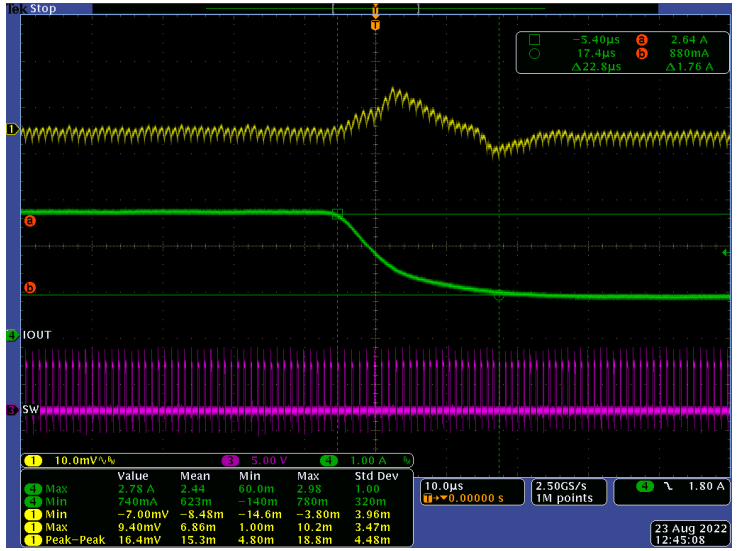
- ❑ 0.44% (3.7 mV) peak-peak ripple at Standby
- ❑ 0.45% (3.8 mV) peak-peak ripple at Half-Load
- ❑ 0.49% (4.2 mV) peak-peak ripple at Full-Load

MPM54524 VCC_PSINTFP Transient

Step Load: 0.93A → 2.78A → 0.93A, 2.5A/us



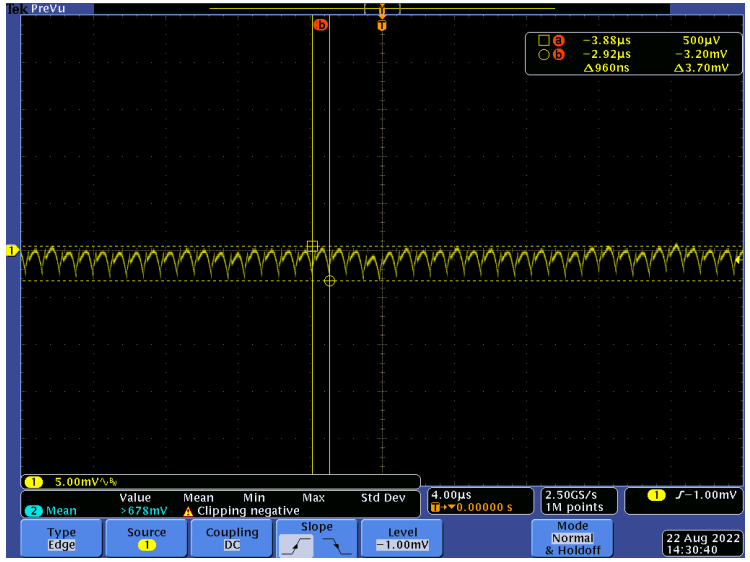




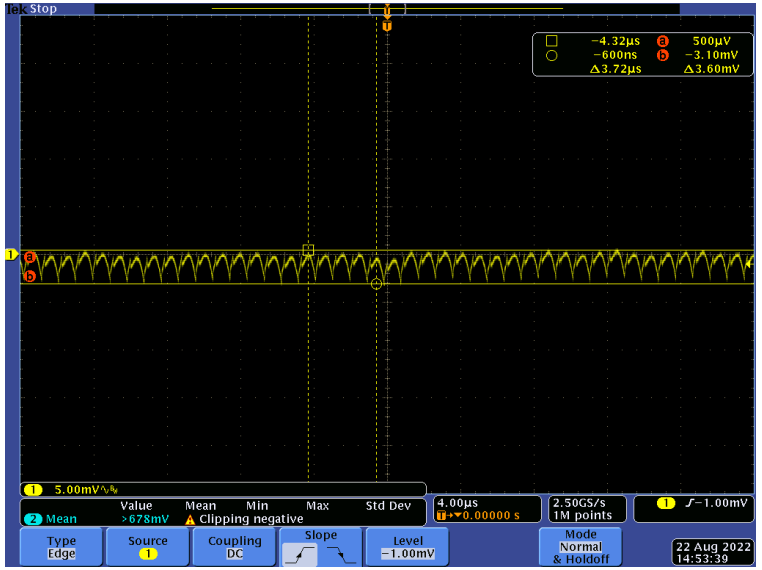
Vo ripple –1.67% (-14.2mV) to +1.15%(9.8mV) with load transient

MPM54524 VCC_PSINTLP Ripple

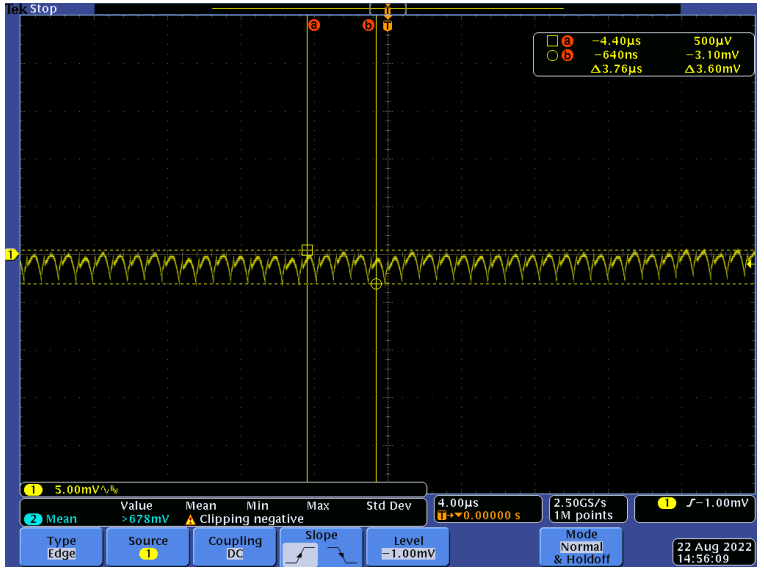
Standby



Half Load



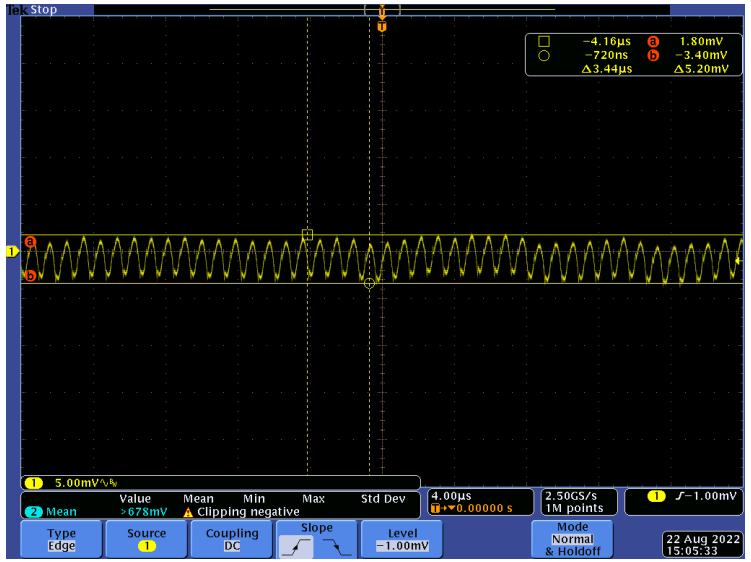
Max Load



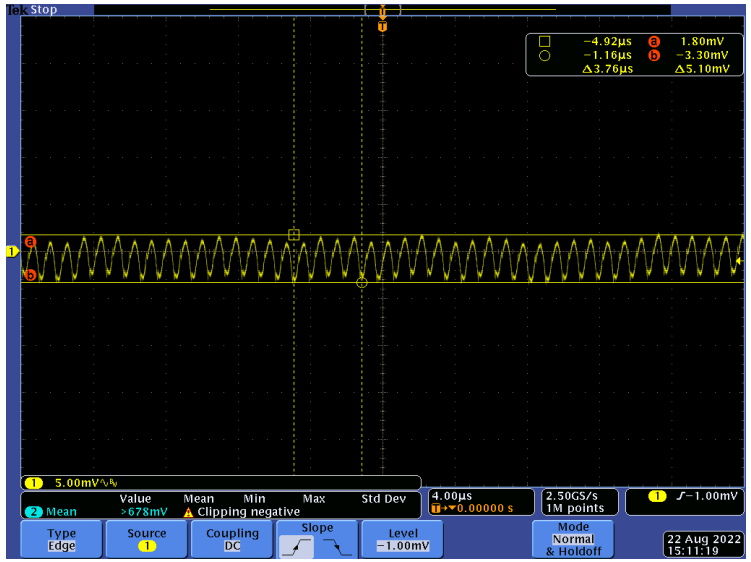
- 0.44% (3.7 mV) peak-peak ripple at Standby
- 0.42% (3.6 mV) peak-peak ripple at Half-Load
- 0.42% (3.6 mV) peak-peak ripple at Full-Load

MPM54524 VCCAUX Ripple

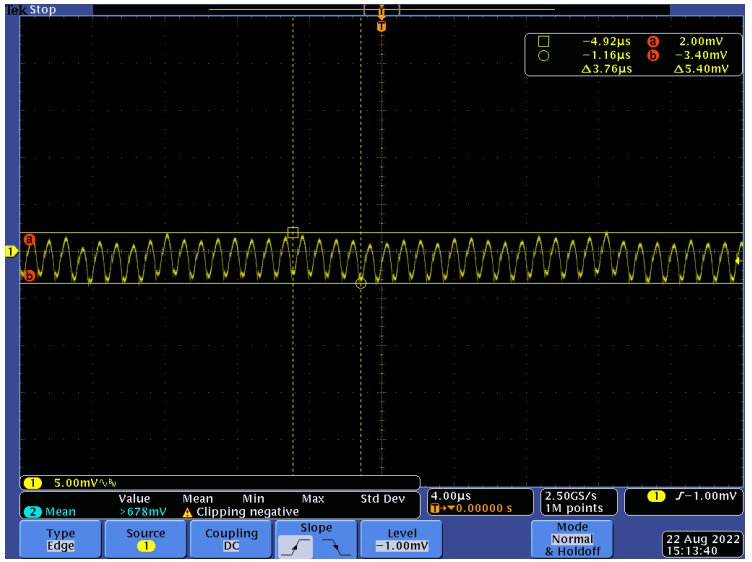
Standby



Half Load



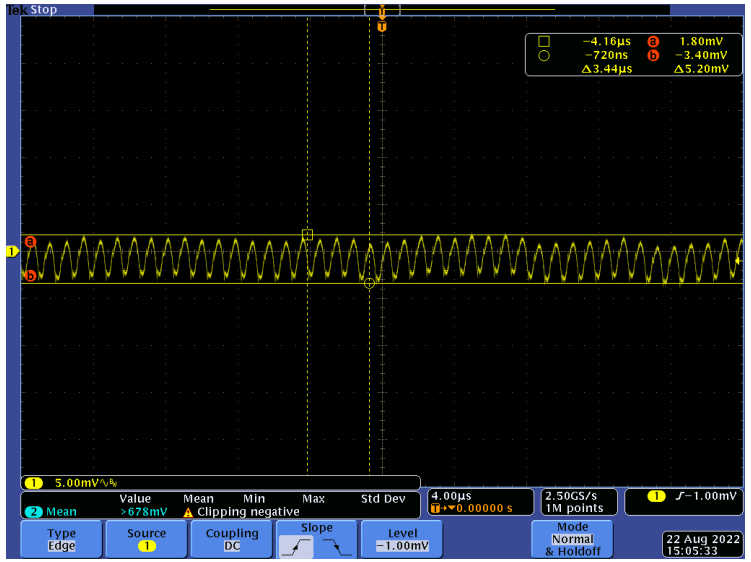
Max Load



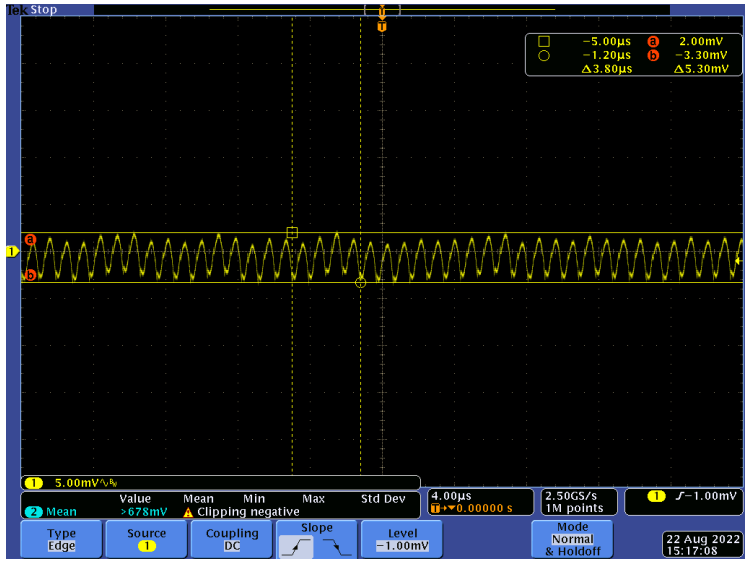
- ❑ 0.29% (5.2 mV) peak-peak ripple at Standby
- ❑ 0.28% (5.1 mV) peak-peak ripple at Half-Load
- ❑ 0.3% (5.4 mV) peak-peak ripple at Full-Load

MPM54524 VCCO_PSIO Ripple

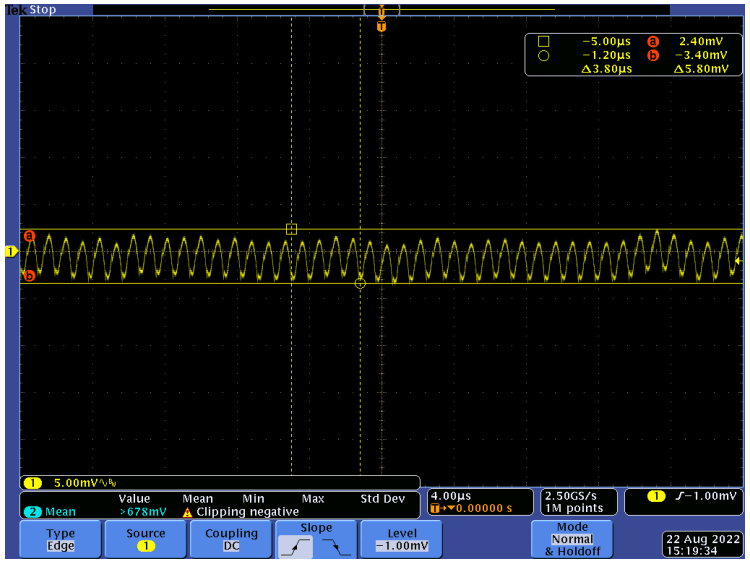
Standby



Half Load



Max Load

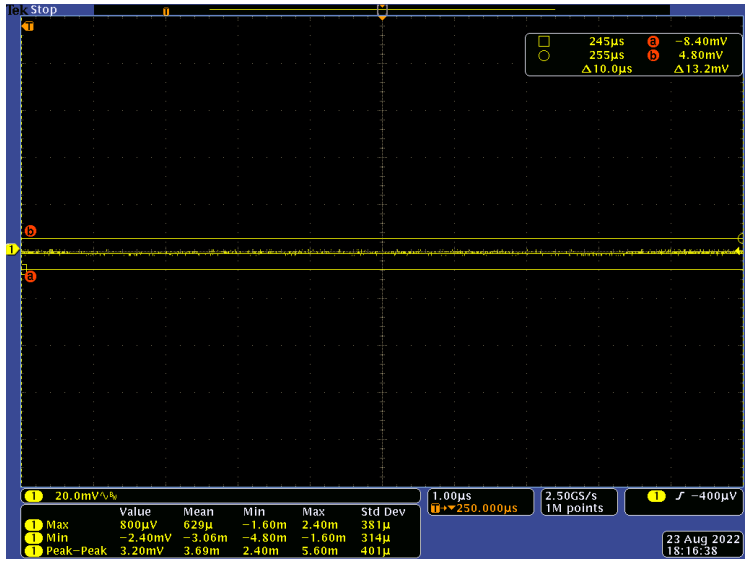


- ❑ 0.29% (5.2 mV) peak-peak ripple at Standby
- ❑ 0.29% (5.3 mV) peak-peak ripple at Half-Load
- ❑ 0.32% (5.8 mV) peak-peak ripple at Full-Load

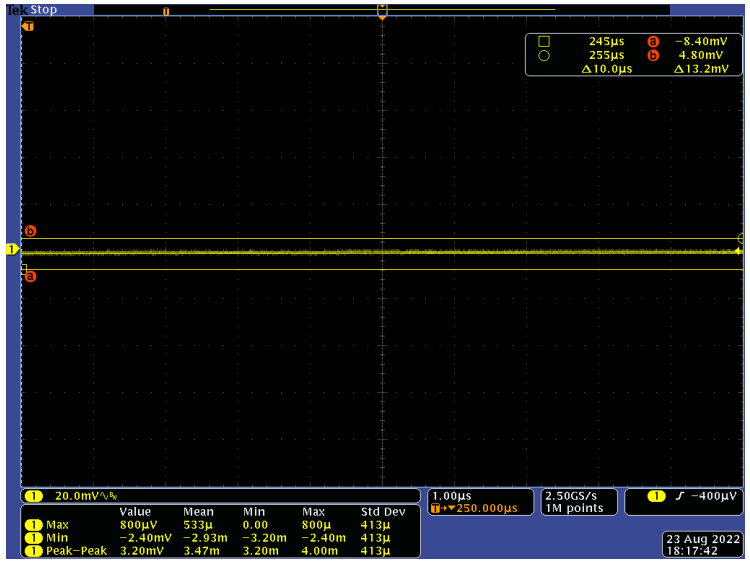
MP2002A VCC_PSPLL Ripple

Standby

Half Load



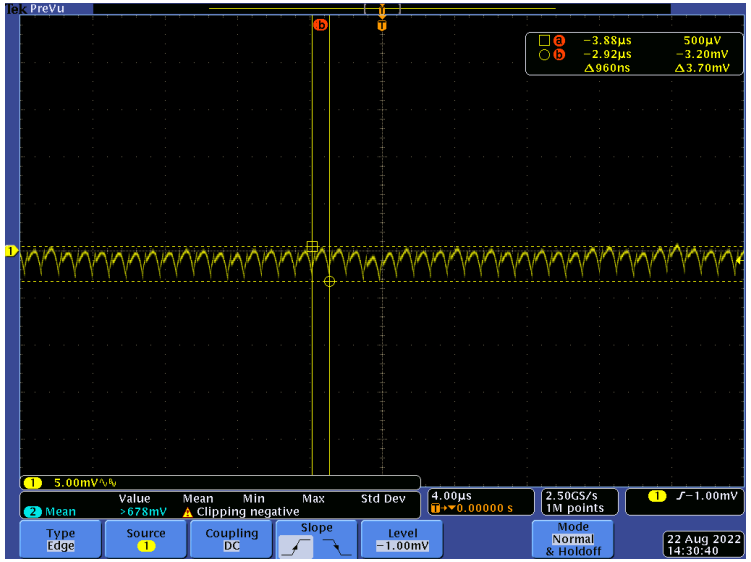
Max Load



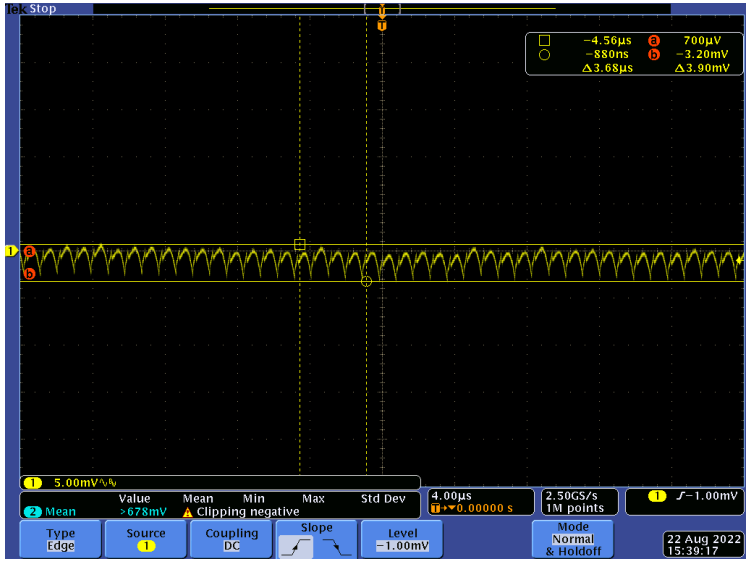
- ❑ 0.33% (4 mV) peak-peak ripple at Standby
- ❑ 0.27% (3.2 mV) peak-peak ripple at Half-Load
- ❑ 0.27% (3.2 mV) peak-peak ripple at Full-Load

MPM54524 VCCINT Ripple

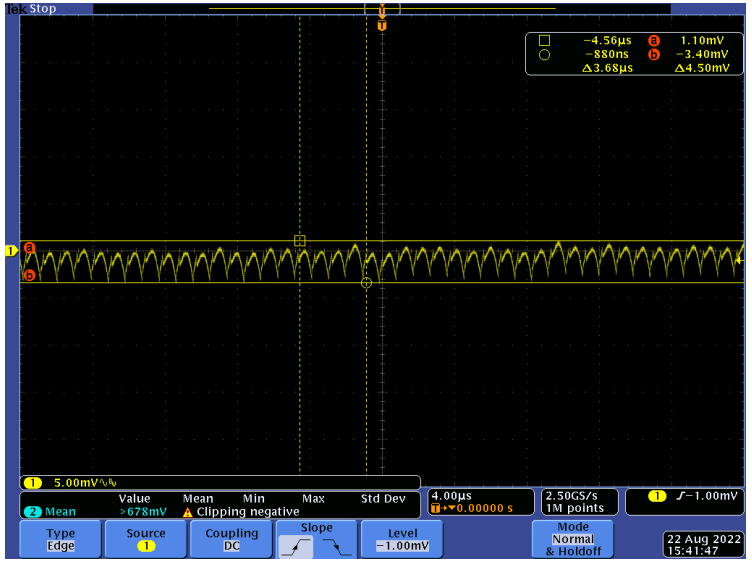
Standby



Half Load



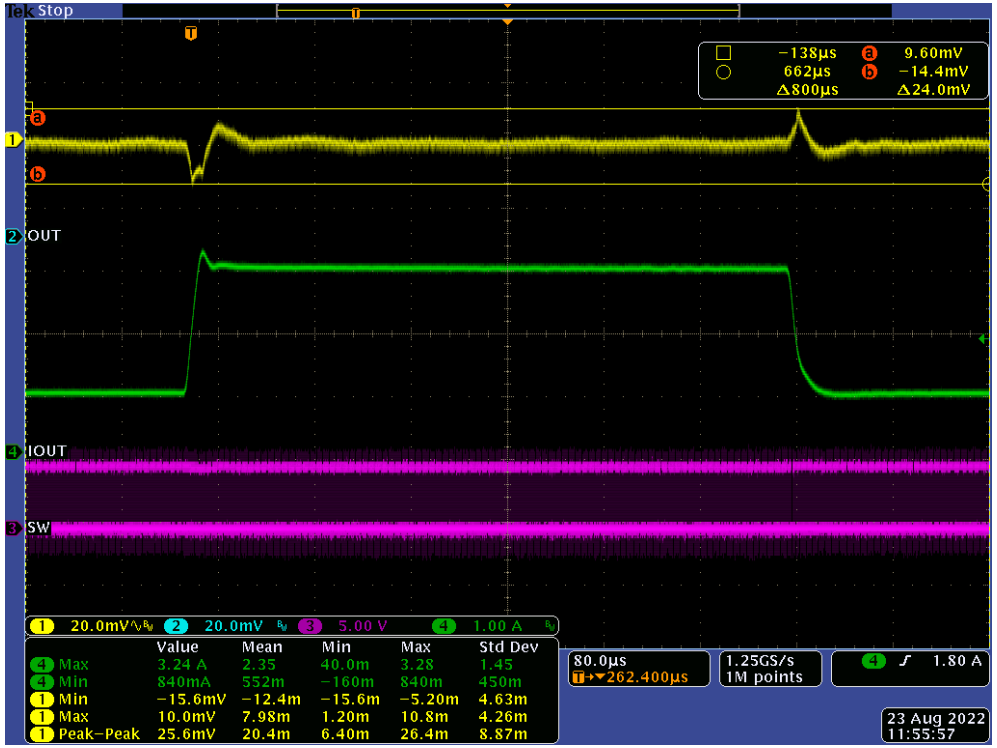
Max Load

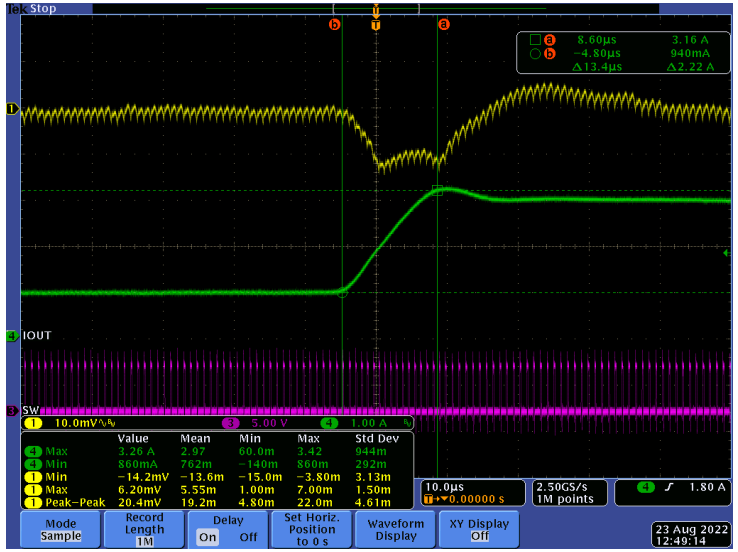


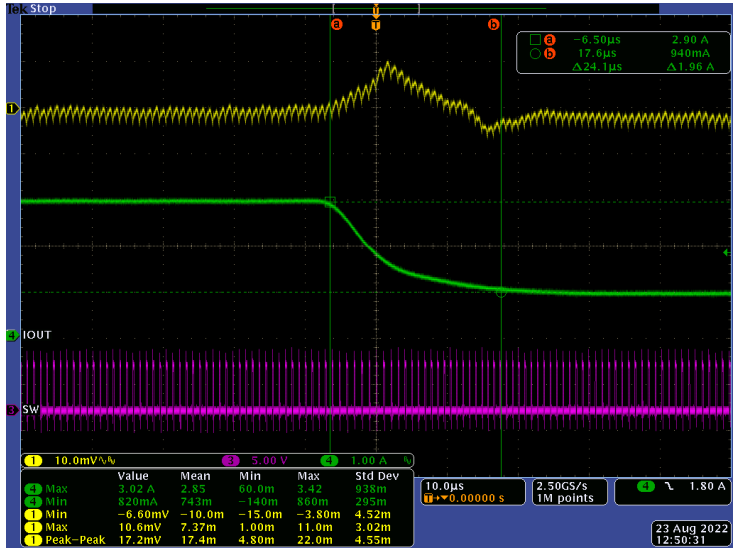
- ❑ 0.43% (3.7 mV) peak-peak ripple at Standby
- ❑ 0.46% (3.9 mV) peak-peak ripple at Half-Load
- ❑ 0.53% (4.5 mV) peak-peak ripple at Full-Load

MPM54524 VCCINT Transient

Step Load: 1A → 3A → 1A, 2.5A/us



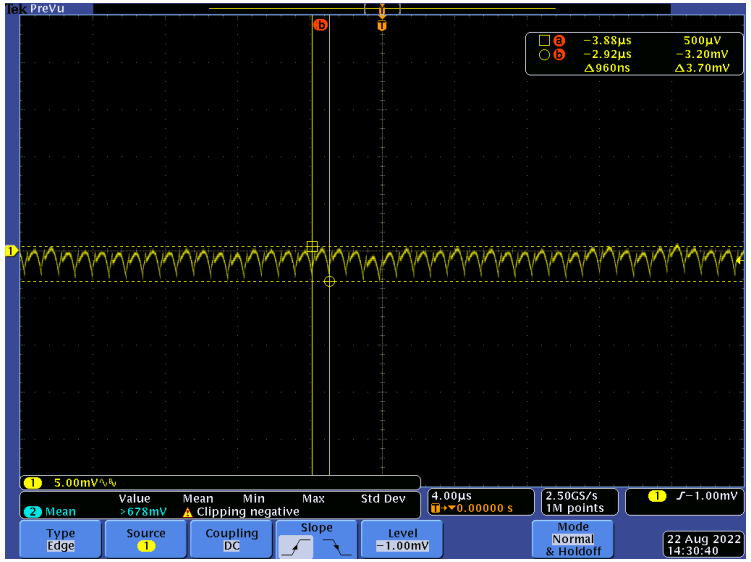




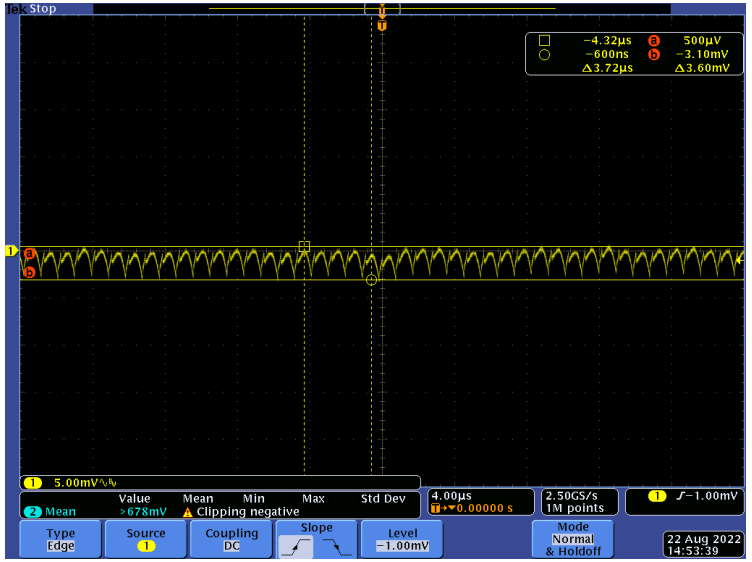
Vo ripple –1.84% (-15.6mV) to +1.17%(10mV) with load transient

MPM54524 VCCINT_IO Ripple

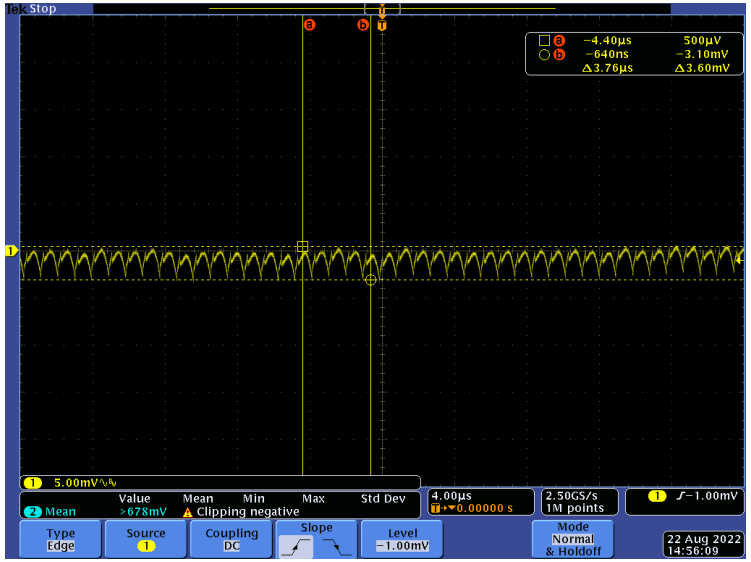
Standby



Half Load



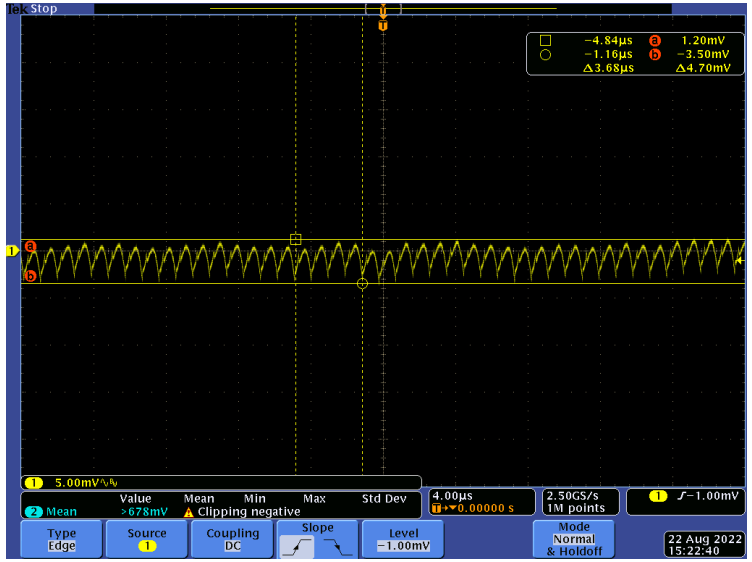
Max Load



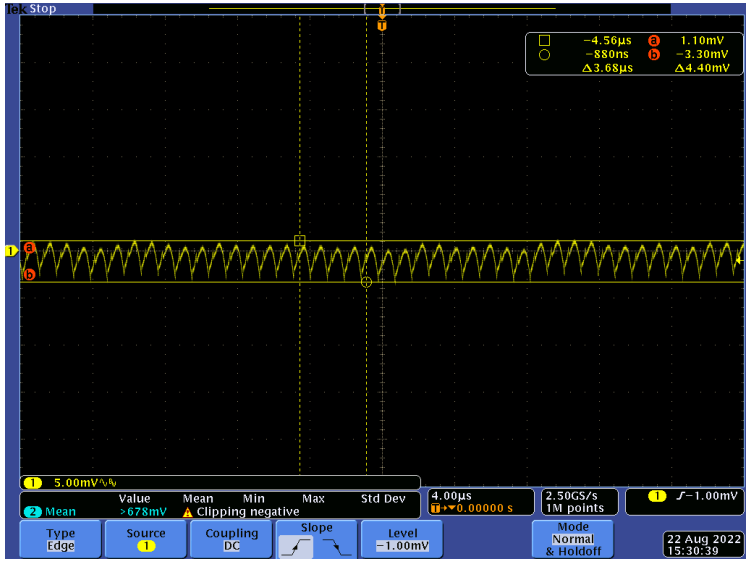
- 0.44% (3.7 mV) peak-peak ripple at Standby
- 0.42% (3.6 mV) peak-peak ripple at Half-Load
- 0.42% (3.6 mV) peak-peak ripple at Full-Load

MPM54524 VCCO_PSDDR4 Ripple

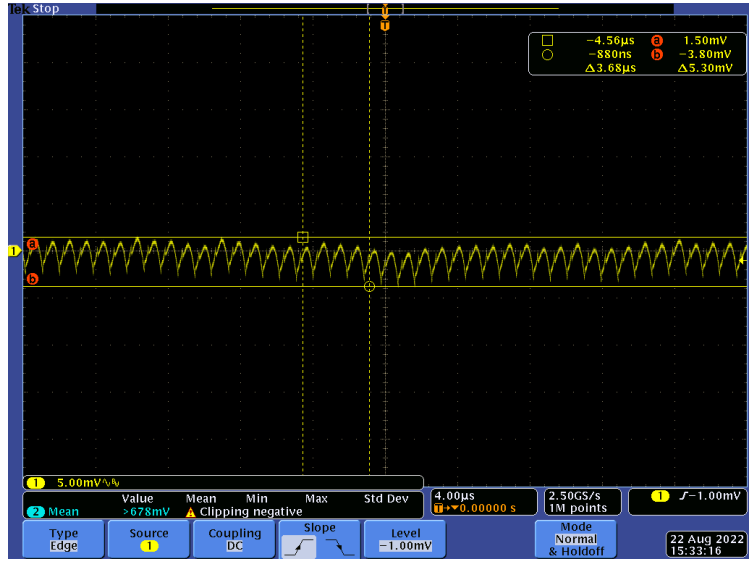
Standby



Half Load



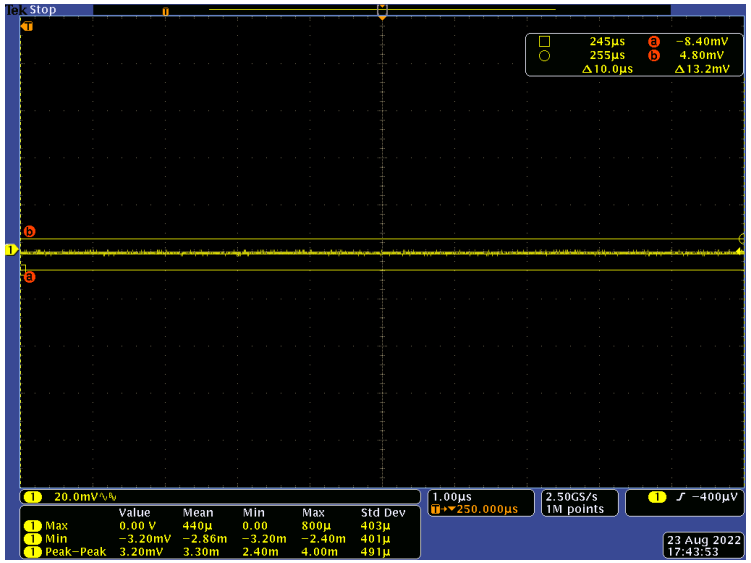
Max Load



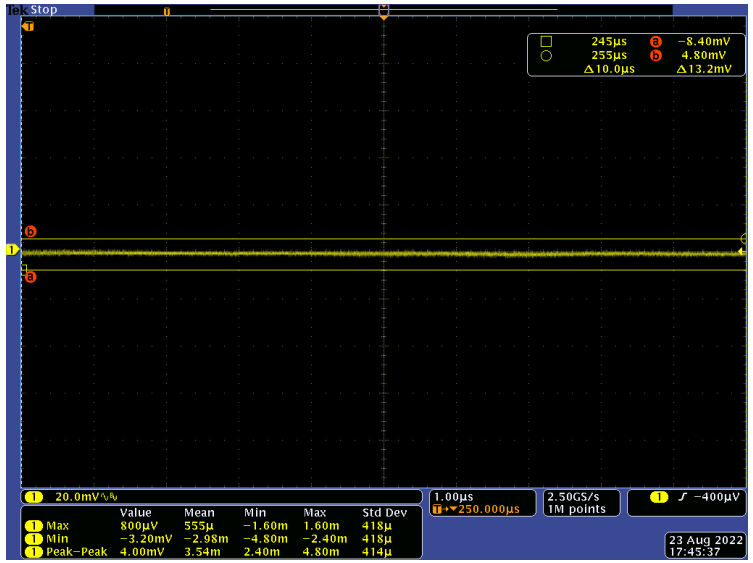
- 0.4% (4.7 mV) peak-peak ripple at Standby
- 0.37% (4.4 mV) peak-peak ripple at Half-Load
- 0.44% (5.3 mV) peak-peak ripple at Full-Load

MP2002A VCC_PSDDR_PLL Ripple

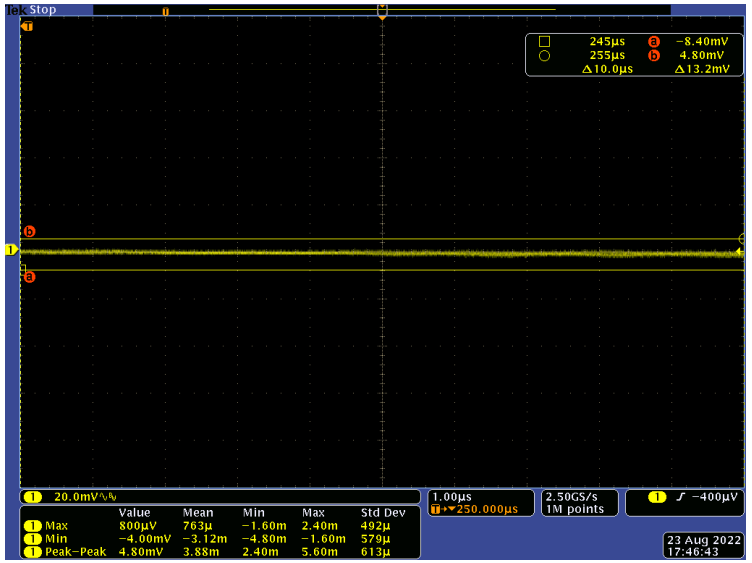
Standby



Half Load



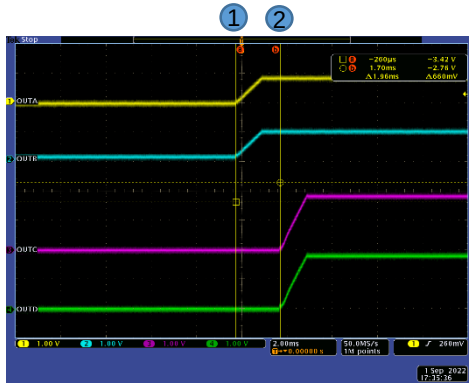
Max Load



- 0.18% (3.2 mV) peak-peak ripple at Standby
- 0.22% (4 mV) peak-peak ripple at Half-Load
- 0.27% (4.8 mV) peak-peak ripple at Full-Load

Power On Sequencing

MPM54524-0012



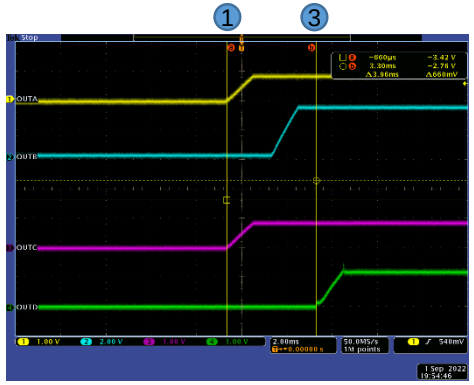
VCC_PSINTFP, VCC_PSINTFPDDR

VCC_PSINTLP

VCCAUX, VCCADC, VCCAUX_IO

VCCO_PSIO (0:3), VCCO_PSADC, VCC_PSAUX

MPM54524-0011



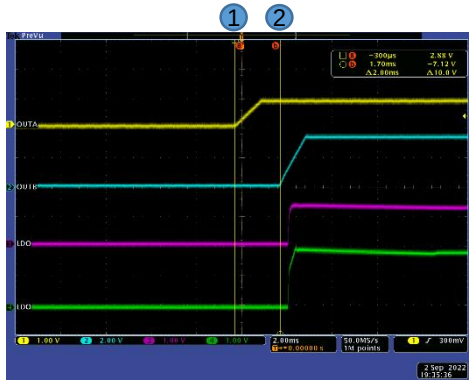
VCCINT

LDO, DDR, 3.3V Enet

VCCINT_IO, VCCBRAM

VCCO_PSDDR4_504

MPM54524-0011
+
MP2002A

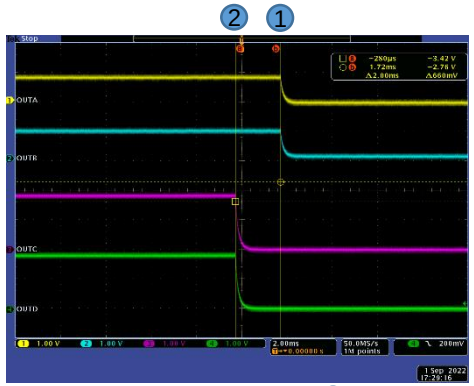


VCC_PSPLL

VCC_PSDDR_PLL

Power Off Sequencing

MPM54524-0012



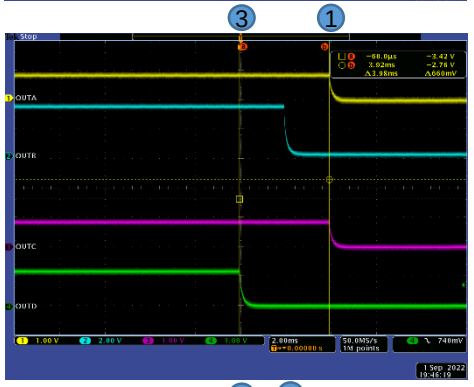
VCC_PSINTFP, VCC_PSINTFPDDR

VCC_PSINTLP

VCCAUX, VCCADC, VCCAUX_IO

VCCO_PSIO (0:3), VCCO_PSADC, VCC_PSAUX

MPM54524-0011



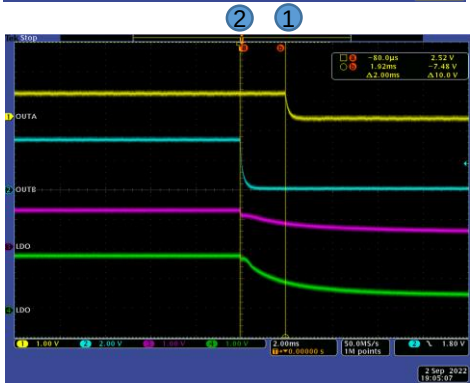
VCCINT

LDO, DDR, 3.3V Enet

VCCINT_IO, VCCBRAM

VCCO_PSDDR4_504

MPM54524-0011
+
MP2002A



VCC_PSPLL

VCC_PSDDR_PLL

MPM54524 Result Summary

Rails		Vo (V) No Load	Vo (V) Half Load	Vo (V) Full Load
VCC_PSINTFP	(0.85V/3.7A)	0.855	0.854	0.854
VCC_PSINTLP	(0.85V/0.6A)	0.855	0.855	0.855
VCCAUX	(1.80V/1.1A)	1.814	1.814	1.814
VCCO_PSIO	(1.80V/0.5A)	1.814	1.814	1.814
VCC_PSPLL	(1.20V/0.2A)	1.218	1.217	1.215
VCCINT	(0.85V/4.0A)	0.855	0.855	0.854
VCCINT_IO	(0.85V/0.6A)	0.855	0.854	0.854
VCCO_PSDDR4	(1.20V/1.2A)	1.201	1.201	1.201
VCC_PSDDR_PLL	(1.80V/0.5A)	1.809	1.805	1.80

MPM54524 Result Summary

Rails		Ripple No Load	Ripple Half Load	Ripple Full Load	Pwr ON Seq
VCC_PSINTFP	(0.85V/3.7A)	0.44% (3.7mV)	0.45% (3.8mV)	0.49% (4.2mV)	1 (0ms)
VCC_PSINTLP	(0.85V/0.6A)	0.44% (3.7mV)	0.42% (3.6mV)	0.42% (3.6mV)	1 (0ms)
VCCAUX	(1.80V/1.1A)	0.29% (5.2mV)	0.28% (5.1mV)	0.3% (5.4mV)	2 (1.96ms)
VCCO_PSIO	(1.80V/0.5A)	0.29% (5.2mV)	0.29% (5.3mV)	0.32% (5.8mV)	2 (1.96ms)
VCC_PSPLL	(1.20V/0.2A)	0.33% (4mV)	0.27% (3.2mV)	0.27% (3.2mV)	2 (2ms)
VCCINT	(0.85V/4.0A)	0.43% (3.7mV)	0.46% (3.9mV)	0.53% (4.5mV)	1 (0ms)
VCCINT_IO	(0.85V/0.6A)	0.44% (3.7mV)	0.42% (3.6mV)	0.42% (3.6mV)	2 (1.96ms)
VCCO_PSDDR4	(1.20V/1.2A)	0.4% (4.7mV)	0.37% (4.4mV)	0.44% (5.3mV)	3 (3.96ms)
VCC_PSDDR_PLL	(1.80V/0.5A)	0.18% (3.2mV)	0.22% (4mV)	0.27% (4.8mV)	2 (2ms)