# How Automotive Mission Profiles Relate to Semiconductor Reliability Testing

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September 30th, 2020

# Agenda

- What Is a Mission Profile?
- Stress to the Silicon
- IC Qualification
- Assessment of Existing and Qualified Components
- Fail Mech, Models, Acceleration Factor
- Equivalent Qualification Stress
- Equivalent Qualification Stress – Example
- Open Q&A

# What is a Mission Profile?

A Mission Profile is a mirror image of the expected life time of an application and the associated stress, which all used device will be submitted to.

It is needed to estimate if all used device will be reliable enough to maintain the specified product performance at least over the projected life time.

Most common is the Mission Profile that details the life time and associated use temperatures in form of a table.
Other MPs specify also mechanical stress or stress that comes along with humidity.

Operating Lifetime 15 years

| Profile 1 | | | |
|---|---|---|---|
| Active | | Passive | |
| Tj in °C | hours | Tj in °C | hours |
| -40 | 45 | -40 | 346 |
| 20 | 45 | 15 | 21168 |
| 40 | 855 | 25 | 42336 |
| 50 | 3150 | 35 | 21168 |
| 60 | 4950 | 40 | 1382 |
| 70 | 9000 | | 86400 |
| 80 | 11250 | | |
| 90 | 6750 | | |
| 100 | 4950 | | |
| 110 | 2700 | | |
| 120 | 1170 | | |
| 125 | 135 | | |
| | 45000 | | |
| | | | |
| Total hours | 131400 | | |

# Stress to the Silicon

What stress is it that the used devices will see during their life time?

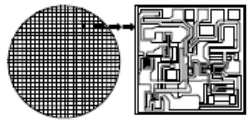
| | |
|---|---|
| Thermo-Mechanical : | the applications will be switched on/off and are used in winter and summer time etc. |
| Voltage- and Temperature: | Voltage (current) as well as temperature will cause aging effects to the silicon-junction |

The stresses will impact the material properties over life time and will (slowly) degrade the device performance. This can compromise the electrical performance as well as the mechanical performance.

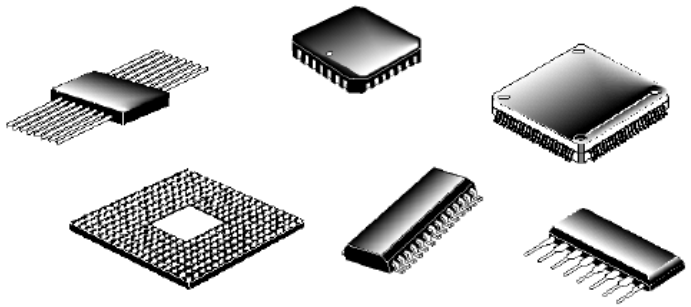
There are numerous standards that define certain qualification tests, which are designed to provoke certain reliability fail mechanisms. In semiconductors the most used standards are JEDEC and AEC.

# IC Qualification

AEC - Q100 - Rev-H
September 11, 2014



## FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR INTEGRATED CIRCUITS



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**Appendix Template 4A: AEC-Q100 Qualification Test Plan**

**Q100H QUALIFICATION TEST PLAN**

| | | | |
|---|---|---|---|
| USER COMPANY: | | DATE: | |
| USER P/N: | | TRACKING NUMBER: | |
| USER SPEC #: | | USER COMPONENT ENGINEER: | |
| SUPPLIER COMPANY: | | SUPPLIER MANUFACTURING SITES: | |
| SUPPLIER P/N: | | PPAP SUBMISSION DATE: | |
| SUPPLIER FAMILY TYPE: | | REASON FOR QUALIFICATION: | |

| STRESS TEST | ABV | TEST# | TEST METHOD | Test Conditions/S.S. per Lot/# Lots (identify temp, RH, & bias) | REQUIREMENTS S.S | REQUIREMENTS # LOTS | RESULTS Fails/S.S./# lots |
|---|---|---|---|---|---|---|---|
| Preconditioning | PC | A1 | JEDEC J-STD-020 | Peak Reflow Temp. = Preconditioning used = | Min. MSL = 3 | | MSL = |
| Temperature Humidity Bias or HAST | THB / HAST | A2 | JESD22-A101/A110 | | 77 | 3 | |
| Autoclave or Unbiased HAST | AC / UHST | A3 | JESD22-A102/A118 | | 77 | 3 | |
| Temperature Cycle | TC | A4 | JESD22-A104 | | 77 | 3 | |
| Power Temperature Cycling | PTC | A5 | JESD22-A105 | | 45 | 1 | |
| High Temperature Storage Life | HTSL | A6 | JESD22-A103 | | 45 | 1 | |
| High Temperature Operating Life | HTOL | B1 | JESD22-A108 | | 77 | 3 | |
| Early Life Failure Rate | ELFR | B2 | AEC Q100-008 | | 800 | 3 | |
| NVM Endurance, Data Retention, & Operational Life | EDR | B3 | AEC Q100-005 | | 77 | 3 | |
| Wire Bond Shear | WBS | C1 | AEC Q100-001 | | 5 | 1 | |
| Wire Bond Pull Strength | WBP | C2 | MIL-STD-883 - 2011 | | 5 | 1 | |
| Electrical Distributions | ED | E5 | AEC Q100-009 | | 30 | 3 | |
| Fault Grading | FG | E6 | AEC-Q100-007 | | | | |
| Characterization | CHAR | E7 | AEC Q003 | | | | |
| Electromagnetic Compatibility | EMC | E9 | SAE J1752/3 | | 1 | 1 | |
| Short Circuit Characterization | SC | E10 | AEC Q100-012 | | 10 | 3 | |
| Soft Error Rate | SER | E11 | JESD89-1, -2, -3 | | 3 | 1 | |
| Lead Free | LF | E12 | Q005 | | | | |
| Process Average Test | PAT | F1 | AEC Q001 | | | | |
| Statistical Bin/Yield Analysis | SBA | F2 | AEC Q002 | | | | |
| Hermetic Package Tests | MECH | G1-4 | Series | | 15 | 1 | |
| Package Drop | DROP | G5 | | | 5 | 1 | |
| Lid Torque | LT | G6 | MIL-STD-883 - 2024 | | 5 | 1 | |
| Die Shear Strength | DS | G7 | MIL-STD-883 - 2019 | | 5 | 1 | |
| Internal Water Vapor | IWV | G8 | MIL-STD-883 - 1018 | | 5 | 1 | |

Supplier: Approved by: (User Engineer)


| | | | |
|---|---|---|---|
| Temperature Cycle | TC | A4 | JESD22-A104 |
| Power Temperature Cycling | PTC | A5 | JESD22-A105 |
| High Temperature Storage Life | HTSL | A6 | JESD22-A103 |
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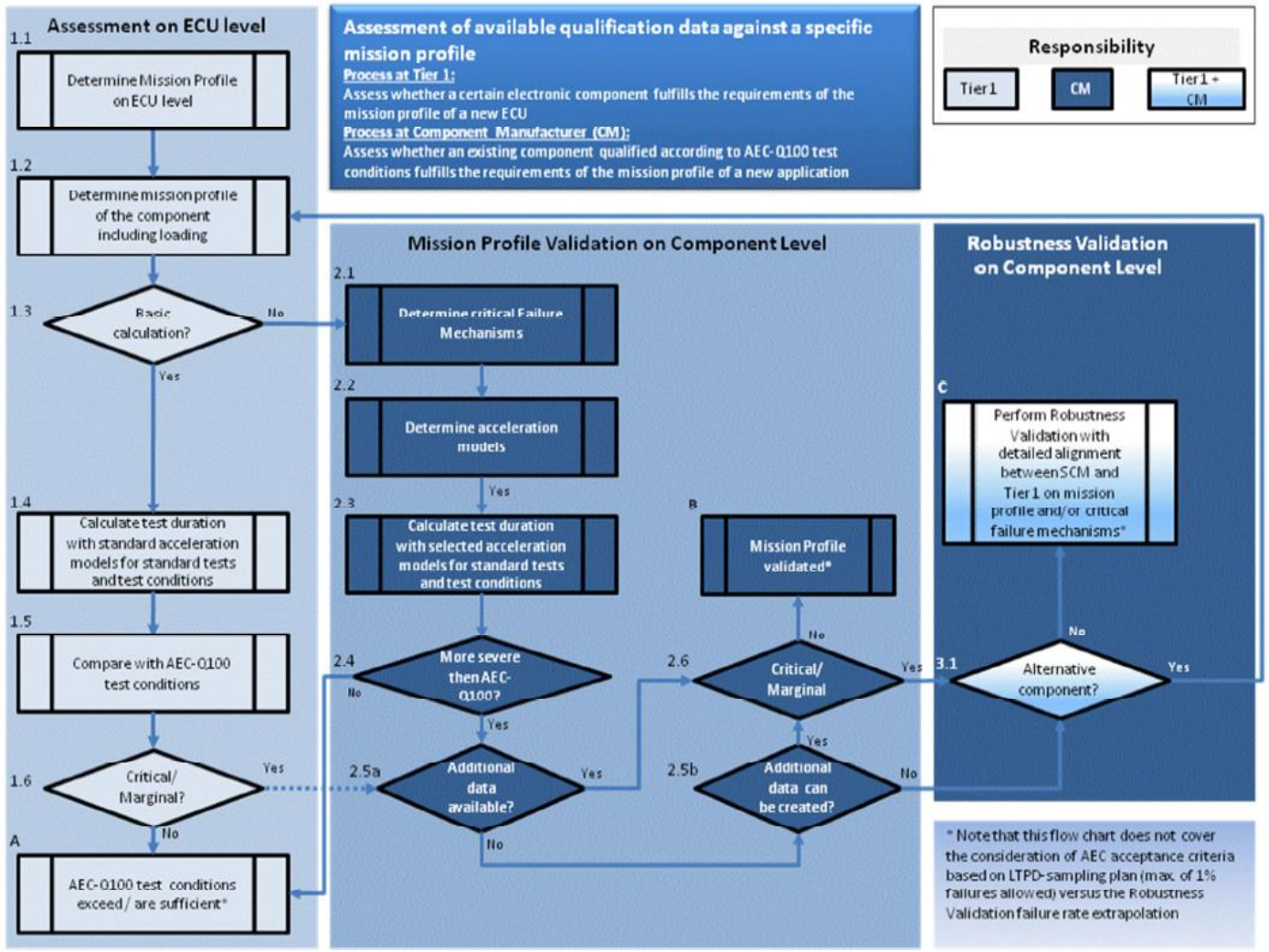
# Assessment of Existing and Qualified Components




**AECQ100, Rev H; Figure A7.2: Flow Chart 2**

AECQ100 defines that the Tier1 shall perform the assessment of the reliability capability on ECU level.

# Fail Mech, Models, Acceleration Factor

| Loading | Mission Profile Input | Stress Test | Stress Conditions | Acceleration Model (all temperatures in K, not in ℃) | Model Parameters | Calculated Test Duration | Q100 Test Duration |
|---|---|---|---|---|---|---|---|
| **Operation** | $t_u$ = 12,000 hr (average operating use time over 15 yr)<br><br>$T_u$ = 87℃ (average junction temperature in use environment) | High Temperature Operating Life (HTOL) | $T_t$ = 125℃ (junction temperature in test environment) | Arrhenius<br>$A_f = \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$<br><br>Also applicable for High Temperature Storage Life (HTSL) and NVM Endurance, Data Retention Bake, & Operational Life (EDR) | $E_a$ = 0.7 eV (activation energy; 0.7 eV is a typical value, actual values depend on failure mechanism and range from -0.2 to 1.4 eV)<br><br>$k_B$ = 8.61733 x $10^{-5}$ eV/K (Boltzmann's Constant) | $t_t$ = 1393 hr (test time)<br><br>$t_t = \frac{t_u}{A_f}$ | 1000 hr |
| **Thermo-mechanical** | $n_u$ = 54,750 cls (number of engine on/off cycles over 15 yr of use)<br><br>$\Delta T_u$ =76℃ (average thermal cycle temperature change in use environment) | Temperature Cycling (TC) | $\Delta T_t$ = 205℃ (thermal cycle temperature change in test environment: -55℃ to +150℃) | Coffin Manson<br>$A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$<br><br>Also applicable for Power Temperature Cycle (PTC) | m = 4 (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials) | $n_t$ =1034 cls (number of cycles in test)<br><br>$n_t = \frac{n_u}{A_f}$ | 1000 cls |

**AECQ100, Rev G; Table A7.1: Basic Calculations for AEC-Q100 Stress Test Conditions and Durations**

AECQ100 also to a loading of "Humidity", but this is typically not requested to us

# Equivalent Qualification Stress

In order to check if a certain device is suitable for a given MP, the stress of the MP must be translated into equivalent qualification stress.

Mission Profile Stress - > Equivalent Qual Stress > or < Qualification Stress

The associated acceleration models “Arrhenius” and/or “Coffin-Manson” provide the equations that needs be used.

# Equivalent Qualification Stress - Example

| Operating Lifetime 15 years | | | |
|---|---|---|---|
| **Profile 1** | | | |
| **Active** | | **Passive** | |
| **Tj in °C** | **hours** | **Tj in °C** | **hours** |
| -40 | 45 | -40 | 346 |
| 20 | 45 | 15 | 21168 |
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| | 45000 | | |
| | | | |
| Total hours | 131400 | | |

$$Af = \exp\left(\frac{Ea}{kb}\right) * \left(\frac{1}{273 - 40} - \frac{1}{273 + 125}\right)$$

$$Af = 4184927.76$$

$$tt = \frac{tu}{Af}$$

$$tt = \frac{45h}{4184927.76}$$

$$tt = 0.0000107h$$

Arrhenius

$$A_f = \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$$

This calculation needs to be done for every profile increment and the total equivalent test time is the sum of all tts.
For this Profile 1 the total equivalent test time is ~5888h.

The typical AECQ100 HTOL testing is only 1000h.
-> the MP stress exceeds the qual stress by factor ~6.
-> there is a certain risk that there will be device failures towards the end of the projected application life time.

# Equivalent Qualification Stress – Example  cont'd

How to address this?

- Either the actual Tj can be reduced in the application by implementing cooling/heat sink
- Extend the qualification by prolonging the test time and/or the increase the Tj

Using a qualification Tj of 150C the total equivalent test time would be  ~1767h.

With a test time of 1000h there would still be a little risk for device failures towards the end of the projected application life time.

If we additionally increased the test duration, say to 2000h, the qual stress would be significantly higher than the expected life time stress. This would provide a very high level of confidence that the device would not compromise operating performance or cause failures towards the end of the projected application life time.

# Thanks !