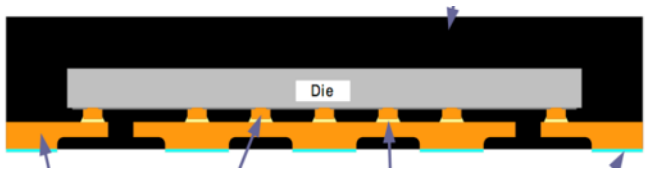
Fundamentals of AEC-Q100: What "Automotive Qualified" Really Means

Richard Oshiro,

Director, QMS-Automotive

November 2018

MPS Automotive Background



Flip-Chip Packaging Qualified

First Q100 Flip-Chip Part, MPQ4470

80 AEC Orderables

Automotive Spiked Out in Company Earnings, $53M

240+ AEC Products
200M Units Shipped

$120M+

2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020

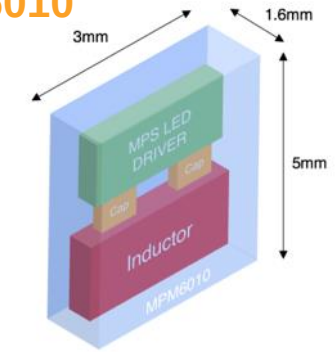
First Q100 Part, MPQ2451

AEC Participation

Automotive Electronics Council
Component Technical Committee

Automotive Hits $12M Annual Revenue

World's Most Compact LED Driver Module, MPM6010



First **Functional Safety** PMIC, MPQ7901
77GHz Radar for ADAS

ISO 26262

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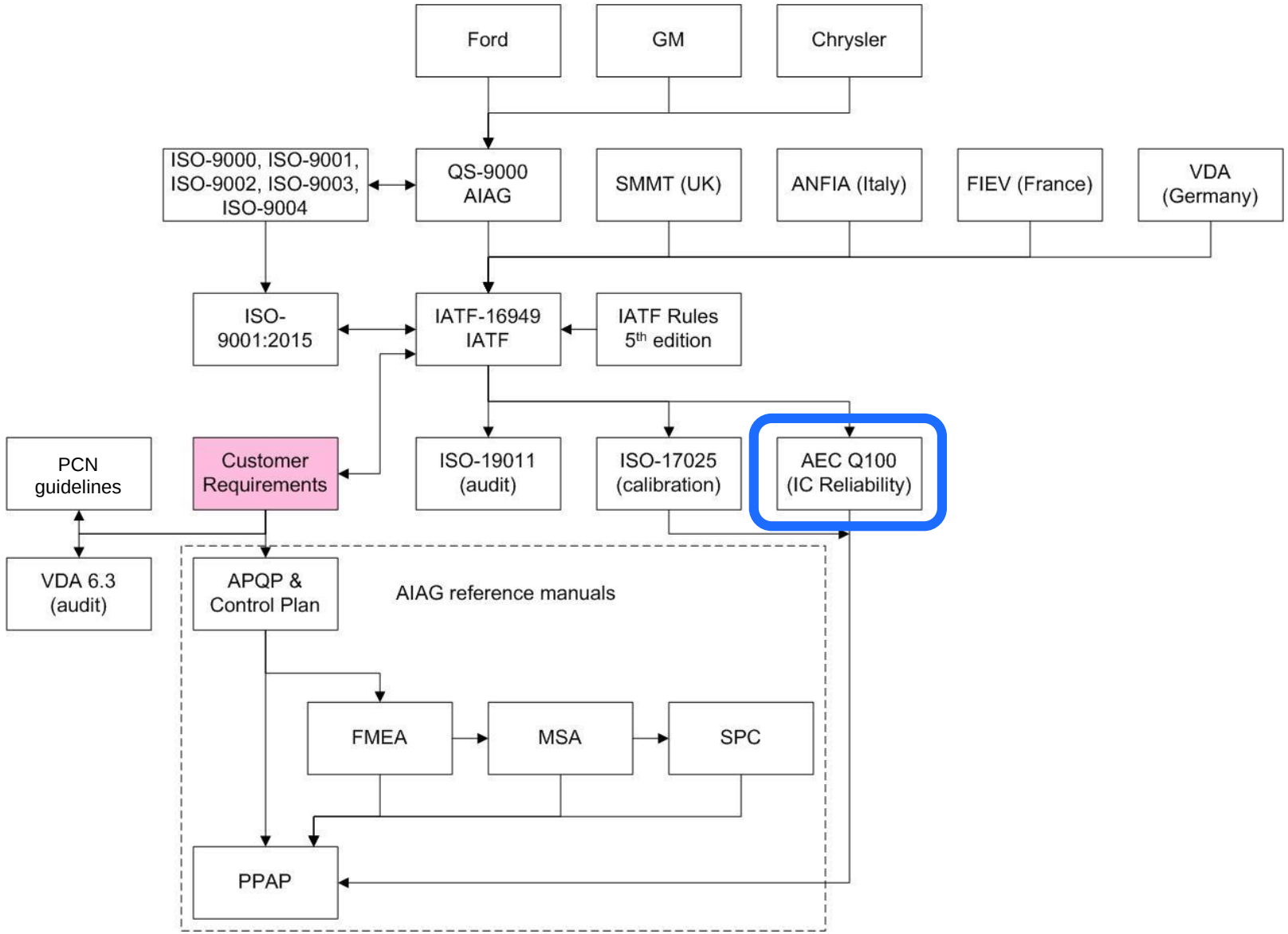
Richard Oshiro – Director, QMS, Automotive

- Nearly 20 years experience in Automotive Quality
- Currently responsible for MPS Automotive Quality as well as our Quality Management System. Representative for MPS on Automotive Electronics Council
- 11+ years as Director of Quality at Cypress Semiconductor with first task getting 2 internal fabs and 1 assembly test facility ISO/TS 16949 certified
- 5 ½ years as Director of Quality at a U.S. based assembly subcon where we assembled a Ford microelectronics component

Agenda

- The Who/What/Why's of AEC
- The Many AEC-Qxxx Standards
- AEC-Q100: Temperature Grades
- AEC-Q100: Key Reliability Tests
- Spotlight on HTOL, ELFR, PTC, TC, HAST
- Beyond AEC: STRM, Road Test, EVB BI
- MPS Consumer / Industrial / Automotive Grades Compared

Background: Automotive Ecosystem



Who is AEC?

Automotive Electronics Council
Component Technical Committee

Automotive Tier-1 Suppliers

Semiconductor Suppliers

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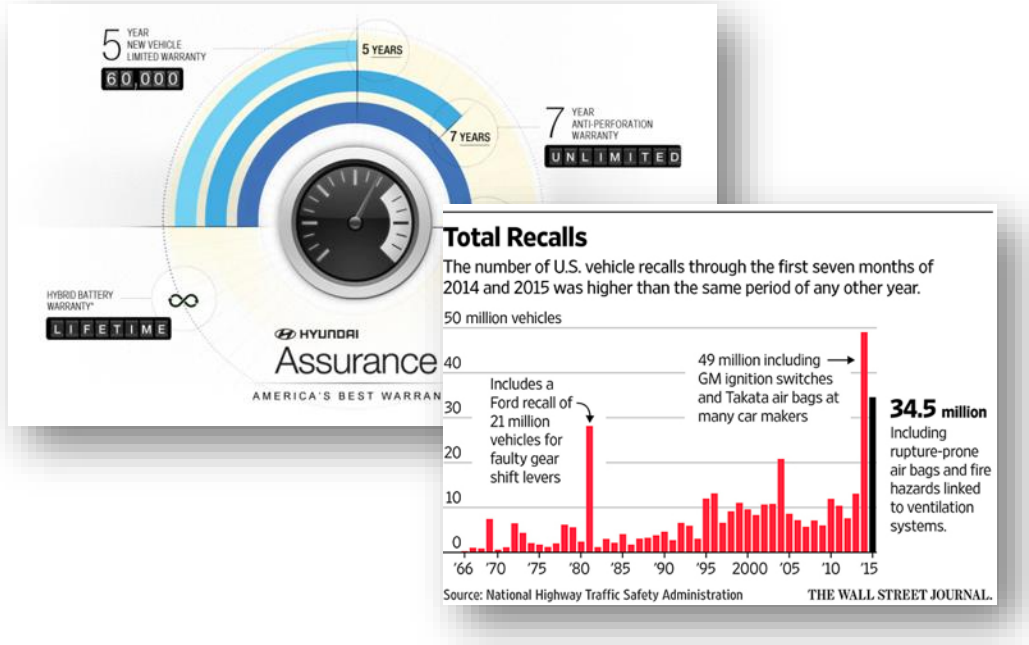
Automotive vs. Consumer

	Consumer	Automotive
Ambient Temperature Range	0° to 85°C	-40°C to 150°C
Expected Operating Life	2-3 years	10 years+
Acceptable Failure Rates	300 parts per million	Zero
Supply Lifetime	2-3 years	15-20 years

Why AEC-Q100 Qualification is Needed

Automotive companies sell millions of very expensive vehicles – to some people this means they think they can sue them for a lot of money

Automotive buyers have increased their quality requirements, partly due to automotive company's own advertisements



Example

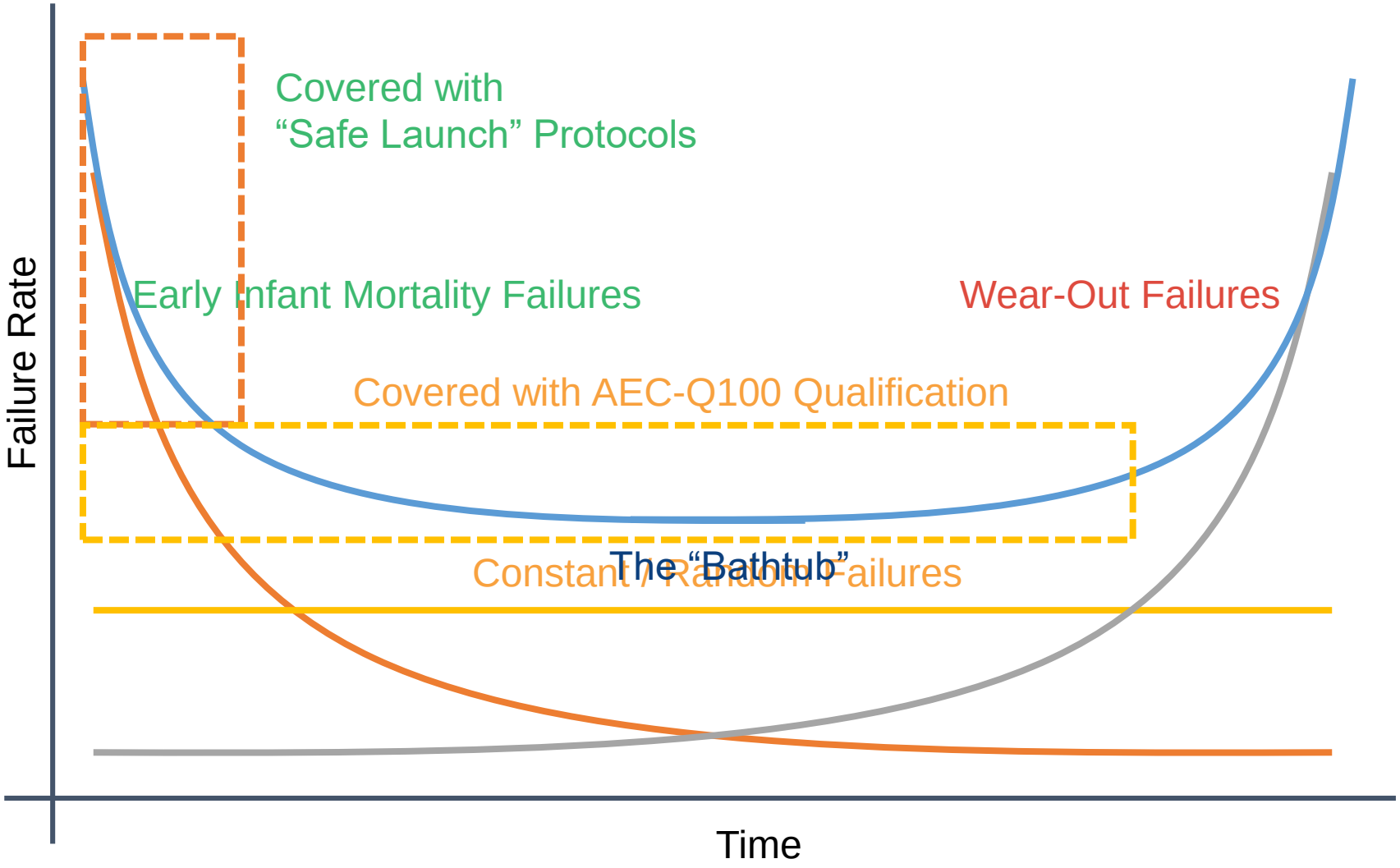
1000 defective cars

Single 1 ppm per part defect rate

1000 parts per ECU (IC, res, cap, etc)

1 Million cars sold

Reliability “Bathtub Curve”



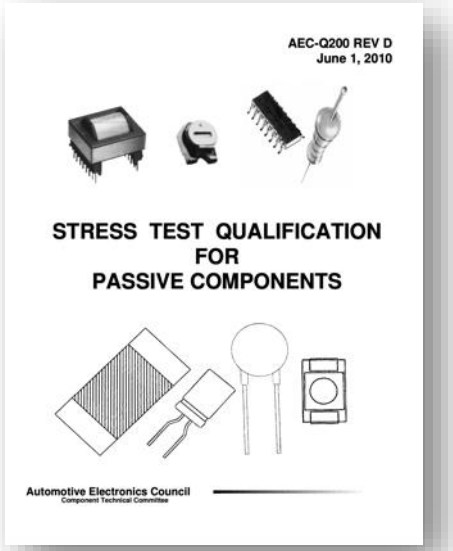
The Many AEC-Q Standards

AEC-Q100

AEC-Q101

AEC-Q102

AEC-Q200



AEC-Q104 (New)

Additional Standards

AEC - Q100-007 - Rev-B: Fault Simulation and Test Grading
AEC - Q100-008 - Rev-A: Early Life Failure Rate (ELFR)
AEC - Q100-009 - Rev-B: Electrical Distribution Assessment
AEC - Q100-010 - Rev-A: Solder Ball Shear Test
AEC - Q100-011 - Rev-C1: Charged Device Model (CDM) Electrostatic Discharge Test
AEC - Q100-001 - Rev-C: Wire Bond Shear Test
AEC - Q100-002 - Rev-E: Human Body Model (HBM) Electrostatic Discharge Test
AEC - Q100-004 - Rev-D: IC Latch-Up Test
AEC - Q100-005 - Rev-D1: Non-Volatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test
AEC - Q100-012 - Rev-: Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems

AEC - Q101 Rev - D1: Failure Mechanism Based Stress Test Qualification For Discrete Semiconductors (base document)
AEC - Q101-001 - Rev-A: Human Body Model (HBM) Electrostatic Discharge Test
AEC - Q101-003 - Rev-A: Wire Bond Shear Test
AEC - Q101-004 - Rev-: Miscellaneous Test Methods
AEC - Q101-005 - Rev-: Charged Device Model (CDM) Electrostatic Discharge Test
AEC - Q101-006 - Rev-: Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems
AEC - Q200 Rev - D base: Stress Test Qualification For Passive Components (base document)
AEC - Q200-001 - Rev-B: Flame Retardance Test
AEC - Q200-002 - Rev-B: Human Body Model (HBM) Electrostatic Discharge Test
AEC - Q200-003 - Rev-B: Beam Load (Break Strength) Test
AEC - Q200-004 - Rev-A: Measurement Procedures for Resettable Fuses …

AEC-Q100 Key Figures & Grades

3	Number of unique lots tested
77	Sample size per lot
1000h	Accelerated tests duration
1.67	Minimum CPK for distribution related parameters
0	Number of fails allowed

Ambient Temperature Range

Grade 3	-40° to 85°C
Grade 2	-40° to 105°C
Grade 1	-40° to 125°C
Grade 0	-40° to 150°C

AEC-Q100 Key Test Categories

- Accelerated Environment Stress
- Accelerate Lifetime Simulation
- Packaging/Assembly
- Die Fabrication
- Electrical Verification
- Defect Screening
- Cavity Package Integrity

AEC-Q100: Key Reliability Tests

Accelerated Environment Stress Tests

- Preconditioning
- Temperature-Humidity-Bias (THB) / Biased Highly Accelerated Stress Test (HAST)
- Autoclave (AC) / Unbiased (HAST)
- Temperature Cycling (TC)
- Powered Temperature Cycling (PTC)
- High Temperature Storage Life (HTSL)

Accelerate Lifetime Simulation Tests

- High Temperature Operating Life (HTOL)
- Early Life Failure Rate (ELFR)
- NVM Endurance, Data Retention, and Operational Life (EDR)

Packaging/Assembly

- Wire Bond Shear (WBS)
- Wire Bond Pull (WPL)
- Solderability (SD)
- Physical Dimensions (PD)
- Solder Ball Shear (SBS)
- Lead Integrity (LI)

Die Fabrication

- Electromigration (EM)
- Time Dependent Dielectric Breakdown (TDDB)
- Hot Carrier Injection (HCI)
- Negative Bias Temperature Instability (NBTI)
- Stress Migration (SM)

Electrical Verification

- Pre- and Post- Stress Function Parameter
- ESD – HBM/CDM
- Latch-Up
- Electrical Distributions
- Fault Grading
- Characterization
- Electromagnetic Compatibility (EMC)
- Short Circuit (SC)
- Soft Error Rate (SER)
- Lead (Pb) Free

Defect Screening

- Part Average Testing
- Statistical Bin/Yield Analysis

Package Integrity

HTOL vs. ELFR

Table 2: Qualification Test Methods (continued)

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
High Temperature Operating Life	**HTOL**	B1	H, P, B, D, G, K	77	3	0 Fails	JEDEC JESD22-A108	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +150ºC T_a for 1000 hours. **Grade 1:** +125ºC T_a for 1000 hours. **Grade 2:** +105ºC T_a for 1000 hours. **Grade 3:** +85ºC T_a for 1000 hours. HTOL NOTES: 1) HTOL stress times for the appropriate grade Ta are the min requirement; the Tj of the test (measured or calculated) should be available. 2) Tj may be used instead of Ta when performing HTOL provided that Tj of the device under HTOL conditions is equal to or higher than the Tj maximum operating (Tjopmax) of the particular device, but below the absolute maximum Tj. 3) If Tj is used to set the HTOL conditions, the minimum stress of 1000 hours at the Ta of the device is to be shown using activation energy of 0.7ev or other value technically justified. 4) V_{cc} (max) at which dc and ac parametrics are guaranteed. Thermal shut-down shall not occur during this test. **TEST before and after HTOL at room, cold, and hot temperature (in that order).**
Early Life Failure Rate	**ELFR**	B2	H, P, B, N, G	800	3	0 Fails	AEC Q100-008	Devices that pass this stress can be used to populate other stress tests. Generic data is applicable. **TEST before and after ELFR at room and hot temperature.**

- EVB based

PTC

Table 2: Qualification Test Methods (continued)

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (CONTINUED)								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Power Temperature Cycling	**PTC**	A5	H, P, B, D, G	45	1	0 Fails	JEDEC JESD22-A105	PC before PTC for surface mount devices. Test required only on devices with maximum rated power ≥ 1 watt or $\Delta T_J \geq$ 40°C or devices designed to drive inductive loads. **Grade 0:** T_a of -40°C to +150°C for 1000 cycles. **Grade 1:** T_a of -40°C to +125°C for 1000 cycles. **Grades 2 and 3:** T_a -40°C to +105°C for 1000 cycles. Thermal shut-down shall not occur during this test. **TEST before and after PTC at room and hot temperature.**

- EVB

TC

Table 2: Qualification Test Methods (continued)

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (CONTINUED)								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Temperature Cycling	**TC**	A4	H, P, B, D, G	77	3	0 Fails	JEDEC JESD22-A104 and Appendix 3	PC before TC for surface mount devices. **Grade 0:** -55ºC to +150ºC for 2000 cycles or equivalent. **Grade 1:** -55°C to +150°C for 1000 cycles or equivalent. **Note:** -65°C to 150°C for 500 cycles is also an allowed test condition due to legacy use with no known lifetime issues. **Grade 2:** -55ºC to +125ºC for 1000 cycles or equivalent. **Grade 3:** -55ºC to +125ºC for 500 cycles or equivalent. **TEST before and after TC at hot temperature.** After completion of TC, decap five devices from one lot and perform WBP (test #C2) on corner bonds (2 bonds per corner) and one mid-bond per side ***on each device***. Preferred decap procedure to minimize damage and chance of false data is shown in Appendix 3.

- Pre-conditioning first

HAST

Table 2: Qualification Test Methods

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Autoclave or Unbiased HAST or Temperature-Humidity (without Bias)	**AC or UHST or TH**	A3	P, B, D, G	77	3	0 Fails	JEDEC JESD22-A102, A118, or A101	For surface mount devices, PC before AC (121°C/15psig for 96 hours) or unbiased HAST (130°C/85%RH for 96 hours, or 110°C/85%RH for 264 hours). For packages sensitive to high temperatures and pressure (e.g., BGA), PC followed by TH (85°C/85%RH) for 1000 hours may be substituted. **TEST before and after AC, UHST, or TH at room temperature.**

- AC

Process/Design Change Impact on AEC-Q100

Table 2 Test #	A2	A3	A4	A5	A6	B1	B2	B3	C1	C2	C3	C4	C5	C6	D1	D2	D3	D4	D5	E2	E3	E4	E5	E7	E9	E10	E11	E12	G1-G4	G5	G6	G7	G8
Test Abbreviation	THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS	LI	EM	TDDB	HCI	NBTI	SM	HBM	CDM	LU	ED	CHAR	EMC	SC	SER	LF	MECH	DROP	LT	DS	IWV
DESIGN																																	
Active Element Design		●	●	M		●	●	DJ							D	D	D	D	D	●	●	●	●	●	●	●	●			F			
Circuit Rerouting			A	M																●	●	●	●	●	●	●							
Wafer Dimension / Thickness			E	M		●	●		E	E								●		E	E	E	●										
WAFER FAB																																	
Lithography	●		●	M		●	G		●	●								●					●										
Die Shrink	●	●		M		●	●	DJ							●	●	●	●	●	●	●	●	●	●	●	●	●						
Diffusion/Doping				M		●	G											●		●	●	●	●	●									
Polysilicon			●	M		●		DJ										●		●	●	●	●	●									
Metallization / Vias / Contacts	●	●	●	M		●			●	●					●				●				●	●		●							
Passivation / Oxide / Interlevel Dielectric	K	K	●	M		●	GN	DJ	K	●						●	●	●	●	●	●	●	●	●									
Backside Operation			●	M		●														M	M	●		●					H			H	
FAB Site Transfer	●	●	●	M		●	●	J	●	●					●	●	●	●	●	●	●	●	●						H			H	
ASSEMBLY																																	
Die Overcoat / Underfill	●	●	●	M	●	●																					●						H
Leadframe Plating	●	●	●	M	●					C	●			●														L				H	
Bump Material / Metal System	●	●	●	M	●	●						●	●														●	L					
Leadframe Material		●	●	M	●					●	●	●		●												●		L	H			H	
Leadframe Dimension		●	●	M							●	●		●												●		L	H				
Wire Bonding	●	●	●	Q	●				●	●													M			●			H				
Die Scribe/Separate	●	●	●	M																													
Die Preparation / Clean	●	●		M		●			●	●																						H	
Package Marking											B																						
Die Attach	●	●	●	M		●																	●			●		L	H			H	H
Molding Compound	●	●	●	M	●	●	●				●	●		●													●	L					
Molding Process	●	●	●	M	●	●					●	●		●														L					
Hermetic Sealing		H	H		H							H		H															H		H		H
New Package	●	●	●	M	●	●	●		●	●	●	●	T	●						●	●		●			●		L	H			H	H
Substrate / Interposer	●	●	●	M	●	●			●	●			T															L	H			H	H
Assembly Site Transfer	●	●	●	M		●	●		●	●	●	●	T	●									●					L	H			H	H

- ● Highly Recommended

A Only for peripheral routing
B For symbol rework, new cure time, temp
C If bond to leadfinger
D Design rule change
E Thickness only

F MEMS element only
G Only from non-100% burned-in parts
H Hermetic only
J EPROM or E^2PROM
K Passivation only

L For Pb-free devices only
M For devices requiring PTC
N Passivation and gate oxide
Q Wire diameter decrease
T For Solder Ball SMD only

FAQ About AEC-Q100 Qual

- Do all qualification tests have to be performed for every new device?
- How long is qualification data valid?

End Product: Qual Report in PPAP

Monolithic Power Systems, Inc.

1. Device Information

Product:	[redacted]
Package:	FCQFN2×3-14
Process Technology:	BCD
Report Date:	09/27/2018

2. Summary of Test Results

Test	#	Test Condition	Lot# or Date Code	Test Results (S.S./Rej)	Comment
Temperature, Bias, and Operating Life	B1	JESD22-A108, @+125°C for 1000 hours or equivalent	HP5431 HP543101 HP543108	77/0 77/0 77/0	
Early Life Failure Rate (ELFR)	B2	AEC-Q100-008, @ +125°C for 48 hours, or equivalent	HA5138 HA9134 H928211	800/0 800/0 800/0	
ESD: Human Body Model (HBM)	E2	AEC-Q100-002	HP543113	3/0	>2000V
ESD: Device Charged Model (CDM)	E3	AEC-Q100-011	HP543113	3/0	>750V
Latch-up	E4	AEC-Q100-004	HP543113	6/0	>+/-100mA & >1.5Vccmax
Moisture/Reflow Sensitivity	A1	J-STD-020	1731 1804 1808	276/0 276/0 276/0	MSL=1
Steady State Temperature Humidity Bias Life Test	A2	JESD22-A101, @85°C/85%RH static bias at Vinmax for 1000 hours or equivalent	1731 1804 1808	77/0 77/0 77/0	
Accelerated Moisture Resistance-Unbiased Autoclave	A3	JESD22-A102, @121°C/100%RH for 168 hours or equivalent	1731 1804 1808	77/0 77/0 77/0	
Temperature Cycling	A4	JESD22-A104, from -65°C to 150°C for 1000 cycles or equivalent	1731 1804 1808	77/0 77/0 77/0	

Production Part Approval Process

For

[redacted]

Customer Part Number

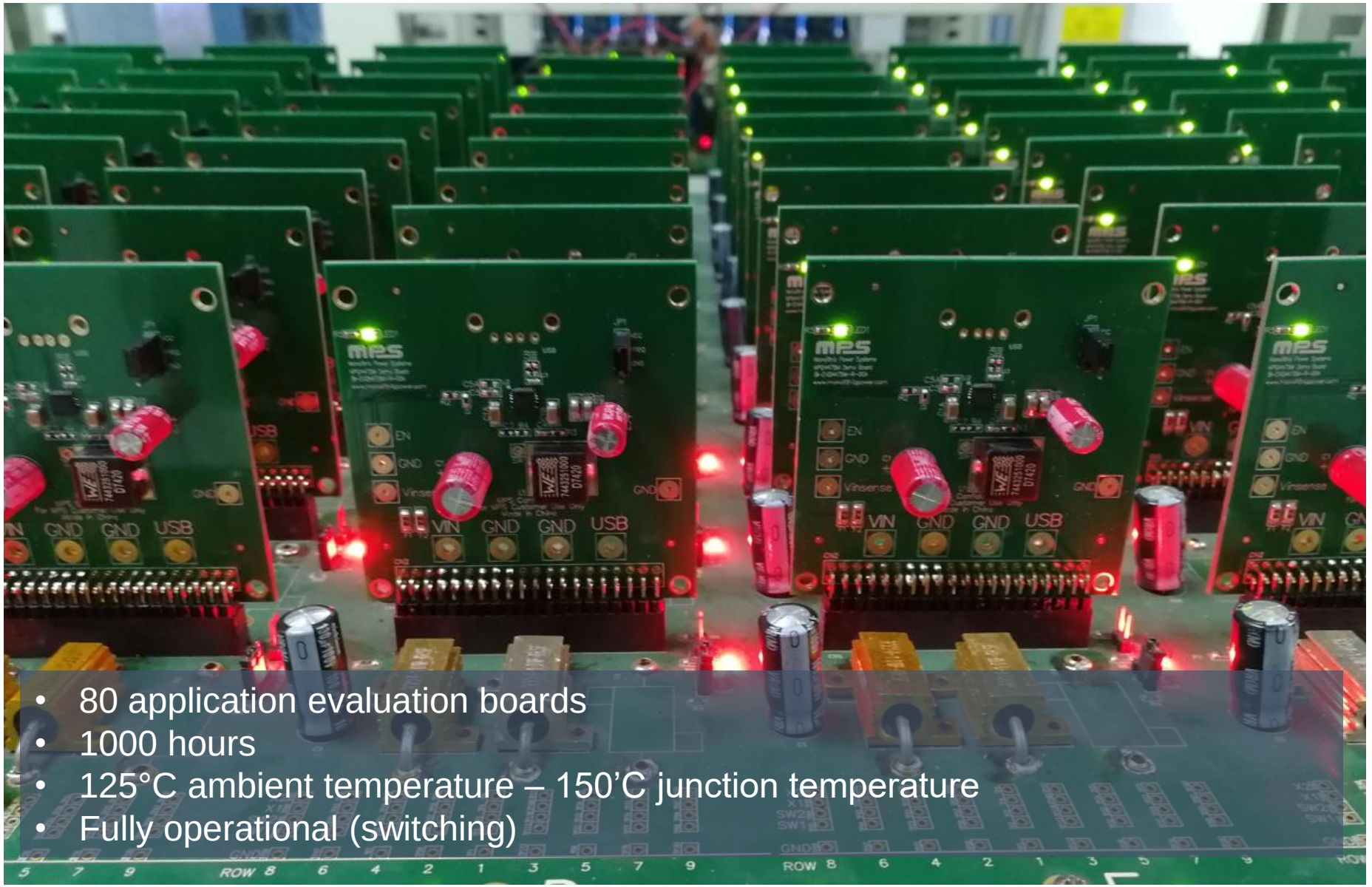
[redacted]

MPS Part Number

[redacted]

Revision: #1.0

Beyond Q100: EVB Burn-In



- 80 application evaluation boards
- 1000 hours
- 125°C ambient temperature – 150’C junction temperature
- Fully operational (switching)

Beyond Q100: Road Test & EMC

MPQ4572GL R2 Quick Road Test Report

2A, 60V, High-Efficiency SYNC Buck

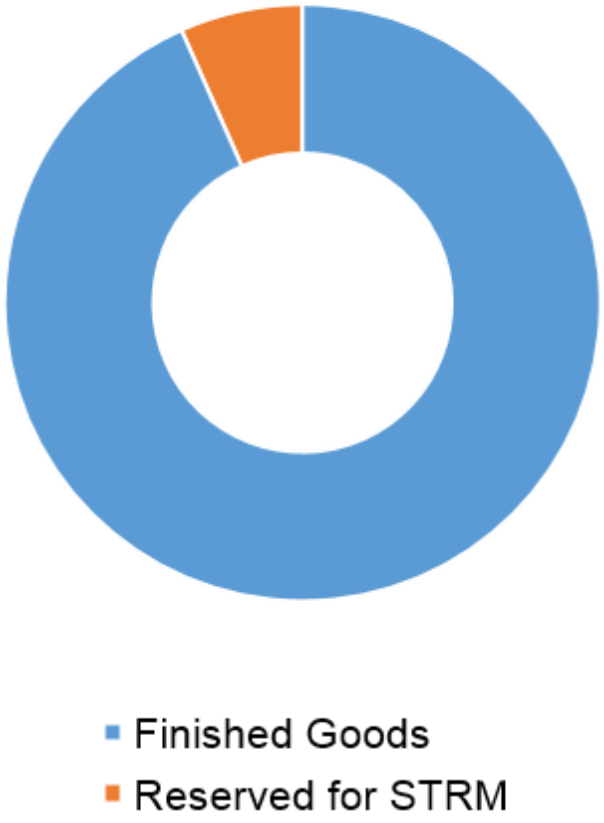
AE	Luke Wang
Supervisor	Huafei Ding
Manager	Zheng Luo
Date	2018-04-27

LOT:	Date code	IC Designer	Production Engineer
HP481815R2W20-C	1814	Surelly (Li) Xu	Lux Zhang

- 300-point application road test
- Grade 1: 25°C, -55°C, 150°C for margin
- Tests include stability/margin, ripple, fault response, load dump, cold crank
- CISPR25 radiated & conducted emissions testing

Beyond Q100: Short Term Reliability Monitoring

MPS "AEC1" Grade Production Lot



Short Term Reliability Monitoring Criteria

- Preconditioning (3x Reflow)
- 96-Cycle Temperature Cycling (-65° to 150°C)
- 48h Autoclave
- Final Test
- Lot Accepted

MPS Product Grades

		Consumer	Industrial	Automotive
Product Qual	Qualification Standard	JEDEC	JEDEC	AEC-Q100
	Tri-Temp Application Road Test	✓	✓	✓
Supply Chain	Dedicated Fab / Assembly		✓	✓
	Specialized Tools / Personnel			✓
Process	Enhanced Process Controls*		✓	
	Ultra-Enhanced Process Controls*			✓
Production	Test Lot Size Restriction		✓	✓
	ATE Test at Room Temp	✓	✓	✓
	ATE Test at Hot Temp			✓
	STRM & QA Sample Test		✓	✓
	PPAP			✓

*(SPC, Particle, PCM) & SBL/SYL

Thank You – Q&A

Additional resources:
http://www.aecouncil.com

For more information, contact:
automotive@monolithicpower.com

Check out our AEC-Q100 Power Management Solutions at **MonolithicPower.com**