

Designing a Power Tree for an Automotive SoC

Pre-Regulator Design

Webinar will begin at 10:00 AM CET | 1:00 AM PST | 4:00 AM EST

November 2022

Agenda

Introduction

Understanding the System-On-Chip (SoC) Power Requirements

Challenges for Automotive Batteries

Selecting the Right Pre-Regulator Architecture

Setting the Pre-Regulator Bus Voltage

How to Select the Optimal IC

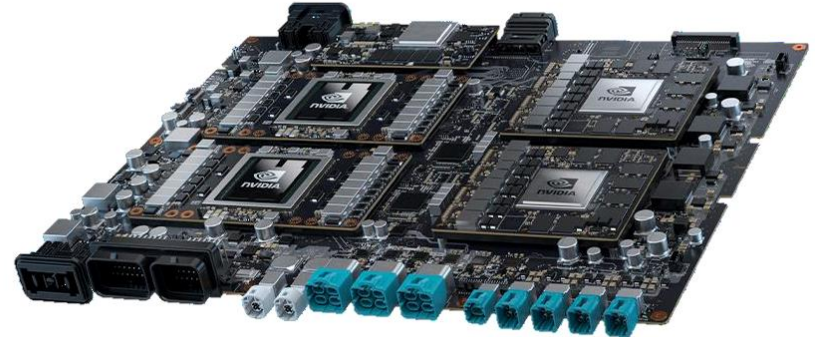
System Protections

Conclusion

Introduction

ADAS and infotainment system-on-chips (SoCs) are offering increasingly higher computing power to enable high-level autonomous driving and optimized user experience.

- ↑ Increased Power Consumption
- ↑ Demanding Converter Performance
- ↑ Higher Power Density



Autonomous drive platform

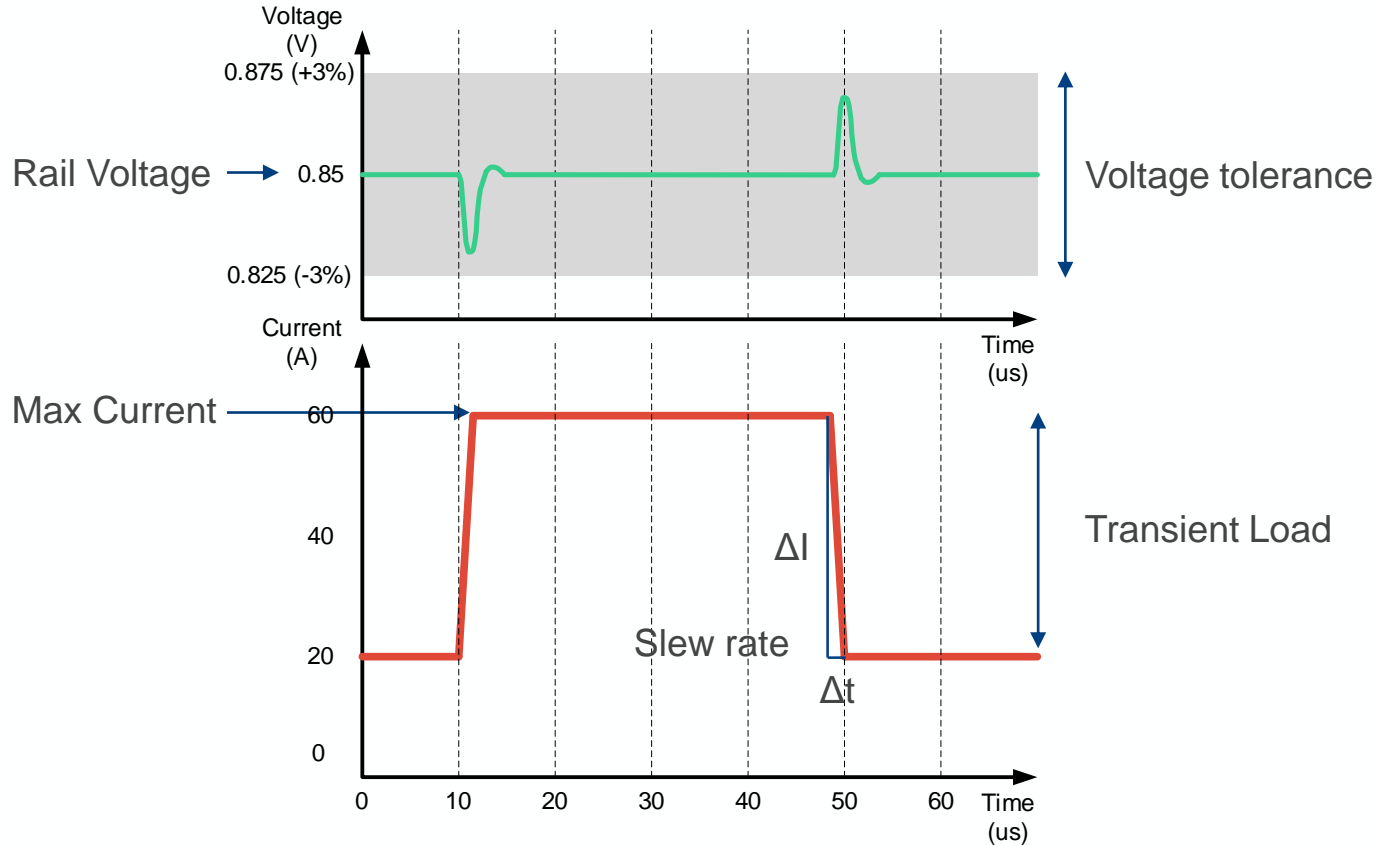
Understanding the SoC Power Requirements

A generic SoC's power requirements is shown below, including the required voltage for each rail, expected current peaks, load change magnitude, and the required accuracy.

Rail Name	Voltage (V)	Current (A)	Transient Load (A)	Slew Rate (A/ μ s)	Voltage Tolerance(%) *	Notes
VDD_CORE	0.85	60	40	40	3	
1V8_GPIO	1.8	5	2.5	2.5	5	
3V3_GPIO	3.3	5	2.5	2.5	5	
1V8_analog	1.8	1.5	0.75	0.75	5	From a low-noise DC/DC converter
DDR_VDD2	1.05	6	3	3	3	
DDR_VDDQ	0.6	6	3	3	5	
PCIe	0.85	1.5	0.75	0.75	5	From a low-noise DC/DC converter
MIPI	0.75	1.5	0.75	0.75	5	From a low-noise DC/DC converter

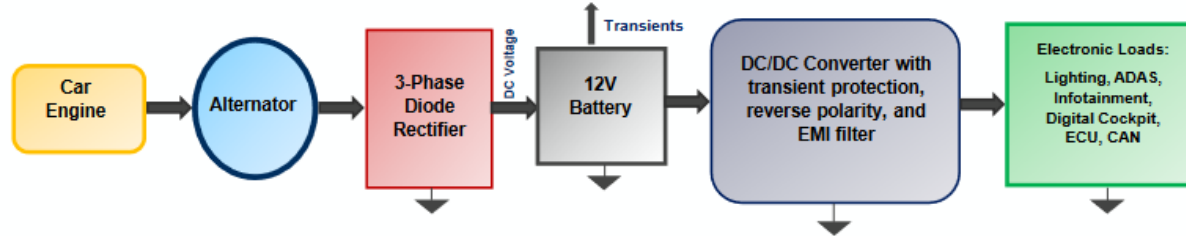
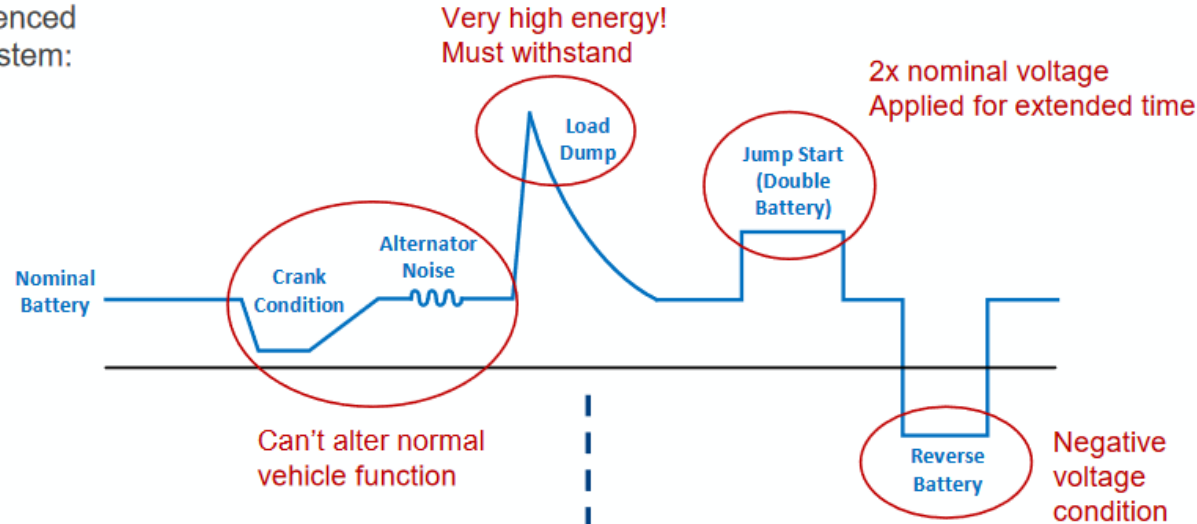
*The voltage tolerance includes the converter's DC accuracy, load transient response, and IR drop.

Understanding the SoC Power Requirements

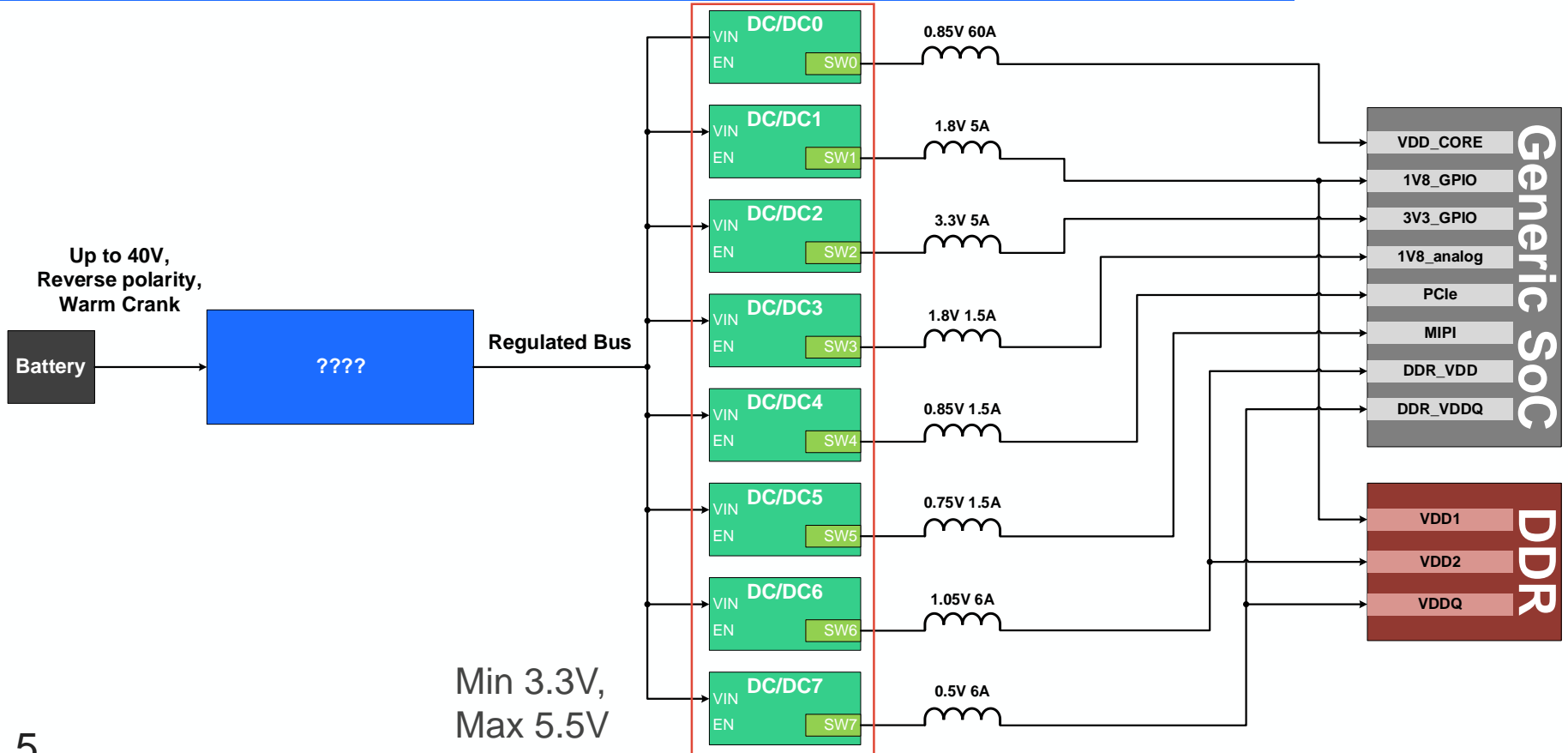


Challenges in Automotive Batteries

Transients experienced on 12V battery system:



Selecting the Right Architecture



Selecting the Right Architecture

The first step is to decide on a topology based on the system specifications:

System Specifications	Topology
Must operate during a warm-crank event	Buck converter
Must operate during a warm-crank event, and some circuits require a voltage exceeding 5V	Buck converter and downstream boost converter
Must operate during a cold-crank event	Buck-boost converter

The example circuit must operate during a warm-crank event, we select a buck converter since all rail voltages are below 5V.

Setting the Pre-Regulator Voltage

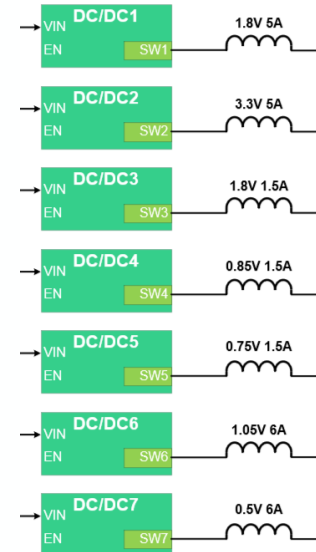
- The Intelli-phase converter for the high current rail (DC/DC0) requires $V_{IN} \geq 5V$

Recommended Operating Conditions ⁽³⁾

VDD5+4.5V to +5.5V

Operating Junction Temp (T_J)...-40°C to +150°C

- The other DC/DC (1 - 7) only require $V_{IN} \geq 3.3V$ because all rail voltages are $\leq 3.3V$



Setting the Pre-Regulator Voltage

To check if it makes sense to use a dedicated 3.3V bus for the lower current rails, calculate the power for regulator 2, and the output current in each case:

$$P_{\text{PRE-REG2}} = \frac{\sum_1^7 V_n \times I_n}{\eta} = \frac{1.8 \times 5 + 3.3 \times 5 + 1.8 \times 1.5 + 0.85 \times 1.5 + 0.75 \times 1.5 + 1.05 \times 6 + 0.6 \times 6}{0.89} = 45.5\text{W}$$

$$I_{\text{PRE-REG2_3.3V}} = \frac{P}{V} = \frac{45.5}{3.3} = 13.8\text{A}$$

$$I_{\text{PRE-REG2_5V}} = \frac{P}{V} = \frac{45.5}{5} = 9.1\text{A}$$

The output current of the 3.3V bus voltage exceeds the output current of the 5V bus voltage by 50%.

Using a 5V bus is preferred

Setting the Pre-Regulator Voltage

Should the 5V bus be consolidated into a single converter?

$$P_{\text{PRE-REG1}} = \frac{V \times I}{\eta} = \frac{0.85 \times 60}{0.89} = 57.3\text{W}$$

$$P_{\text{PRE-REG2}} = 45.5\text{W}$$

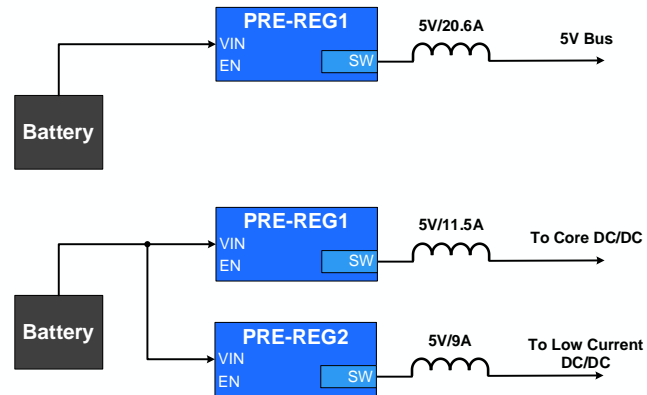
$$P_{\text{PRE-REG}} = 102.8\text{W}$$

$$I_{\text{PRE-REG}} = 20.58\text{A}$$

If separated:

$$I_{\text{PRE-REG1}} = 11.5\text{A}$$

$$I_{\text{PRE-REG2}} = 9.1\text{A}$$



It is easier to handle two low-current buses than a single 20A bus.

How to Select the Optimal IC

COMPILED REQUIREMENTS

- Tolerate load dump up to 40V
- Operate in warm-crank down to 6V
- Output current capability above 11.5A

SHOW COLUMNS	Status	MPS Inventory	Vin (min) [V]	Vin (max) [V]	Iout (max) [A]	Iq (typ) [mA]	Vfb [V]	fsw (max) [kHz]	Common Features	Special Features	Control Mode	Package (mm)
Part Number	MPSafe	BUY ON MPS	6.02	58.82	11.99	520	2.55	4000	<input type="checkbox"/> Soft Start <input type="checkbox"/> Synchronous <input type="checkbox"/> Synchronous Buck <input type="checkbox"/> Synchronous Mode <input type="checkbox"/> Synchronous Rectification <input type="checkbox"/> Wettable Flank QFN Option	<input type="checkbox"/> Multi-Page One-Time Programmable (MOTP) Memory <input checked="" type="checkbox"/> Multi-Phase Capability <input type="checkbox"/> OCP <input type="checkbox"/> OCP with Hiccup Mode <input type="checkbox"/> Output Current Limit	<input type="checkbox"/> Current Mode <input type="checkbox"/> COT Control <input type="checkbox"/> Hysteretic <input type="checkbox"/> Peak-Current Mode	<input type="checkbox"/> QFN-6L <input type="checkbox"/> QFN-8 (1.5x2) <input type="checkbox"/> QFN-8 (3x3) <input type="checkbox"/> QFN-10 (3x3) <input type="checkbox"/> QFN-11 (2x3) <input type="checkbox"/> QFN-12 (2x3)

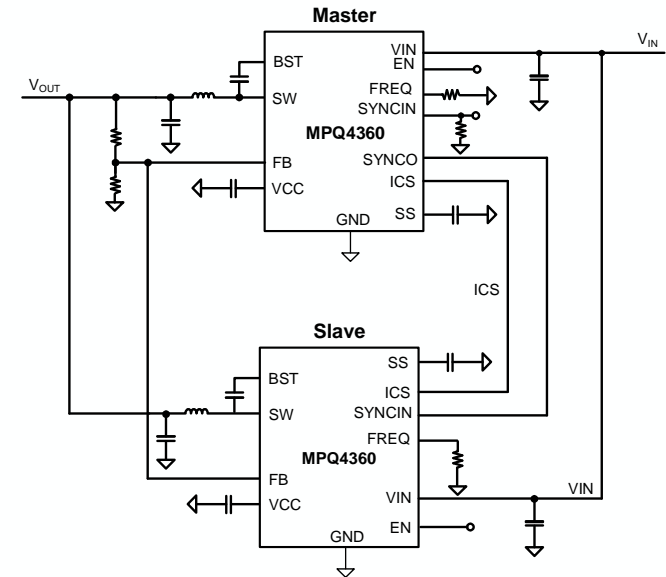
When applying filters to the product catalog, no single part is capable of 11.5A. However, two MPQ4360 devices can be paralleled to achieve a 12A output.

<https://www.monolithicpower.com/en/products/automotive-aecq-grade/switching-converters-and-controllers-aecq-grade.html>

MPQ4360-AEC1 Overview

FEATURES

- Wide 3.3V to 45V Input Voltage (V_{IN}) Range
- 6A Output Current (I_{OUT}) with Multi-Phase Capability
- Low I_Q (10 μ A Sleep Mode, 1 μ A Shutdown Mode)
- Configurable Switching Frequency (f_{SW}) or External Clock Sync
- Output Clock with 180° Phase Shift
- Optional 3.3V, 3.8V, and 5V Fixed Outputs
- Symmetric V_{IN} Layout for Improved EMI
- Selectable AAM Mode or FCCM
- Power Good (PG)
- External Soft Start (SS)
- Low-Dropout Mode (LDO)
- Over-Current Protection (OCP) in Hiccup Mode
- Available in a QFN-20 (4mmx4mm) Package with Wettable Flanks



Available in a QFN-20 (4mmx4mm) Package

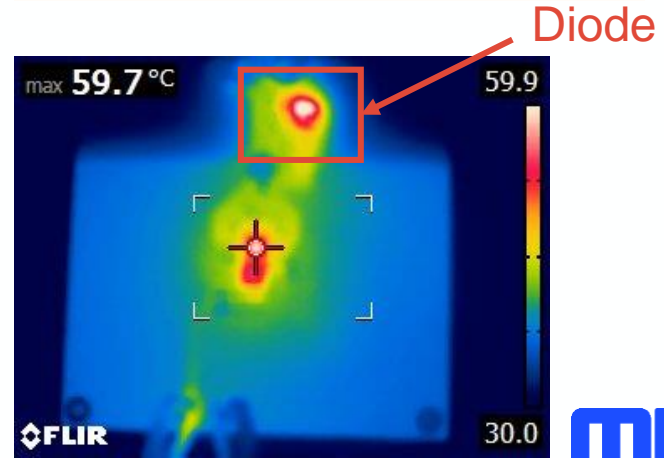
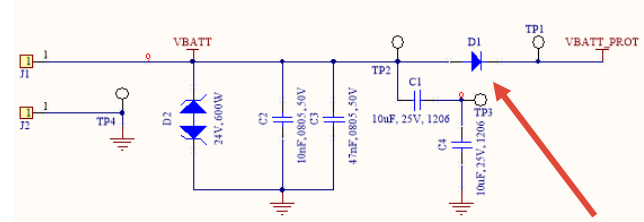
Key Specs

V_{IN}	3.3V to 45V
I_{OUT}	6A
f_{SW}	350kHz to 2.2MHz
HS-FET/LS-FET $R_{DS(ON)}$	40m Ω /17m Ω
Package	QFN-20 (4mmx4mm)

System Protection

The MPQ4360 Pre-regulator can protect the systems against load dump voltage, but can be damaged when the battery polarity is reversed.

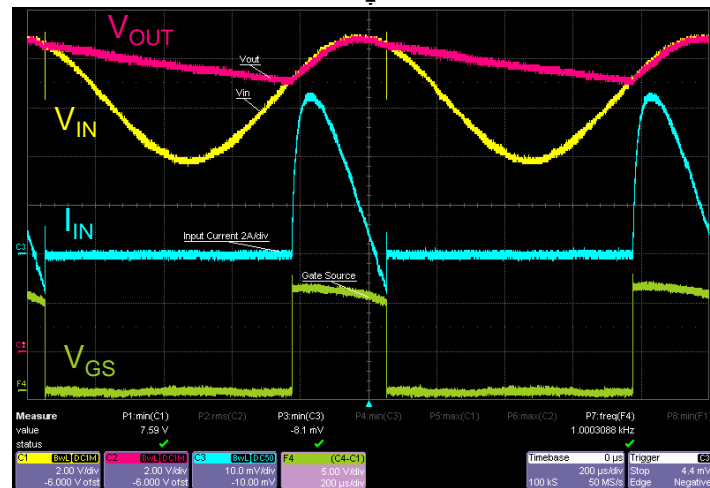
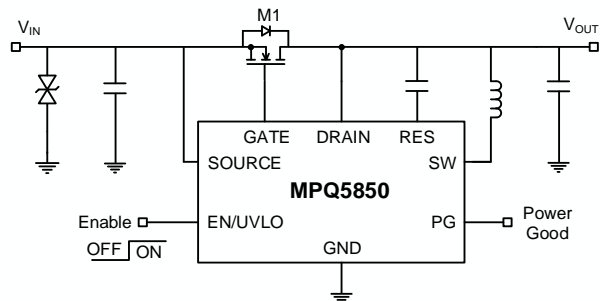
- The typical protection is placing a diode in series with the input line.
- In this SoC system, the input current can exceed 8A, which causes a very high dissipation on the diode. At 8A, the power loss on a Schottky diode is about 2.5W.
- A P-Channel MOSFET circuit can address the negative DC polarity, but it is too slow to rectify any superposed AC voltage on the input line



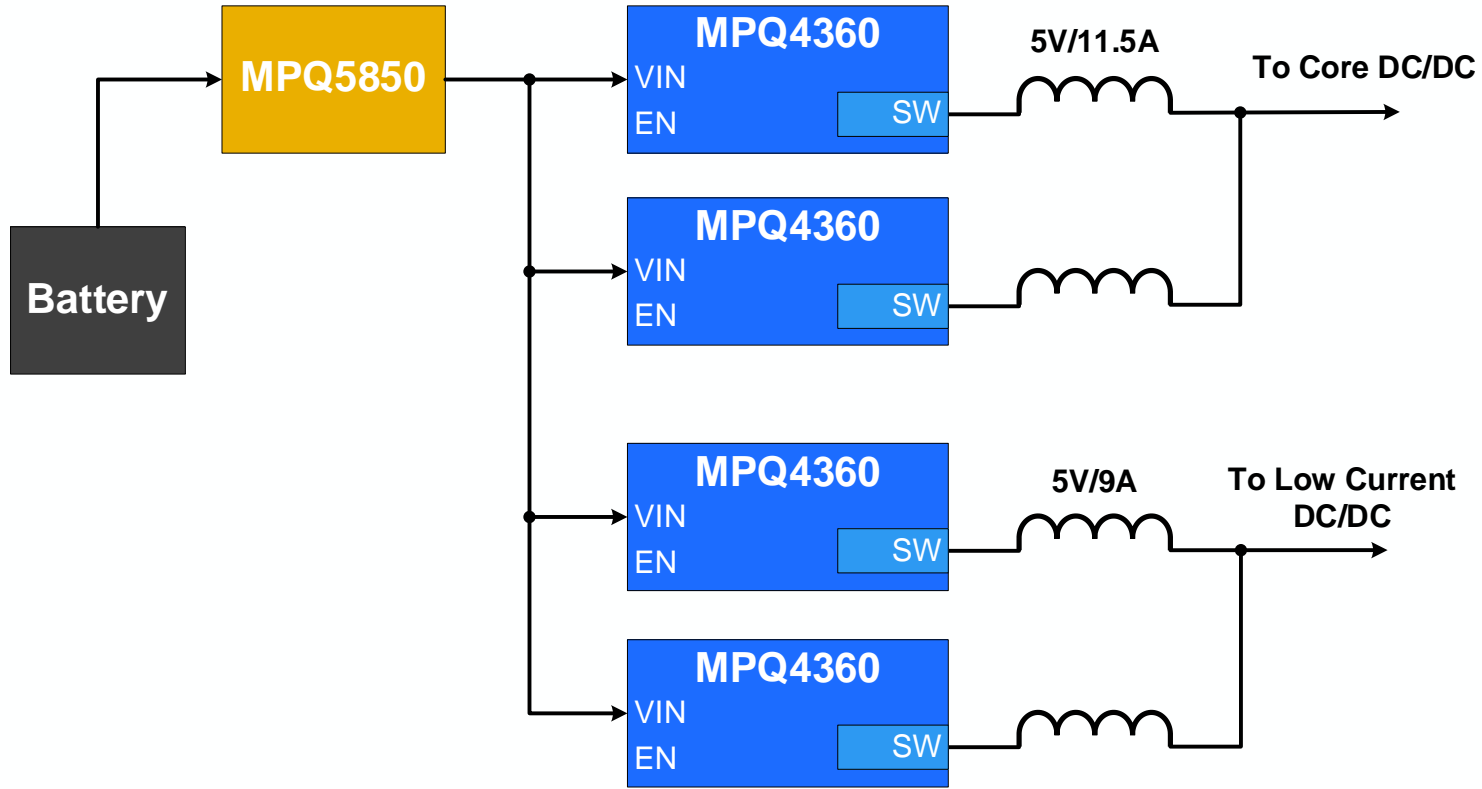
MPQ5850-AEC1 Overview

The MPQ5850-AEC1 is an ideal diode controller that uses an N-channel MOSFET emulating a diode.

- During forward conduction the FET is fully turned on to minimize the power loss.
- In the event of negative currents, the controller will quickly turn the FET off to block the reverse current and protect the circuitry.
- An integrated boost converter is used to generate the gate voltage.



Conclusions



Conclusions

There are 3 main topics to consider when designing the pre-regulator for an SoC:

- Select an IC that can operate correctly under all automotive battery conditions
- A 5V bus voltage is typically more cost-effective, but can be inadequate for certain applications
- When the input current is high, an ideal diode controller is the most efficient way to protect the system

Q&A

Let us know your questions.