Optimize Switch-Mode Power Modules to Achieve Ultra-Low (μV) Ripple and Noise

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Background

- The growing bandwidth of wireless networks and data centers demand for **power regulators** with **high power density**, **fast load transient response**, and **high efficiency**.
- High-performance RF data converters, e.g. Xilinx Zynq UltraScale+ RFSoCs which provides a comprehensive RF signal chain, are necessary for wireless applications.
- The **performance of the RF data converters** is closely coupled with the **noise level** of their power supplies. LDO is widely selected due to its low noise.
- **Switching regulator has much higher efficiency than LDO**. This paper designs a passive output filter for switching regulator, which can meet the **low noise (uV)** requirement.

Output Voltage Ripple with Forced CCM Operation

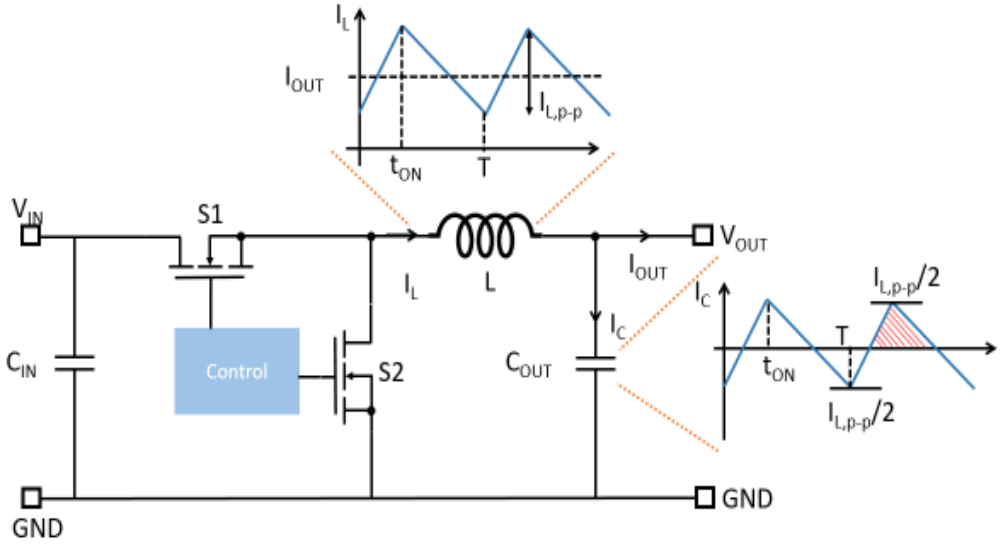


Figure 1. Low Noise Filter Design

- An **ultra-small and ultra-low noise** power module, MPM3833C, is used as a design example. It features forced **CCM** operation, which brings low ripple at light load.

Why use second stage inductive filter?

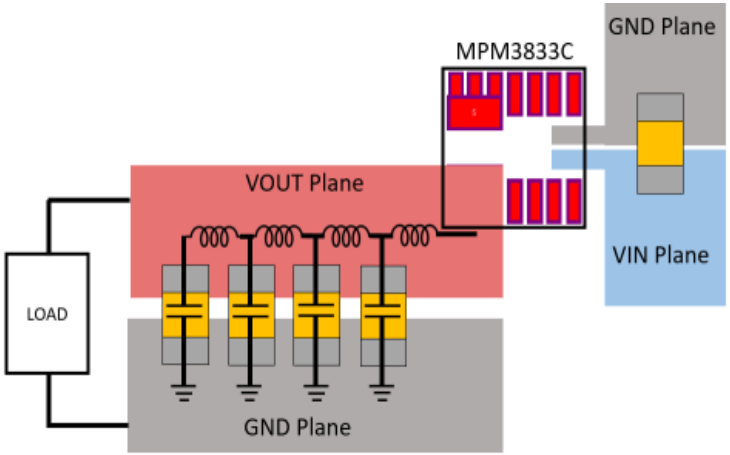
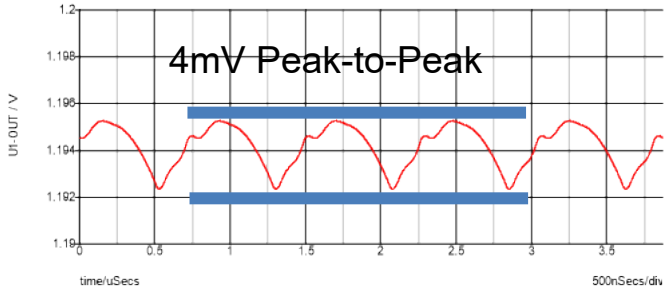


Figure 2. Typical PCB Layout for the MPM3833C Power Module

- As more capacitors are placed on the output plane, the distance from the additional capacitor to the output pin of the power module increases.
- Consequently, more **parasitic inductance** is involved in the output capacitor that is farther away from the power module.

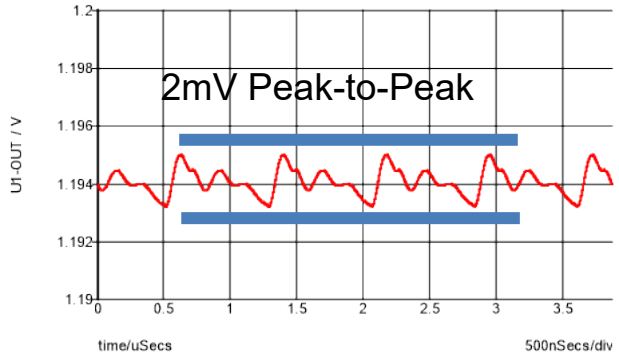
Why use second stage inductive filter?

Output voltage ripple with one 22uF output capacitor



- Additional output capacitor becomes less effective

4x22uF output capacitor



5x22uF output capacitor

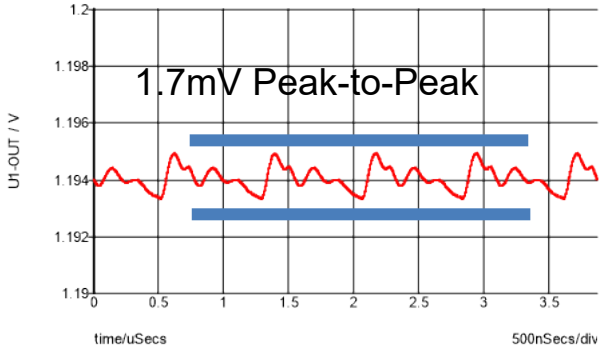


Fig. 3 Output Voltage Ripple of the MPM3833C with (a) 22uF Output Capacitor (b) 4x22uF Output Capacitors and (c) 5x22uF Output Capacitors

Design of the Second Stage Filter

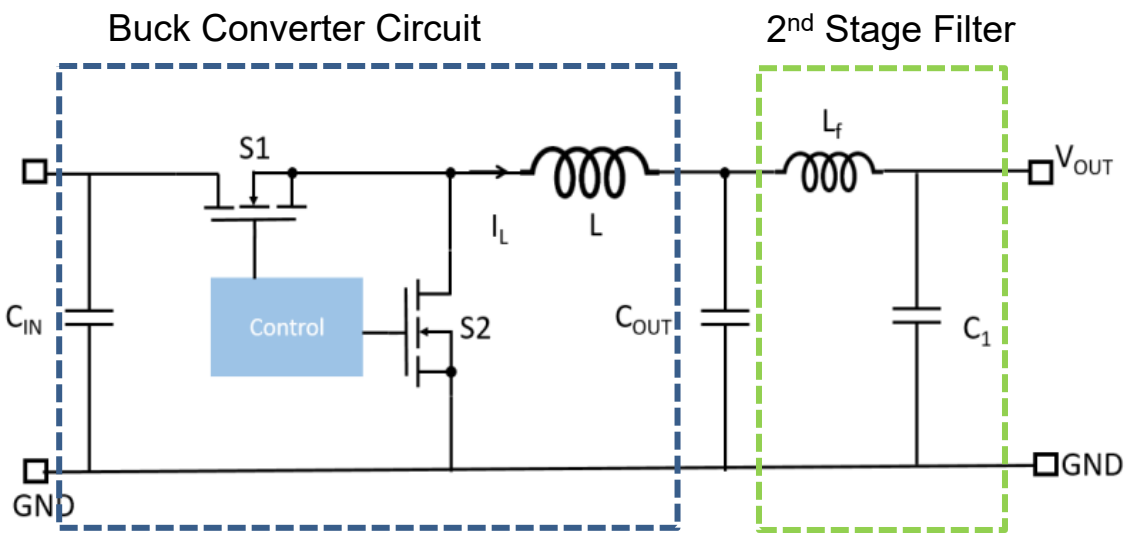


Figure 4. Second Stage LC Filter with Parallel Damping Branch [1]

- Design C_{OUT} to reduce the output voltage ripple to 5mV-10mV
- Select L_f at 0.22uH-1uH value. The inductor should be selected to have minimal DCR
- $$f_0 = \frac{f_{sw}}{10^{\frac{20log\frac{V_{O,p-p}}{V_{1,p-p}}}{-40}}}$$

[1] https://www.monolithicpower.com/cn/passive-filter-design-concept-of-buck-regulators-for-ultra-low-noise-applications

Damping of the LC filter

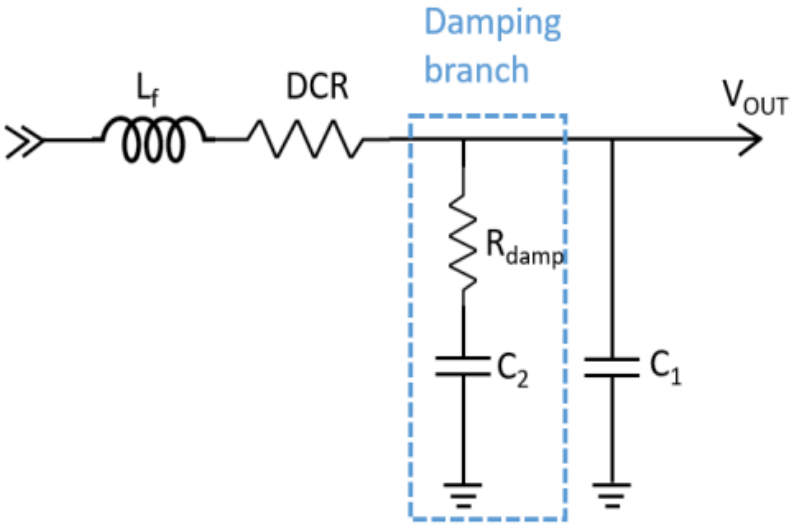


Figure 5. Second Stage LC Filter with Parallel Damping Branch

- At **load transient**, the resonance between the filtering inductor and bypassing capacitor may amplify the output ripple and create undesired ringing.
- To **avoid undesired ringing** at load transient, the second stage LC filter resonance must be properly **damped**.

Damping of the LC filter

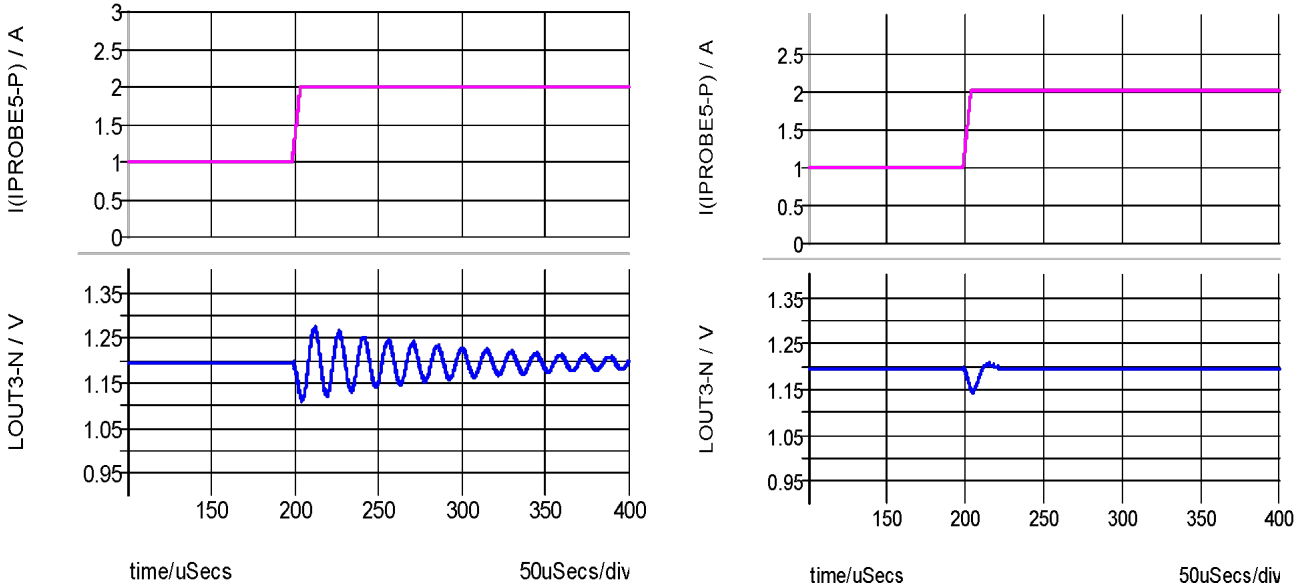


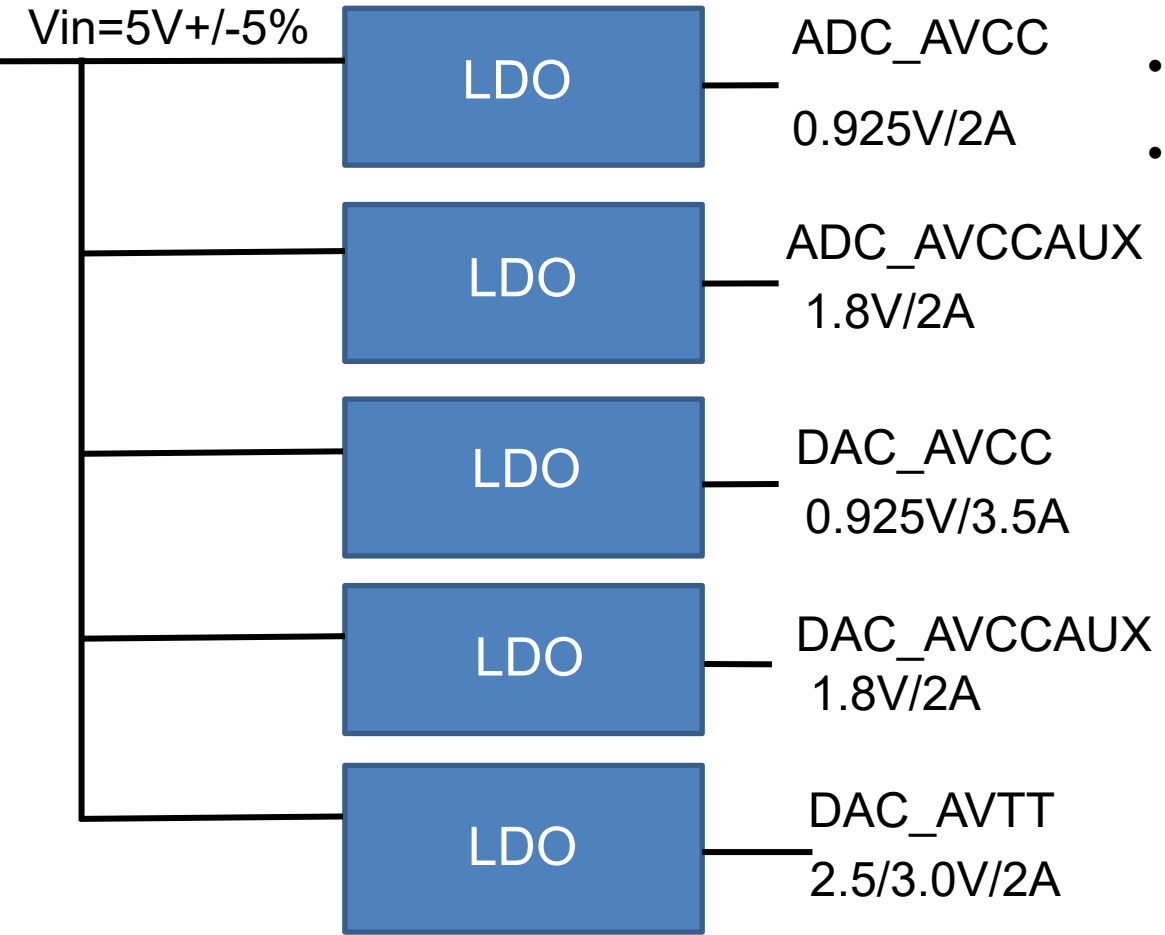
Figure 6. Step Response of (a) Underdamped LC Filter and (b) Overdamped LC filter

- R_{Damp} needs to satisfy $R_{Damp} > 2\sqrt{\frac{L_f}{C_2}}$

Design Specification for ADC rails

Rail Name	VIN	VOUT	IOUT	Target Ripple Magnitude
ADC_AVCC	5V	0.925V	2A	0.4mV
DAC_AVCC	5V	0.925V	3.5V	0.4mV
ADC_AVCCAUX	5V	1.8V	2A	5.5mV
DAC_AVCCAUX	5V	1.8V	2A	1mV
ADC_AVTT	5V	2.5V/3V	2A	5mV

Traditional Solution – LDO Approach



- High Loss
- Noise target achieved

Switch Mode Power Module + Passive Filter Solution

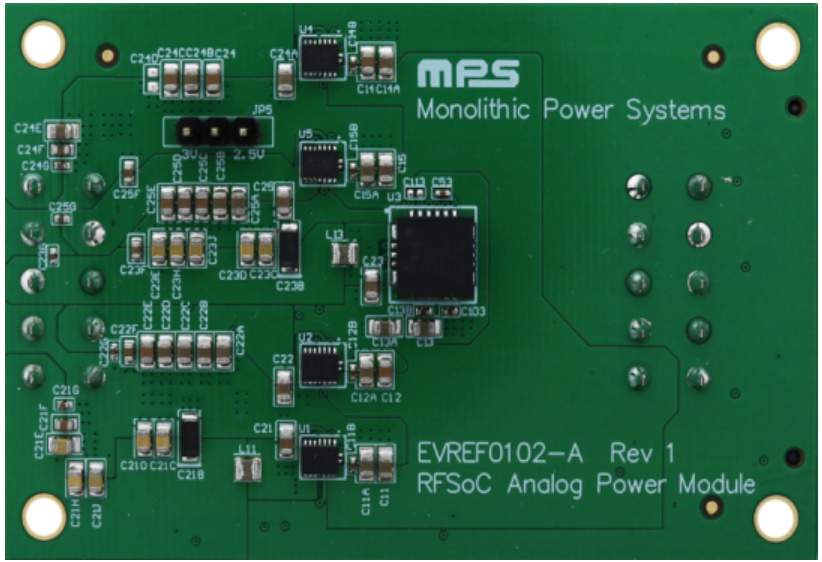
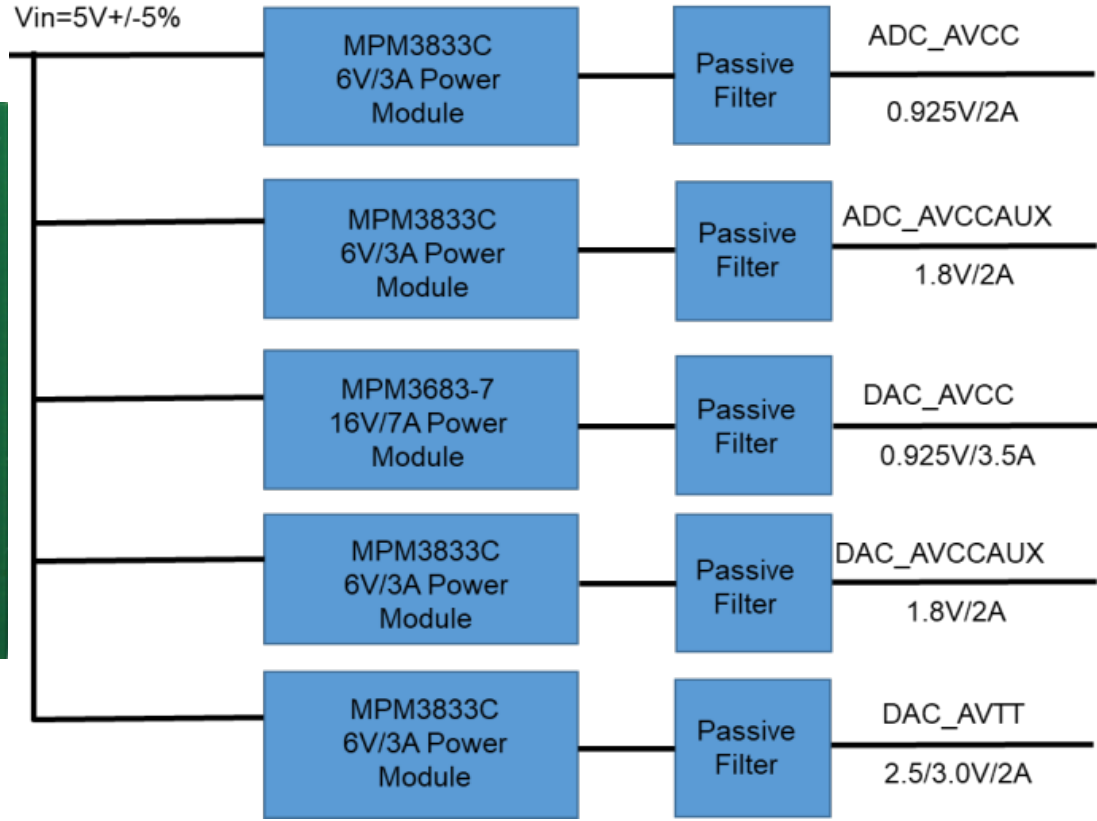


Figure 7. MPS EVREF0102 Power Module



Same Noise Performance as LDO Solution

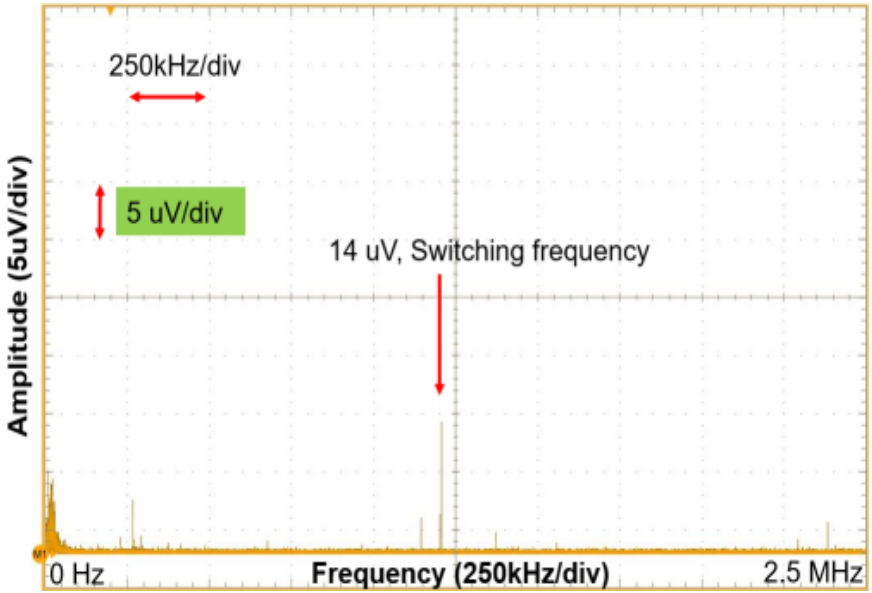


Figure 8. MPS EVREF0102 Power Module Noise Spread Spectrum

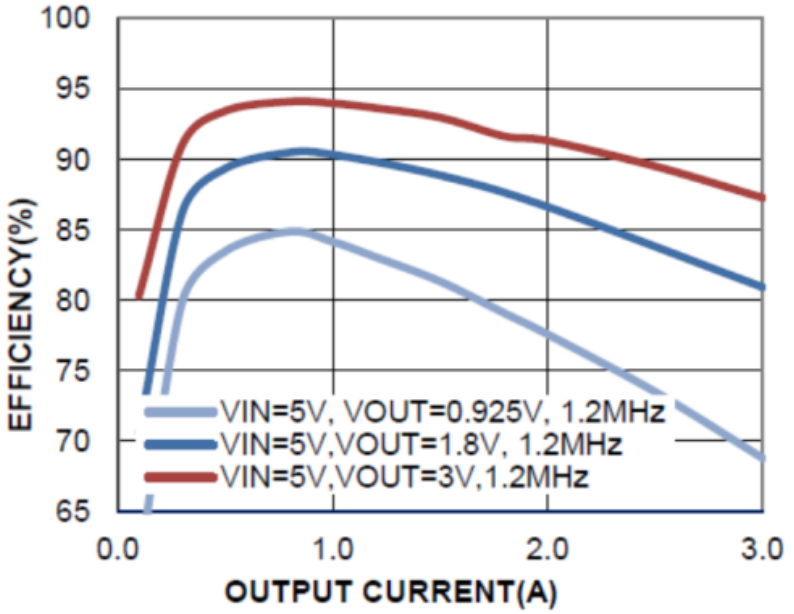


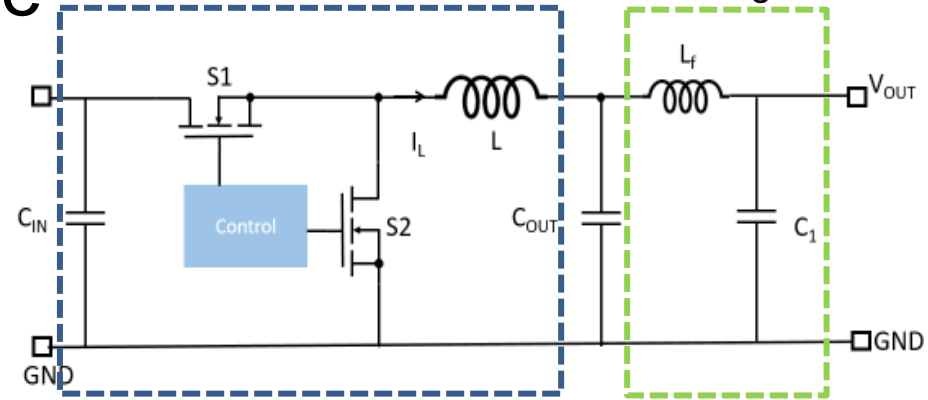
Figure 9. MPM3833C Efficiency VS. Output Current

Same noise performance

4X more efficient than LDO

Passive Filter Design Example

VIN	VOUT	IOUT	Target Ripple Magnitude
5V	0.925V	2A	20uV



STEP 1.

Calculate Output voltage ripple with 22uF output capacitor C_{out}

$$\Delta V_{C,p-p} = \frac{I_{L,p-p}}{8 f_{SW} C_{OUT}} = 3.2mV$$

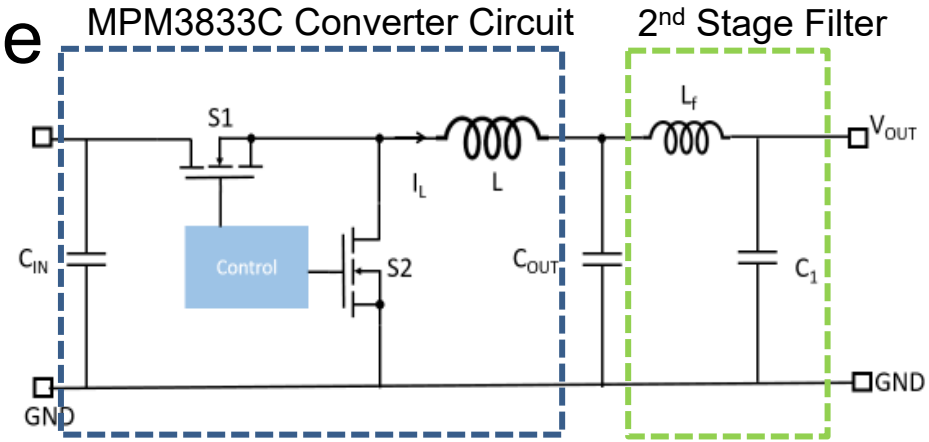
STEP 2.

Calculate the resonant frequency of second stage filter which can reduce V_{out} ripple to target magnitude

$$f_0 = \frac{f_{sw}}{10^{\frac{20log\frac{V_{O,p-p}}{V_{1,p-p}}}{-40}}} = \frac{1.15MHz}{10^{\frac{20log\frac{3.2mV}{20uV}}{-40}}} = 91kHz$$

Passive Filter Design Example

VIN	VOUT	IOUT	Target Ripple Magnitude
5V	0.925V	2A	20uV



STEP 3.

Select $L_f = 0.24uH$. The minimum second stage filter capacitance can be calculated. The significant de-rating of ceramic capacitor at DC bias should be noted.

$$C_1 = \frac{1}{4\pi^2 f_0^2 L_f} \div (0.8) = 16.25uF$$

STEP 4.

In this use case, more output capacitors are used to achieve better load transient performance. The required damping resistance can be calculated

$$C_1 = 100uF + 47uF \times 5 \times 0.8 = 288uF$$

$$R_{Damp} > 2\sqrt{\frac{L_f}{C_2}} = 58mOhm$$

Thank You