IS17.4 - Enhance a Voltage Regulator Module's Thermal Performance Using an Inductor with a Metal Band and 3D Packaging

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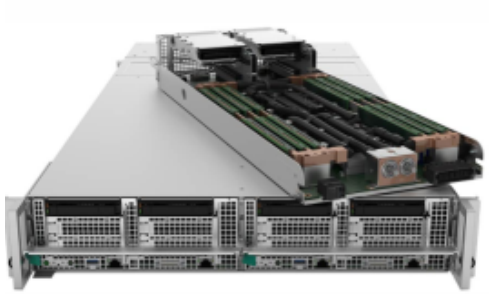
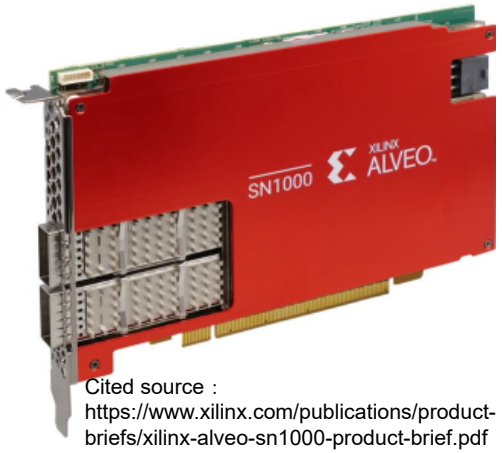
Outline

- Introduction & Background
- Industry Voltage Regulator Module (VRM) solution Analysis
- Innovative VRM Solution and Demonstration
- Analysis of Benefits and Results
- Conclusion

Introduction and Background –
What's Driving Power Innovation?



Cited source：
https://www.aspsys.com/server-list/intel-s9200wk-server/



Cited source：
https://www.xilinx.com/publications/product-briefs/xilinx-alveo-sn1000-product-brief.pdf

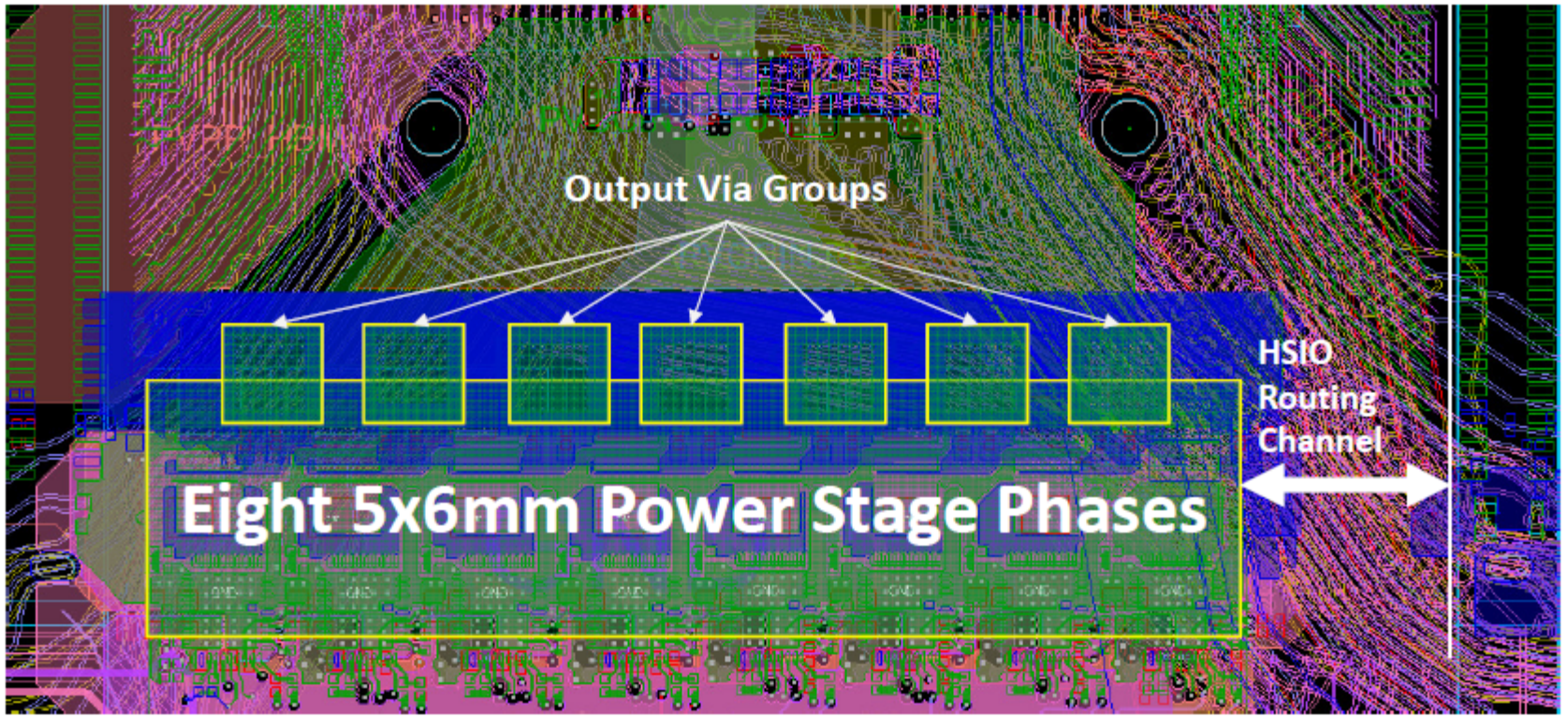
Cited source： https://globemoving.net/blog/moving-fully-populated-server-racks-during-data-center-relocation/

Cited source：https://www.supermicro.com/en

Cited source：https://www.techpowerup.com/175790/supermicro-3u-superserver-achieves-over-10-gb-s-throughput

The booming development of AI, Big data, IoT, etc facilitates extraordinary development of datacenter

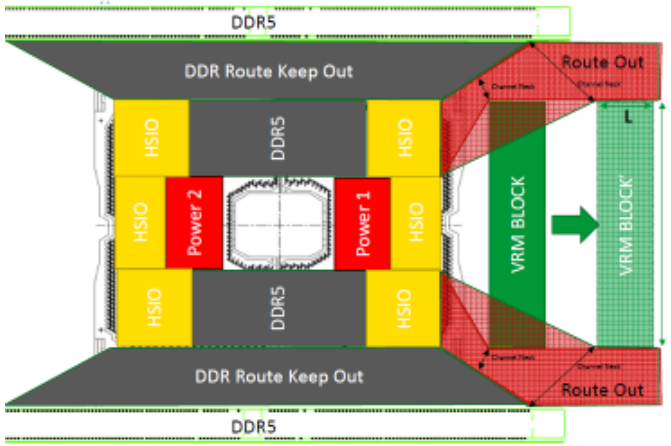
Introduction and Background-
Current Industry V-core Solution Review



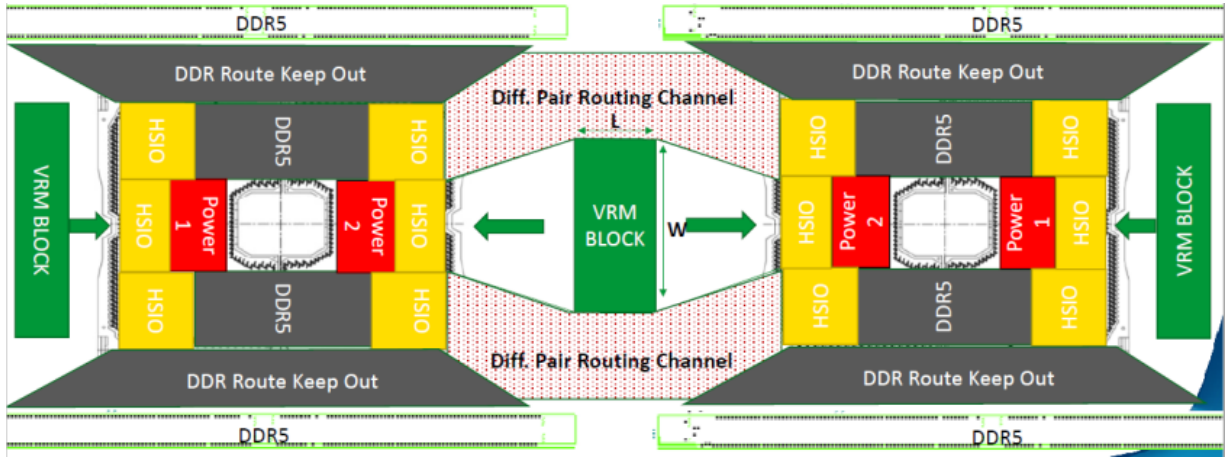
The popular planar V-Core architecture with 5x6 DrMOS plus inductors and 8 phases

Routing space is limited especially as HSIO (High Speed I/O) number keep increasing

Introduction and Background –
Current Industry Vcore Solution Review



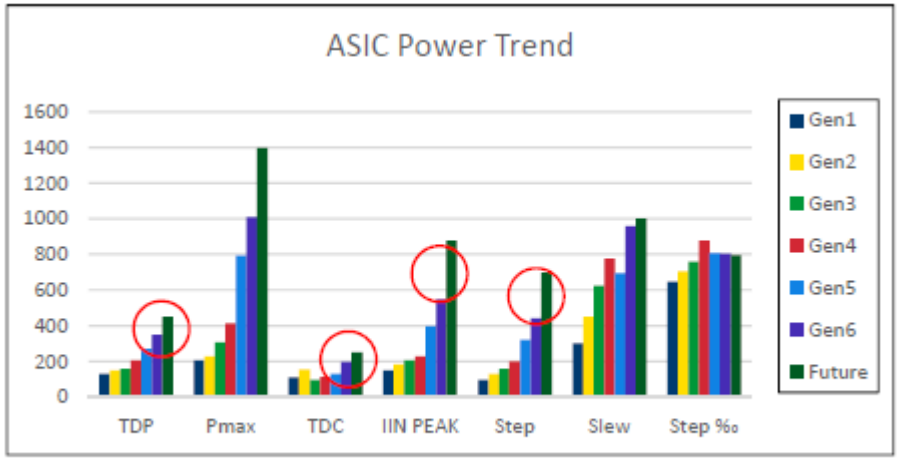
V-core scheme with single socket



V-core scheme with dual socket

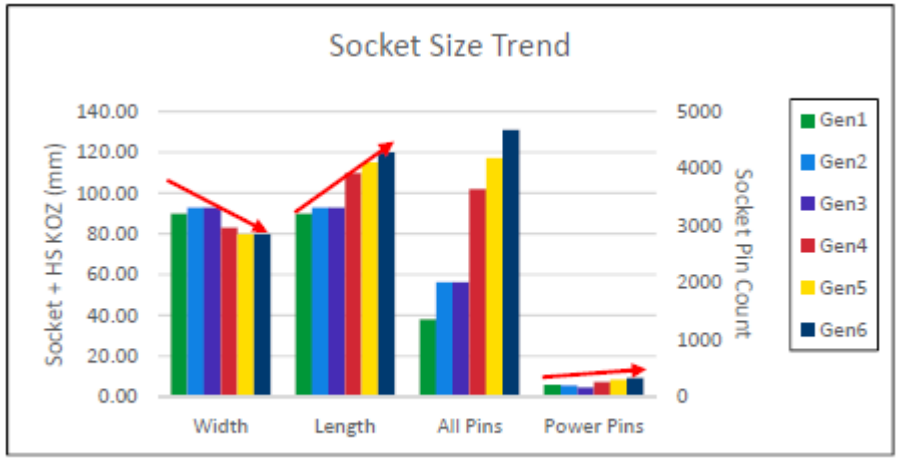
With the same solution area for V-core, trade-off needs to be made between HSIO routing space and Power Delivery Network

Introduction and Background-
Challenges and Needs for Innovative VRM Solutions



*Data based off Internet information and Estimation

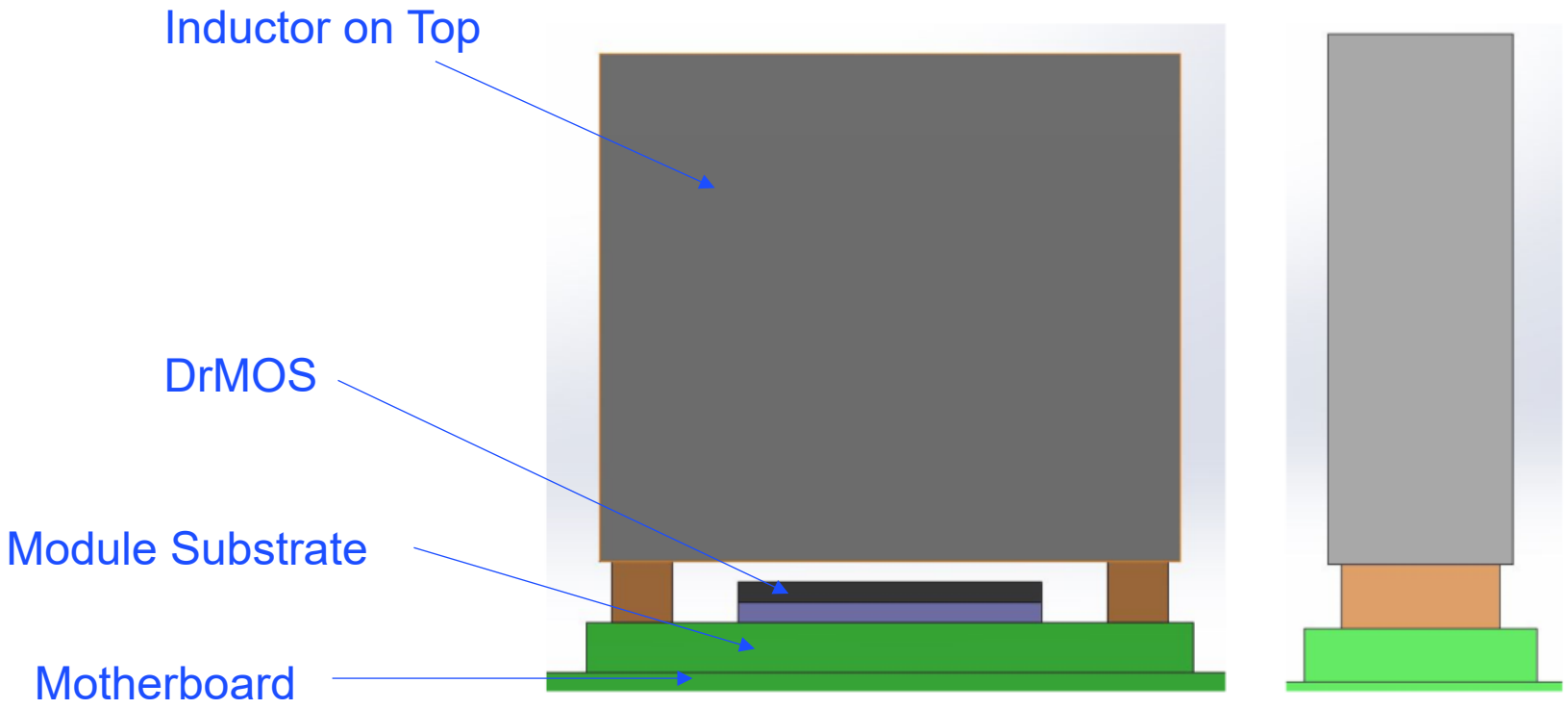
- **High power capability**
- **High current capability with more phase count**
- **Better transient performance**
- **Better thermal performance**
- **Better efficiency**



*Data based off Internet information and Estimation

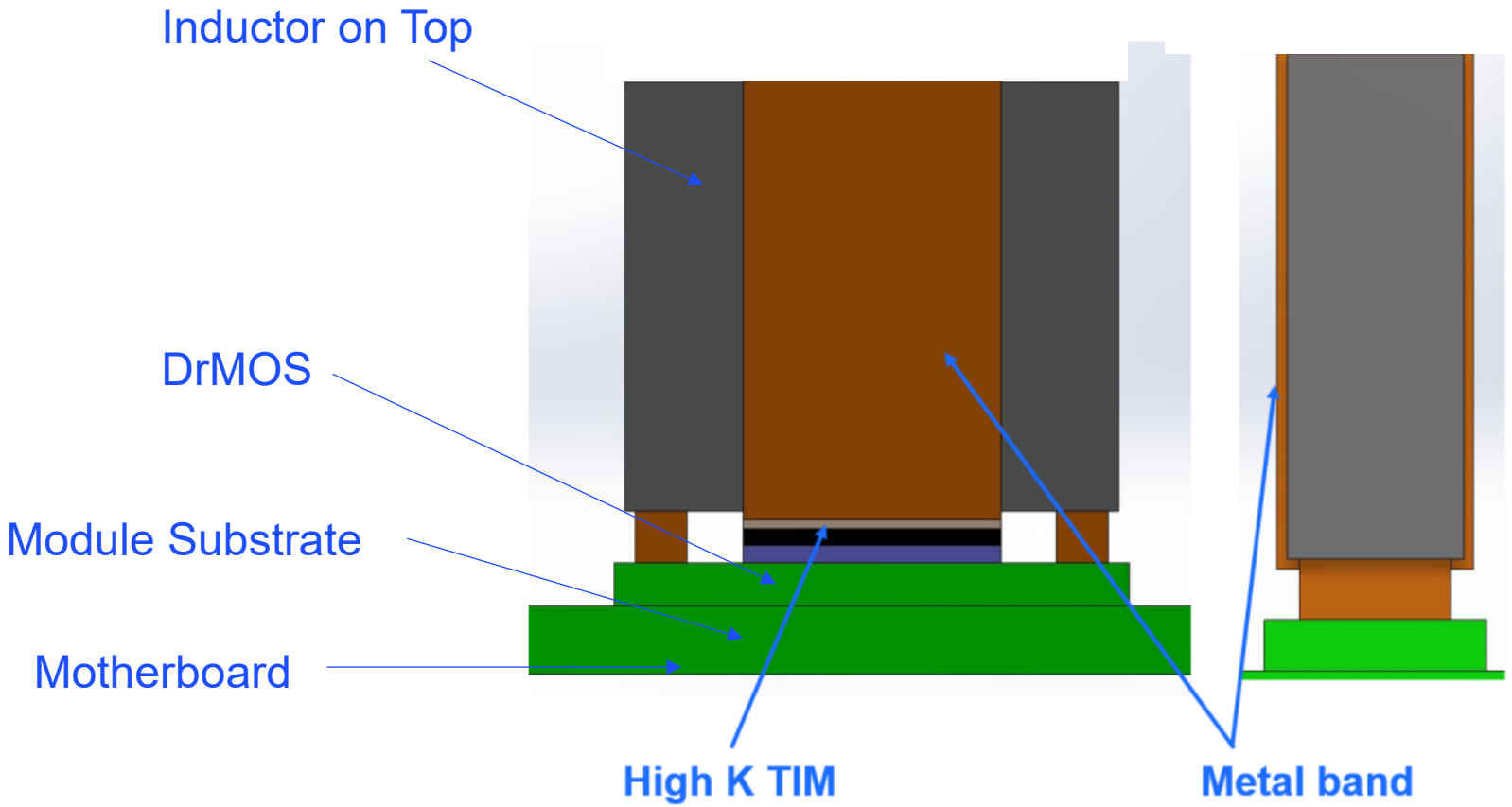
- **Slimmer form factor for more on board space for more signal and power connections**
- **Higher power density**

Innovative VRM solution –
3D packaging architecture



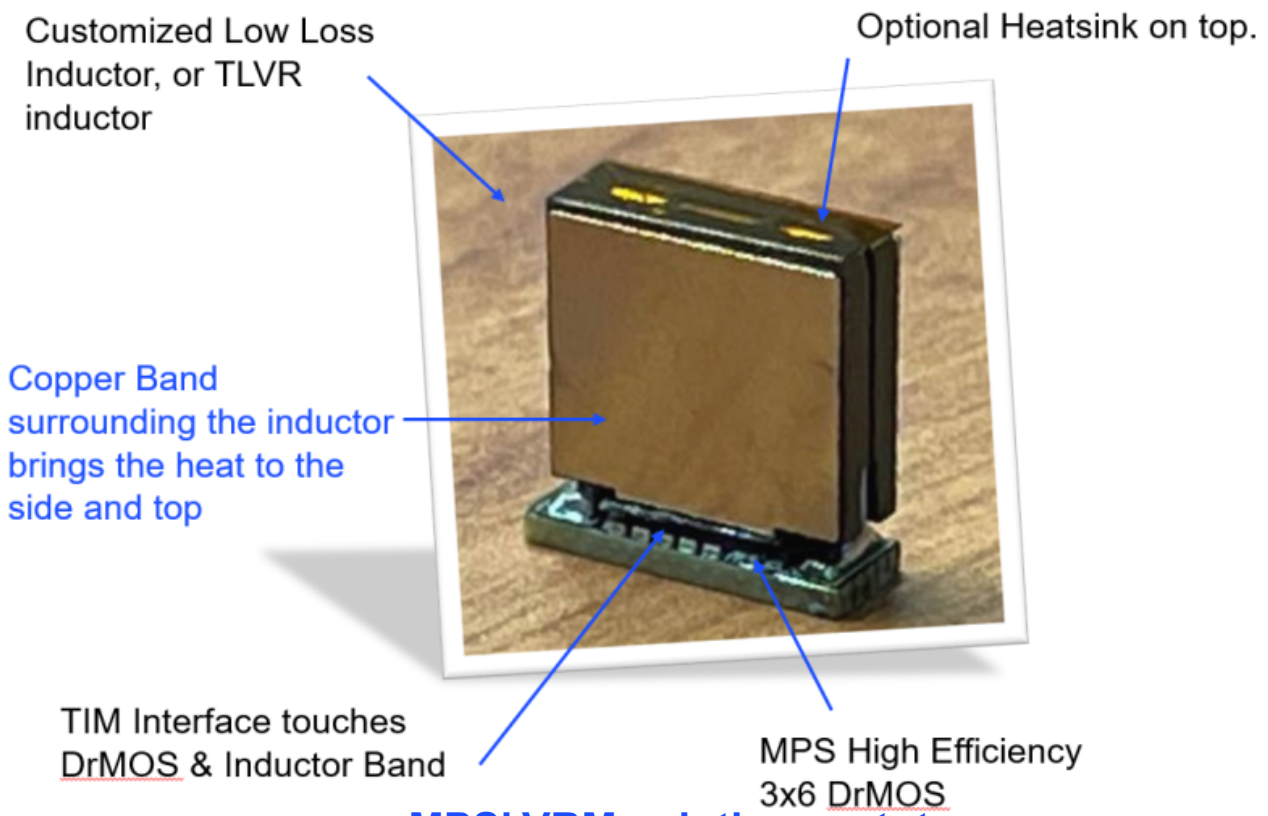
With 3D packaging architecture,
solution area for VRM can be significantly reduced

Innovative VRM solution –
MPS' VRM solution with 3D packaging and enhanced thermal performance

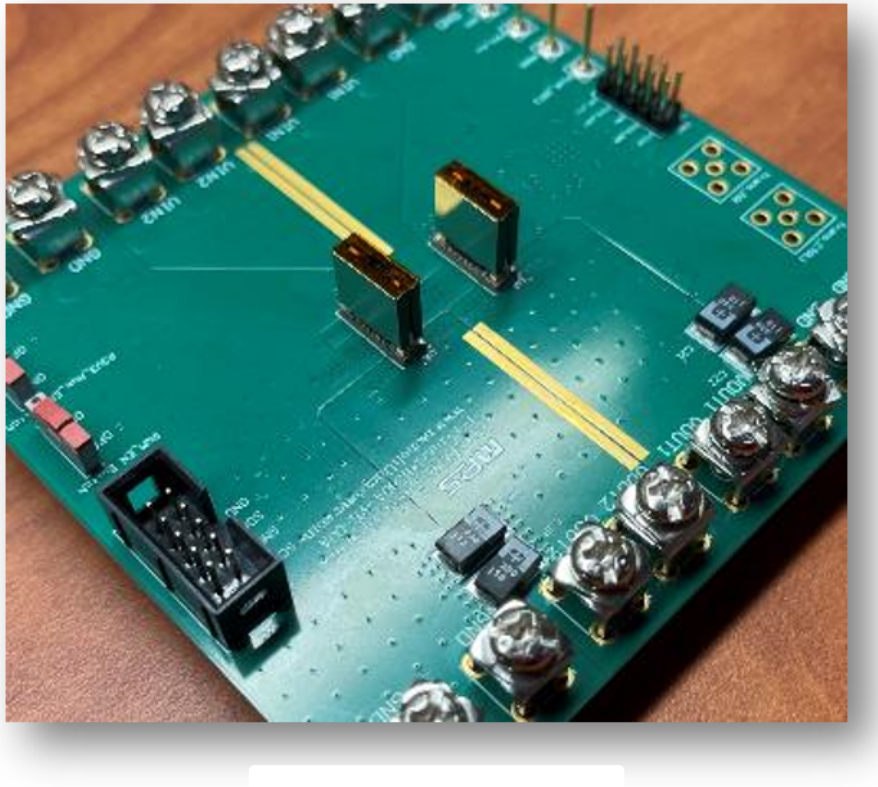


The Cu Band on Inductor and Thermal Interface Material is applied to improve thermal performance of VRM in 3D package

Demonstration of Innovative VRM solution-
Prototype and multiphase demonstration



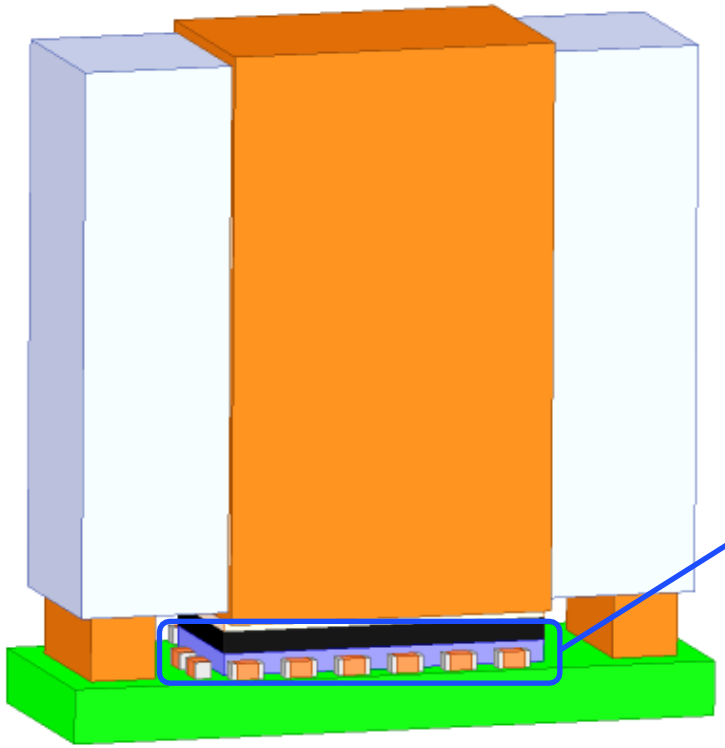
MPS' VRM solution prototype

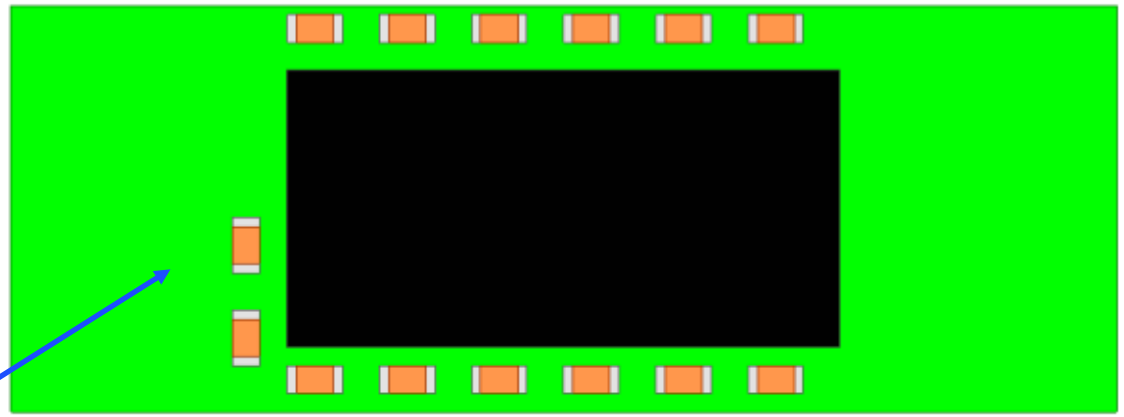


MPS' VRM solution in dual phase demonstration

Ultra-slim footprint (12x4.4mm) and thermal design enable ease of use on system level design and better thermal performance

Innovative VRM-
Integration for Ease of Use



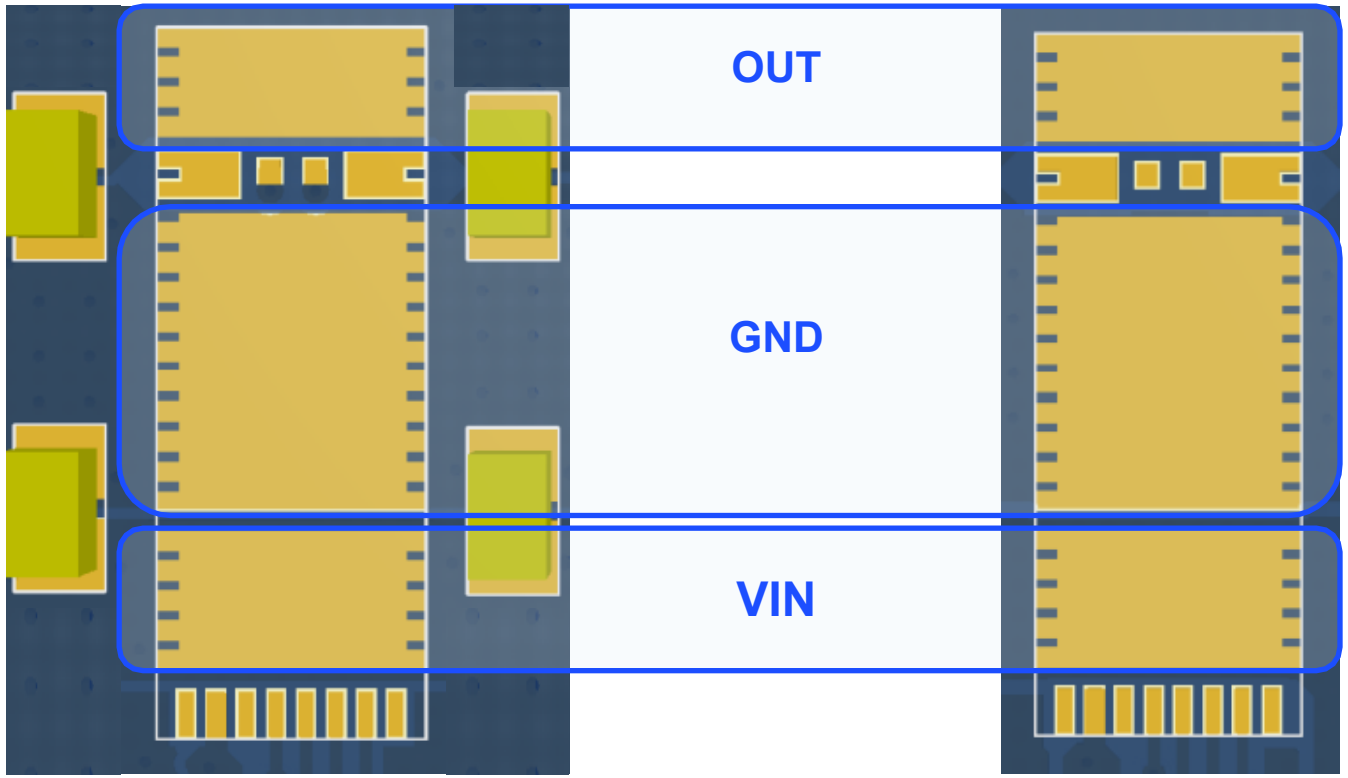


Internal components

- VDD decoupling capacitors (VDRV+VDD of DRMOS)
- BST capacitors
- Vin decoupling capacitors

Integration of components optimizes decoupling performance, eases system level design and further reduces solution size

Innovative VRM-
Integration for Ease of Use



Solution with Caps on Top layer

Solution with Caps on Bottom layer

Ultra slim module footprint for significant solution size reduction
Pin out for ease of use with optimized decoupling loop for both Vin and OUT

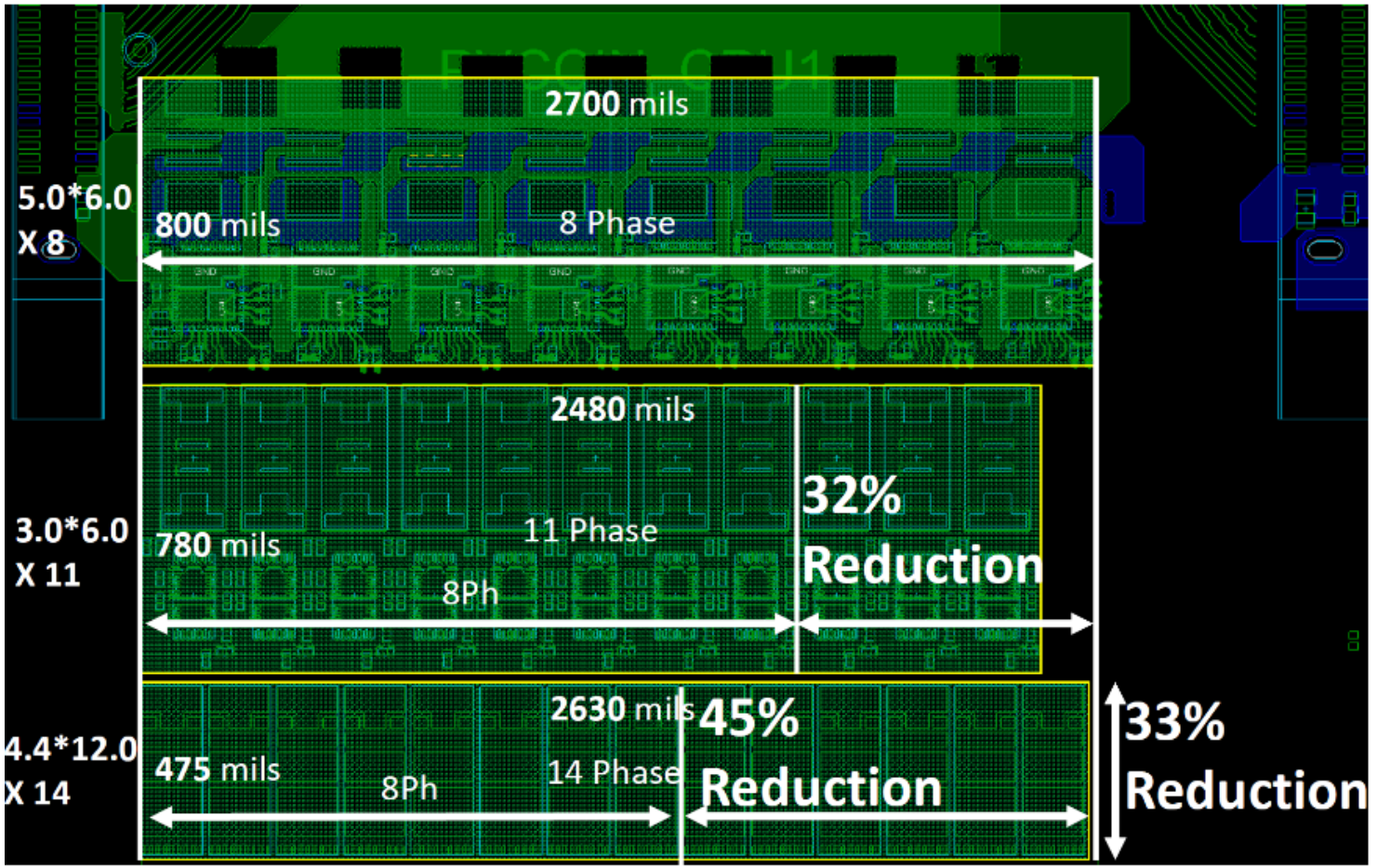
Innovative VRM on System-Level Application-

Reduces Solution Size Significantly

Discrete solution with 5x6mm DrMOS

Discrete solution with 3x6mm DrMOS

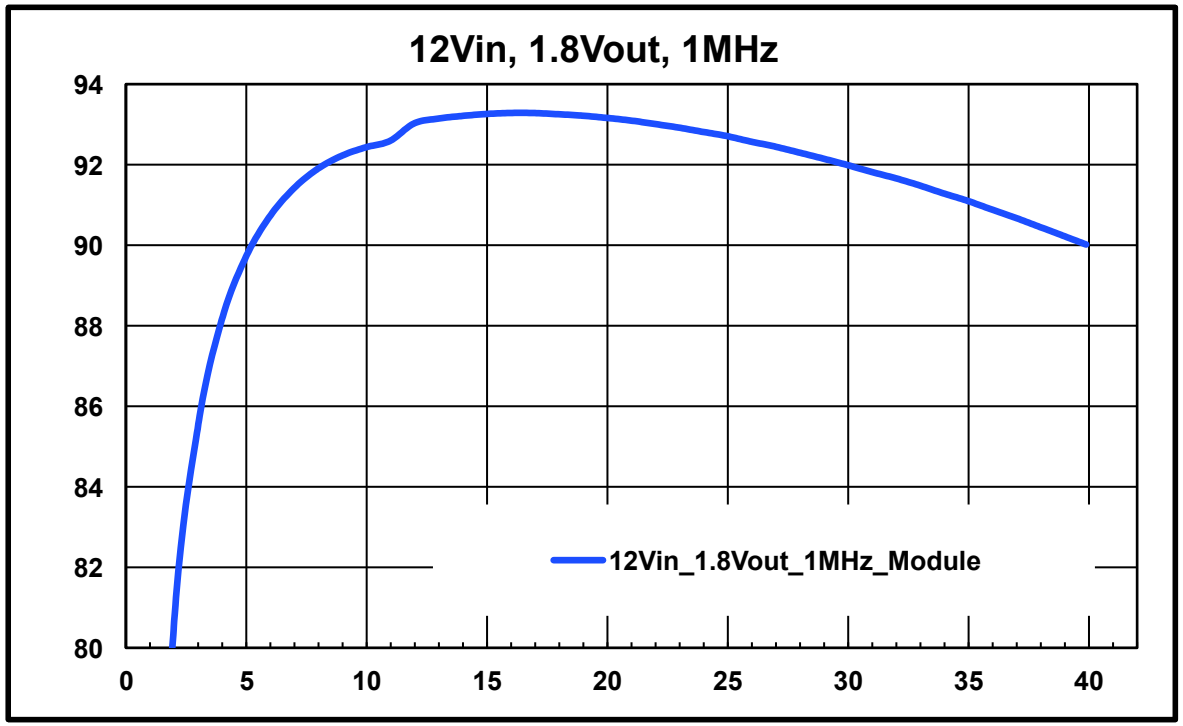
MPS' Innovative VRM solution

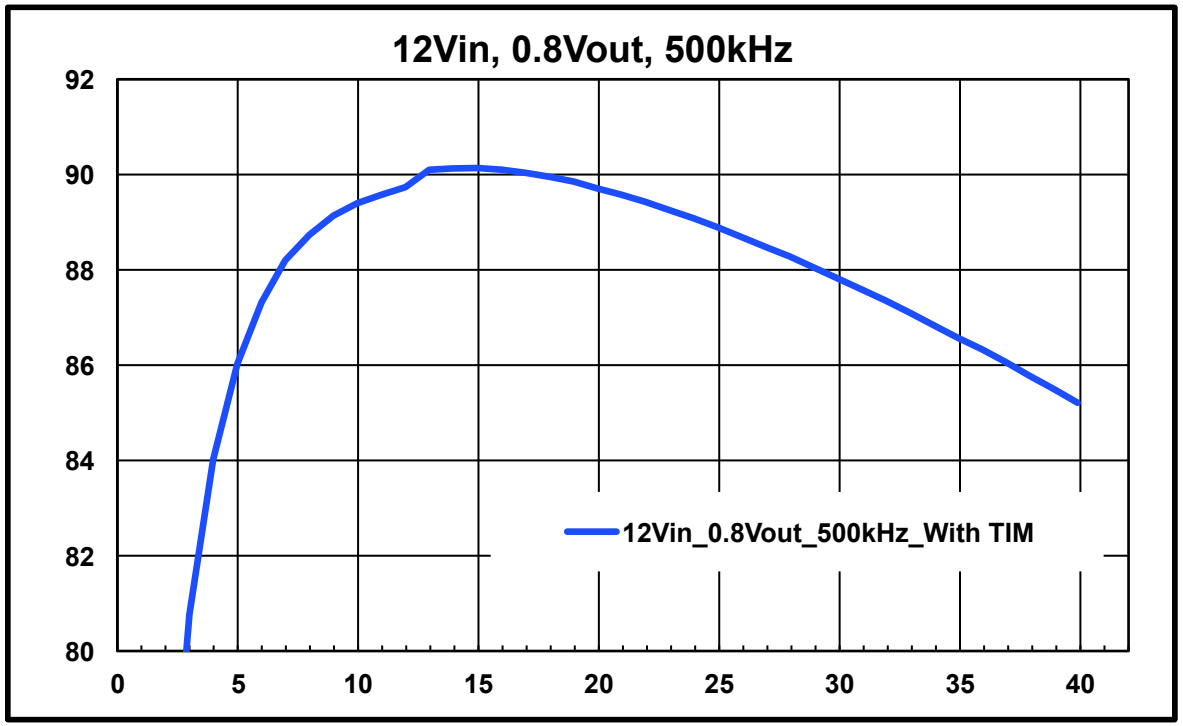


The Ultra-slim VRM solution requires much less space for system level board design

Innovative VRM Solution Efficiency in Typical Applications

- The proposed ultra-slim VRM in single phase operation



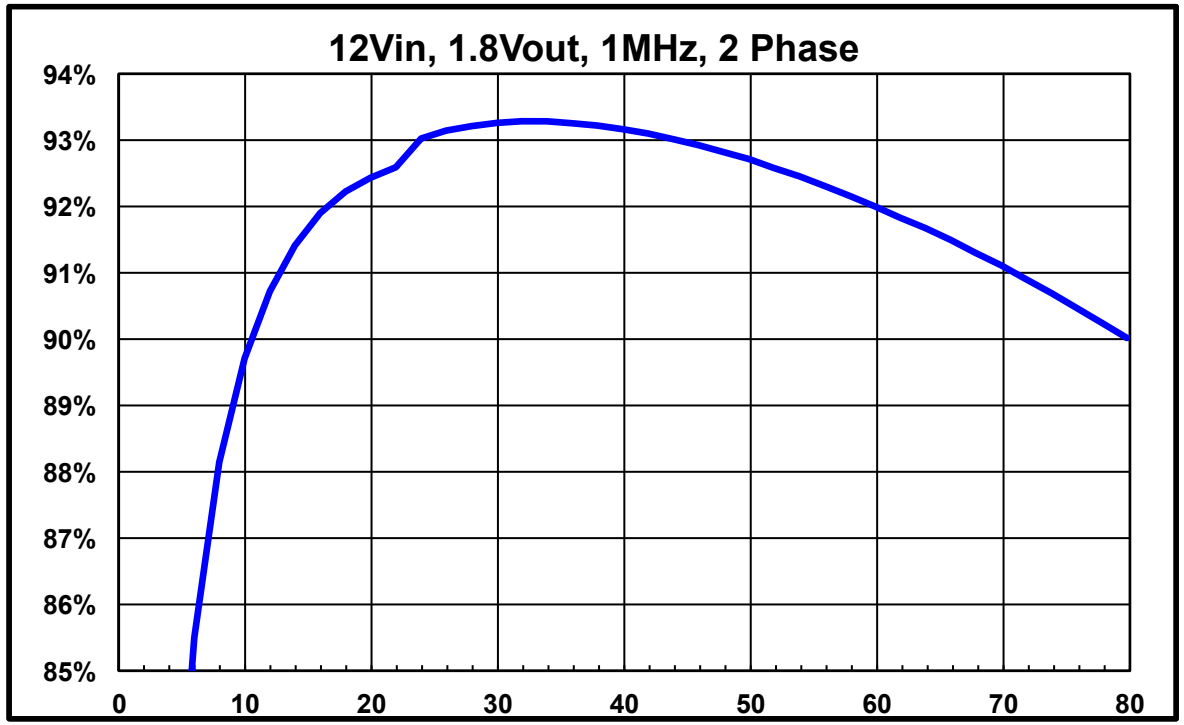


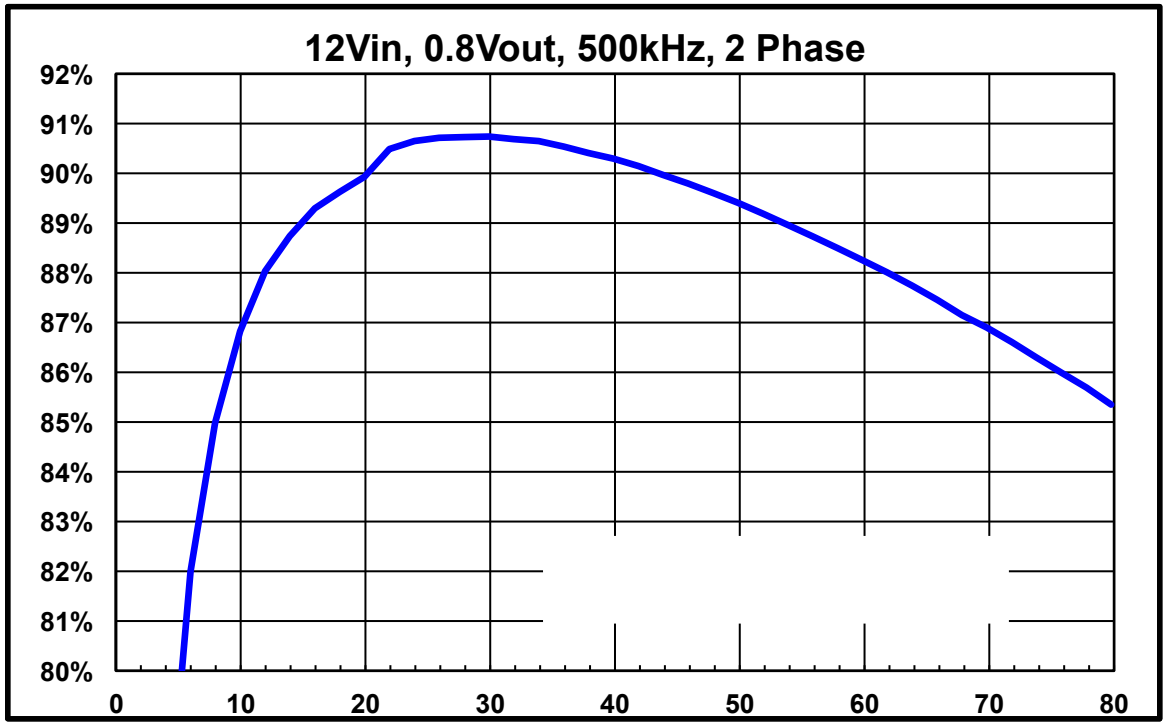
With 12Vin, 1.8Vout @1MHz, the peak efficiency is 93%, and 90.2%@40A

With 12Vin, 0.8Vout @ 500KHz, the peak efficiency is 90.14%, and 85.5% @ 40A

Innovative VRM Solution Efficiency in Typical Applications

- The proposed ultra-slim VRM in dual phase operation



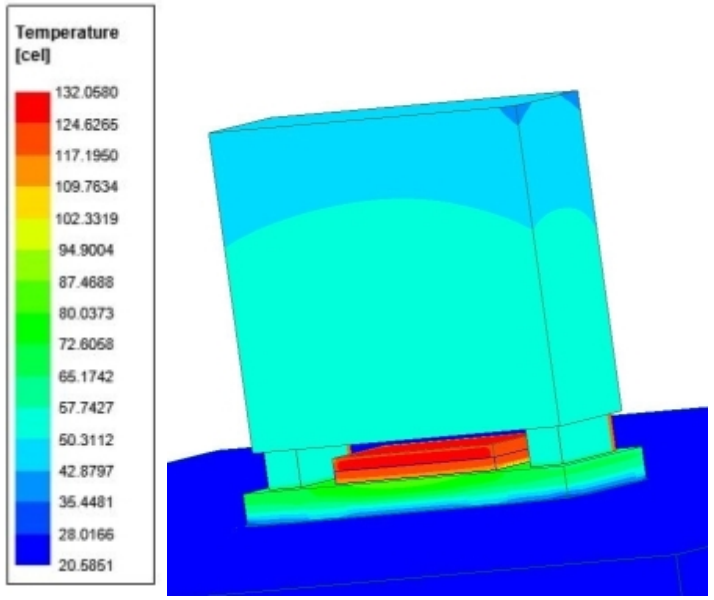


With 12Vin, 1.8Vout @1MHz, the peak efficiency is 93.2%, and 90.2%@40A

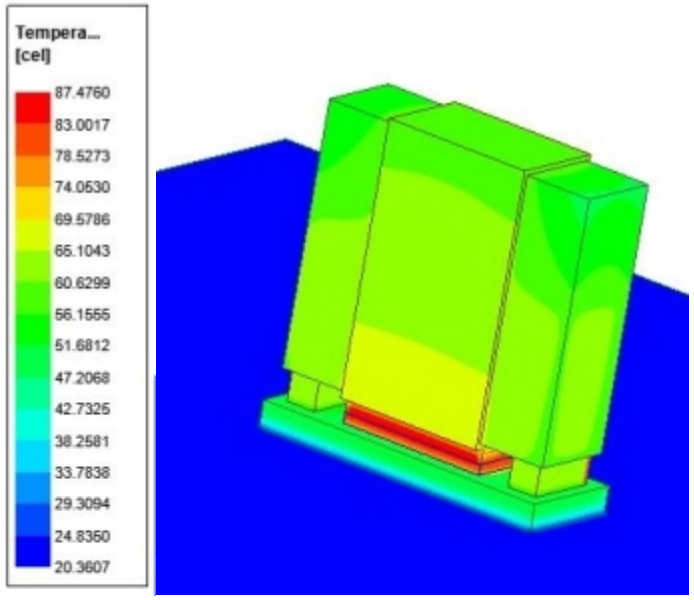
With 12Vin, 0.8Vout @ 500KHz, the peak efficiency is 90.5%, and 85.5% @ 40A

Innovative VRM – Enhanced Thermal Performance

- **Significant reduction in junction temperature**



$T_{J,max}$ = 132.1°C
Traditional L-on-Top design



$T_{J,max}$ = 87.5°C
MPS' Innovative VRM solution

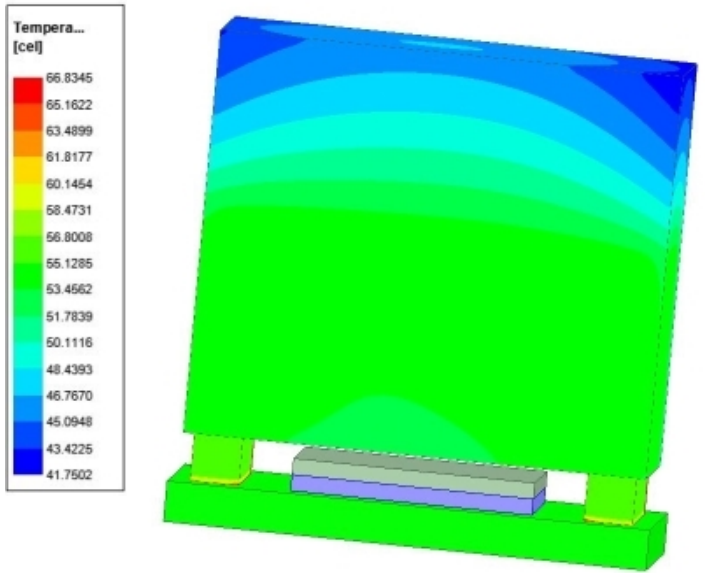
Simulation Boundary Conditions

- **400CFM air flow is defined on the surface**
  - **32m/s speed based on the defined area**
- **Loss estimation based on 12Vin, 1.8Vout, 30A**
  - **Die, 2.4W**
  - **Inductor, 0.8W**
- **A equivalent 6-L EVB is set on the bottom**
  - **51x51mm in area**
  - **1.6mm thick**

Innovative VRM features 45°C lower junction temperature

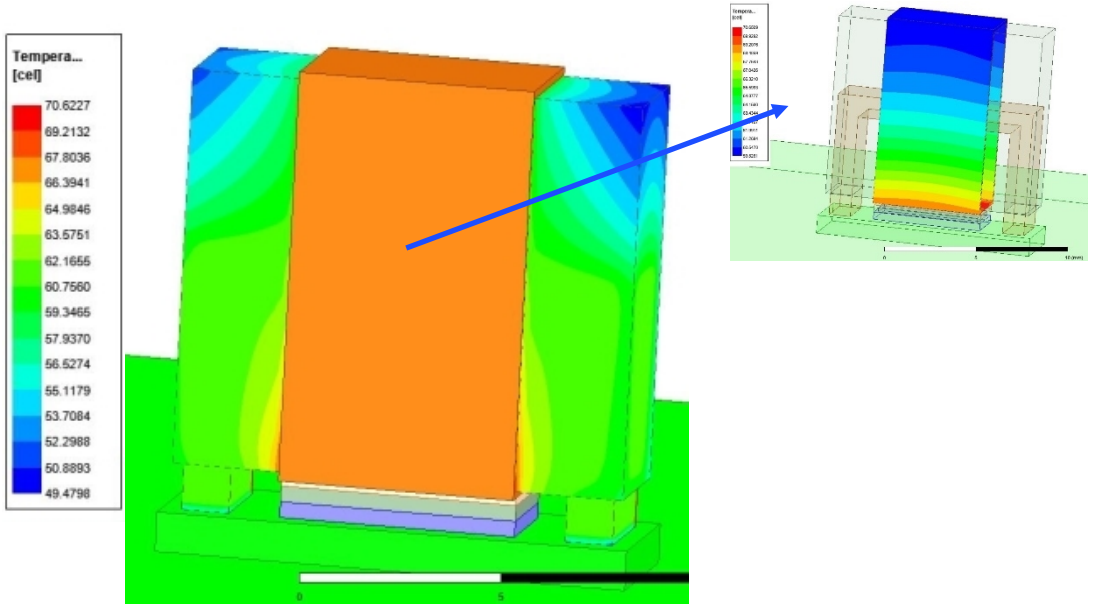
Innovative VRM- Enhanced Thermal Performance

- **Metal band design with TIM as heatsink**



Traditional L-on-Top design

$T_{max,L}$ = 68.8°C



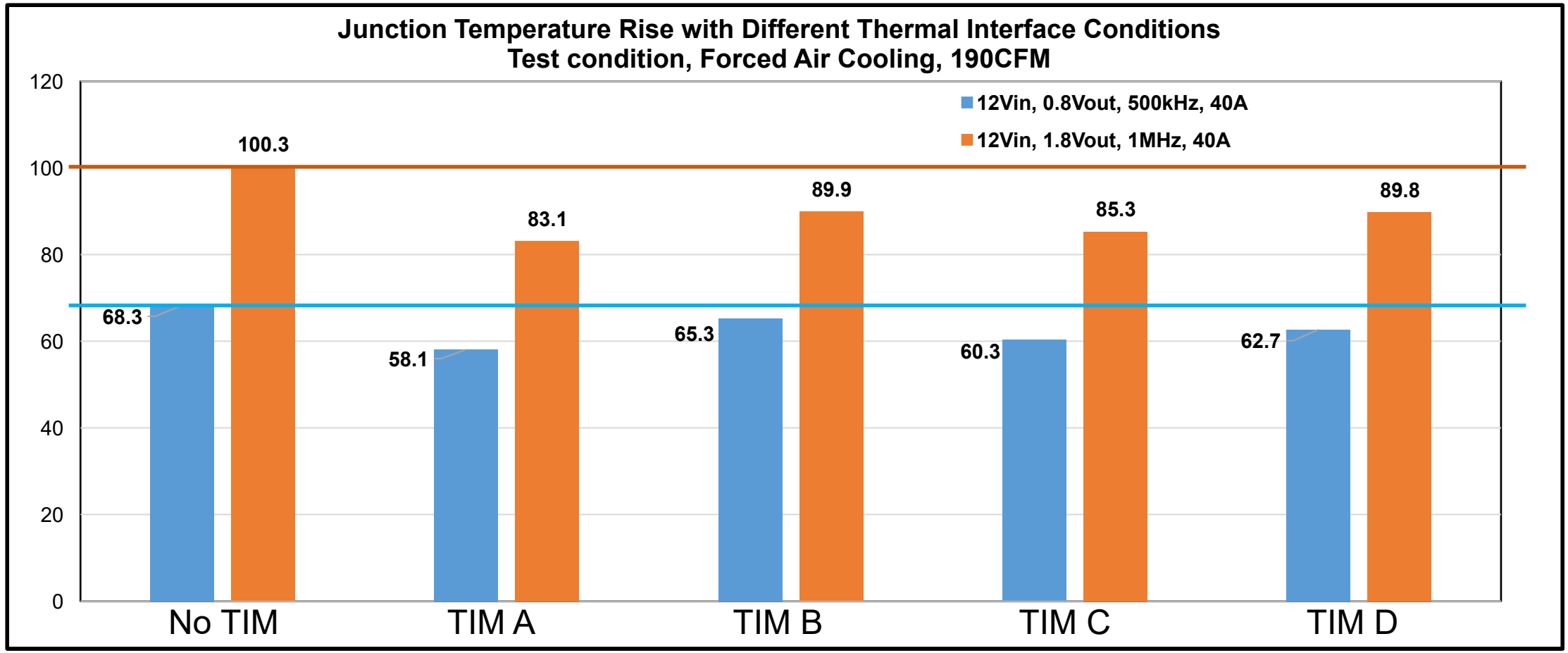
MPS' Innovative VRM solution

$T_{max,L}$ = 70.6°C

Cu band on Inductor greatly contributes heat transfer from IC to ambient

Innovative VRM- Enhanced Thermal Performance

- Bench verification on different TIMs for enhanced thermal performance



The proposed VRM shows >10°C junction temperature reduction with different Thermal Interface Materials

Conclusion

- An innovative VRM solution is introduced with ultra-slim form factor and enhanced thermal performance
- 3D Packaging with Cu band on inductor, and thermal interface material filled in the gap between Cu band and DrMOS IC, which significantly reduced the junction temperature of module
- Innovative VRM solution features 4.4x12mm footprint, with decoupling components integrated, significantly reduce system level solution size
- MPS' Innovative VRM features high efficiency, up to 93% and junction temperature reduction up to 45 ^{o}C

Q&A

Thanks