MPQ3426 Pre-Boost Reference Design

Simple Solution to Cold-Crank Transients

1 Table of Contents

1 Overview

1.1 Description

Start-stop functionality is an expected feature in more and more new car models from any manufacturer. However, this presents a challenge in automotive electronics design, as starting the motor in cold weather can make the battery's voltage drop as low as 3V. This is called a "cold crank."

The power stage for most 12V automotive systems consists of a single buck converter that typically regulates the output voltage to 5V or 3.3V. Even if the regulator starts working in low-dropout mode, most circuits can be affected by a dip in the input voltage, and may stop functioning. The electronic control unit (ECU) always starts from the nominal battery voltage of 12V, and it is after start-up that cold-crank transients can occur. Using a pre-boost offers a solution to this problem.

A pre-boost consists of a boost converter connected in series before a buck converter, which raises the voltage when it falls below a certain threshold. This allows the buck converter to have a steady input voltage and correctly regulate its output to a constant level, regardless of transients in the 12V harness. The boost's bias voltage is provided by the main buck converter, thus extending the operating input voltage of the system to 2V or lower.

This reference design will help engineers designing a pre-boost for a power supply up to 18W.

1.2 Features

- Wide Operating Input Range (from <2V to 36V)
- 3.5A Continuous Output Current
- 350kHz to 2.5MHz Programmable Switching Frequency
- Low-Dropout Mode
- Over-Current Protection (OCP) with Valley-Current Detection and Hiccup Mode
- Available with Wettable Flank
- High Efficiency Up to 92%
- Reverse Polarity Protection
- Second-Order EMI Filter
- Available in AEC-Q100 Grade 1
- Meets CISPR25 Class 5 EMC Standard

1.3 Applications

- Automotive Infotainment
- Automotive Safety and ADAS

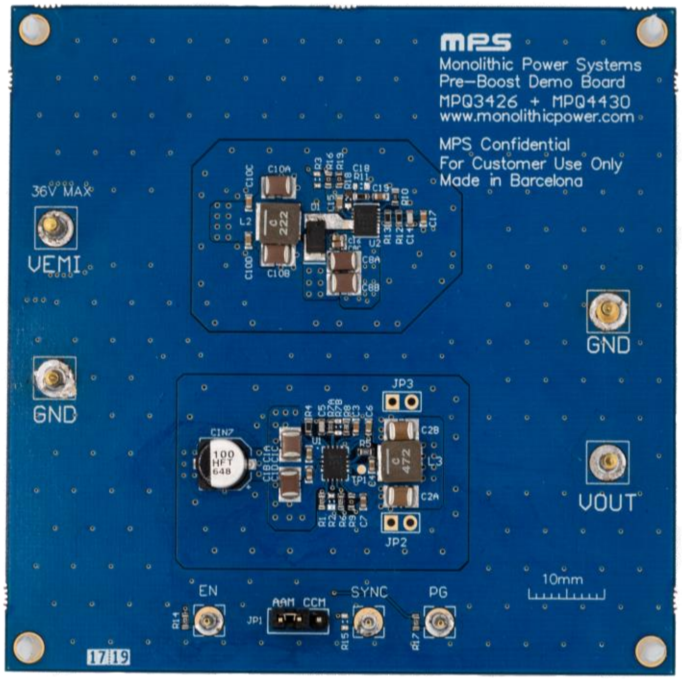


Figure 1: MPS Pre-Boost Reference Design Board

2 Reference Design

2.1 Block Diagram

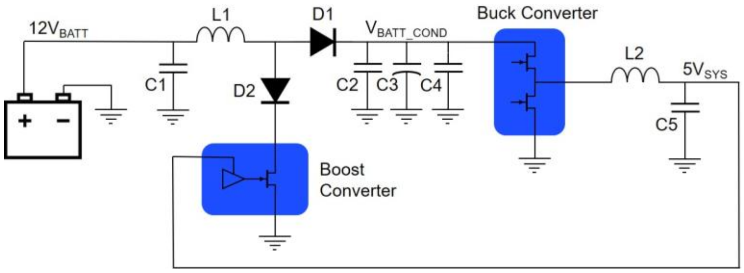


Figure 2: Block Diagram

In addition to being part of the pre-boost converter, L1 and C1 act as an input filter for conducted EMI. D1 protects the buck converter IC from reverse polarity. D2 is optional to protect the boost IC if no other reverse polarity protection is implemented.

2.2 Related Solutions

This reference design is based on the following MPS solutions:

Table 1: System Specifications

MPS Integrated Circuit	Description
MPQ3426	Asynchronous boost converter with 6A of switch current capability and a 3.2V bias voltage
MPQ4430	36V synchronous buck converter capable of delivering 3.5A

2.3 System Specifications

Table 2: System Specifications

Parameter	Specification
Working input voltage	<2V$_{DC}$ to 36V$_{DC}$
Start-up input voltage	5V$_{DC}$ to 36V$_{DC}$
Output voltage	5V$_{DC}$
Maximum output current	3.5A (at 5V output)
Switching frequency	400kHz
Board form factor	90mmx90mmx10mm
Efficiency	>85%
12V output ripple	15mV

Table 3: Battery Voltage Transient vs. Output Current

Lowest Battery Voltage during Cold Crank	Max Output Current at 5V Output Voltage
1.5V	0.9A
2.0V	1.2A
2.5V	1.6A
3.0V	2.1A
3.5V	2.8A
4.0V	3.3A
4.2V	3.5A

3 Design

3.1 Selecting the Input Capacitor

The pre-boost requires a capacitor to supply the AC ripple current to the inductor while limiting noise at the input source. Use a low-ESR, >10µF capacitor to minimize noise. Ceramic capacitors are recommended, as they act as part of the input filter for conducted emissions. However, since they absorb the input switching current, an adequate ripple current rating is also required. Use a capacitor with an RMS current rating greater than the calculated inductor ripple current.

This capacitor should be placed close to the inductor. The IC also requires a small, 1µF ceramic capacitor close to its VIN bias supply for the driver circuit.

3.2 Selecting the Inductor

In a common boost converter, a higher-value inductor is typically selected to reduce the inductor's ripple current. However, in a pre-boost application this is less important than reducing its impact on the cost and efficiency of the whole system.

Several considerations must be accounted for when choosing the inductor for a pre-boost to ensure correct regulation:

- The inductor's peak current should not exceed 75% of the boost's converter switch current limit.
- MPQ3426's current limit changes depending on the duty cycle. Refer to page 5 of the part's datasheet before doing your design.
- The inductor's peak current should not exceed the specified inductor's saturation current.

The calculation for the inductor's peak current (I_{L_PEAK}) should take into account the highest value for the input current (I_{L_DC}), which is when the input battery voltage (V_{BATT}) decreases during a cold crank event and there is a maximum load. Calculate this using Equation (1):

$$I_{L\_DC} = \frac{V_{SYS} \cdot I_{SYS}}{V_{BATT} \cdot \eta} \tag{1}$$

Where V_{SYS} and I_{SYS} refer to the system's output voltage and current, V_{BATT} is the battery's voltage during a cold crank event, and the efficiency (η) can be obtained from the buck converter's datasheet or empirically.

In the evaluation board, V_{SYS} is 5V, the maximum I_{SYS} is 3.5A, and the pre-boost has its output voltage (V_{BATT_COND}) set to 9.5V. The MPQ4430's efficiency can be estimated as about 90% in these conditions. Calculate I_{L_PEAK} using Equation (2) and Equation (3):

$$\Delta I_L = \frac{V_{BATT} \cdot (V_{BATT\_COND} - V_{BATT})}{V_{BATT\_COND} \cdot f_{SW} \cdot L} \tag{2}$$

$$I_{L\_PEAK} = I_{L\_DC} + \frac{\Delta I_L}{2} \tag{3}$$

In this application, as I_{L_DC} dominates the I_{L_PEAK} value, reducing ΔI_L does not have a significant impact on I_{L_PEAK}, but does increase the inductor's size and conduction losses. A 2.2µH inductor is a good compromise between size, losses, and EMI filtering capability.

3.3 Selecting the Output Capacitor

The output capacitor maintains the DC output voltage and affects the output ripple of the pre-boost. Since the only load connected to the pre-boost output is the buck converter, the output ripple requirement is non-existent as long as the buck converter remains stable. However, a large output capacitance helps smooth the voltage drop during a cold crank event so that the boost converter has some margin to start switching. A ceramic capacitor between 4.7µF and 22µF is usually suitable. Placing a smaller capacitor close to the IC and diode helps reduce the return path for the high-frequency current.

A 100µF electrolytic capacitor also helps smooth the voltage drop of V_{BATT_COND}, and dampens the input filter in case the input voltage oscillates due to the filter's resonant frequency.

3.4 Selecting the Diode

The output rectifier diode (D1 in Figure 2) supplies current to the inductor when the internal MOSFET is off. Use a Schottky diode to reduce losses from the diode forward voltage and recovery time. The diode should be rated for a reverse voltage greater than the expected output voltage. The average current rating must exceed the maximum expected I_{SYS}, and the peak current rating must exceed I_{L_PEAK} during a cold crank event.

In applications where there is no reverse polarity protection for the system, the pre-boost IC needs an additional diode to protect its internal FET. D2 represents this protection diode (see Figure 2). Choose a similar diode to D1.

Note that D2 is not directly in the power path for the buck converter, and thus it does not introduce losses during normal operation.

3.5 Setting V_{BATT_COND}

V_{BATT_COND} is set by the voltage divider in the pre-boost IC's FB pin. Calculate V_{BATT_COND} with Equation (4):

$$V_{BATT\_COND} = \mathrm{V}_{FB} \cdot \left(1 + \frac{R_{TOP}}{\mathrm{R}_{BOT}}\right) \tag{4}$$

Where R_{TOP} is the top feedback resistor, R_{BOT} is the bottom feedback resistor, and V_{FB} is the feedback reference, which equals 1.225V.

In a pre-boost, V_{BATT_COND} should be set to a value that is not reached during normal conditions (typically below 10.8V), but is high enough that its load current does not become too high and that the buck converter does not enter low-dropout mode.

For this application, V_{BATT_COND} is set to about 9.4V, with R_{TOP} = 86.6kΩ and R_{BOT} = 13kΩ.

3.6 Setting the Switching Frequency

The switching frequency (f_{SW}) is set by connecting a resistor (R_{FSET}) between the FSET pin and ground, calculated with Equation (5):

$$f_{SW} = 23 \cdot \left(R_{FSET}^{-0.86}\right) \tag{5}$$

Where f_{SW} is in MHz, and R_{FSET} is in kΩ.

The pre-boost's switching frequency is not restricted by EMC performance, as it turns off during testing. This means that higher frequencies can be used to reduce ΔI_L in case it is needed.

In this application, R_{FSET} = 91kΩ, which makes f_{SW} = 475kHz.

3.7 V_{IN} Bias Supply

The VIN pin in the MPQ3426 should not be connected to the battery input voltage, as its voltage range admits 3.2V to 22V. To ensure that it will operate during a cold crank event and will not be damaged by transients in the battery line, it should be connected to the buck's V_{SYS}. This also helps improve the standby consumption.

3.8 VDD Gate Drive Supply

In the MPQ3426, the VDD pin is the output voltage of the internal LDO. When V_{SYS} is equal to or below 5.9V, this pin can be connected to the buck's output voltage. Doing so bypasses the LDO and ensures that a higher voltage is applied to the MOSFET's gate, increasing efficiency.

3.9 Schematic

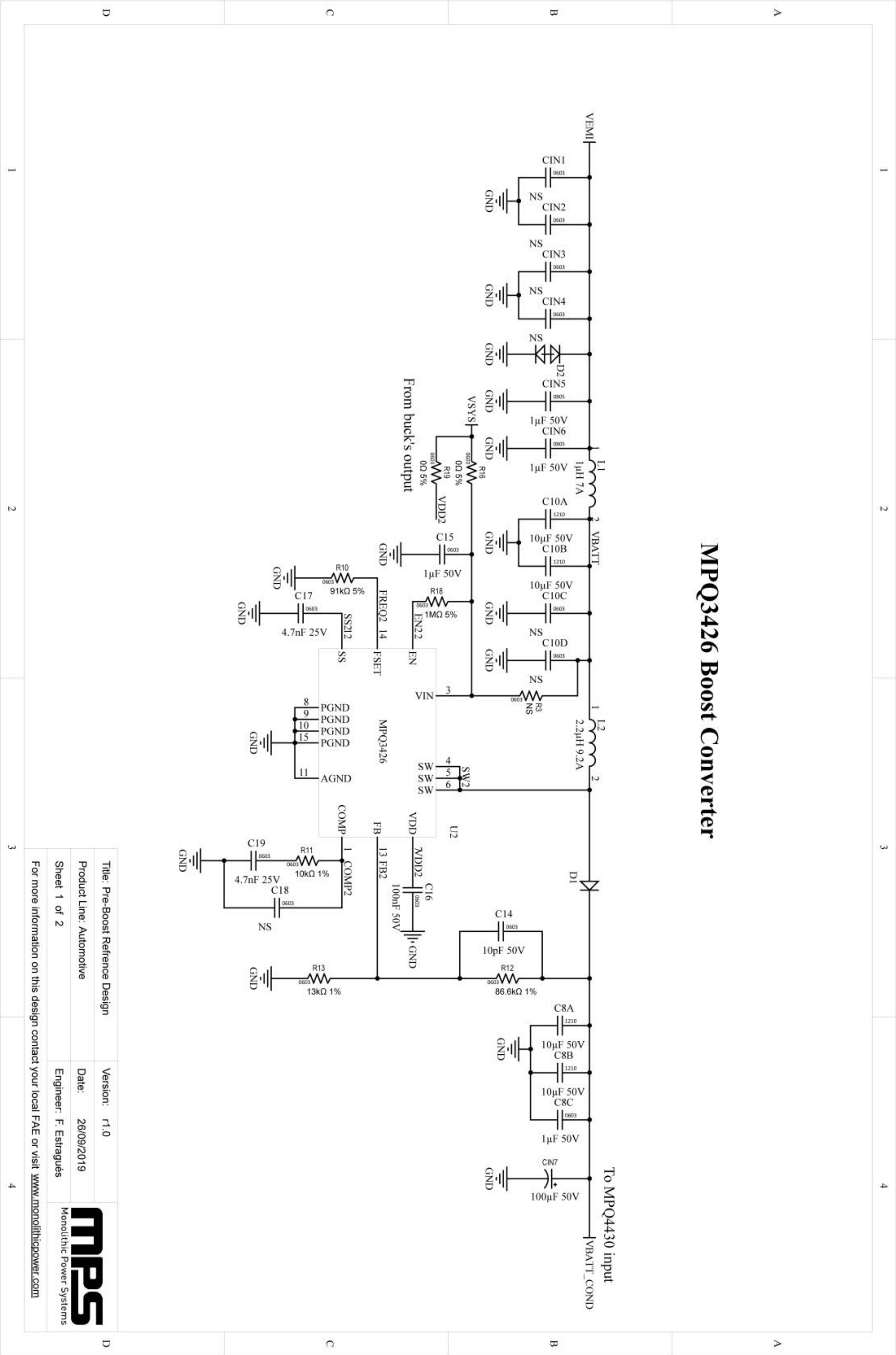


Figure 3: MPQ3426 Pre-Boost Schematic Page 1

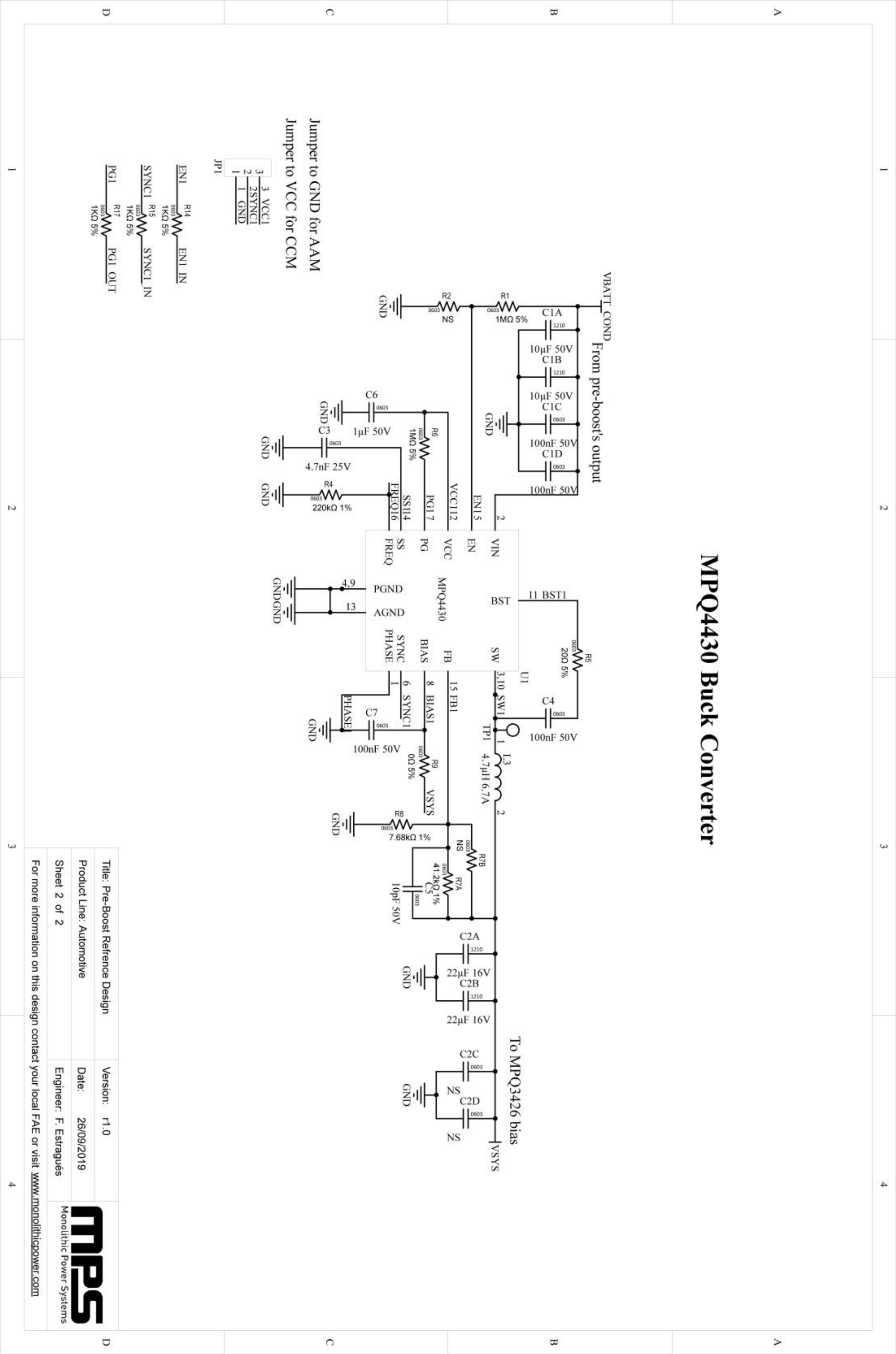


Figure 4: MPQ3426 Pre-Boost Schematic Page 2

3.10 BOM

Table 4: MPQ3426 Pre-Boost Bill of Materials

Designator	Qty	Value	Package	Part Number	Manufacturer
C1A, C1B, C8A, C8B, C10A, C10B	6	10µF, 50V	1210	CGA6P3X7S1H106K250AE	TDK
C1C, C1D, C4, C7, C16	5	100nF, 50V	0603	CC0603KRX7R9BB104	Yageo
C2A, C2B	2	22µF, 16V	1210	CGA6P1X7R1C226M250AC	TDK
C3, C17, C19	3	4.7nF, 25V	0603	C0603C472J3RACTU	KEMET
C5, C14	2	10pF, 50V	0603	CC0603JRNPO9BN100	Yageo
C6, C8C, C15	3	1µF, 50V	0603	06035C104K4T4A	Kyocera AVX
CIN5, CIN6	2	1µF, 50V	0805	GCM21BR71H105KA03L	Murata
CIN7	1	100µF, 50V	7mm	EEE-FTH101XAP	Panasonic
D1	1	V3PAL45HM3_A/I	DO-221BC	V3PAL45HM3_A/I	Vishay Semiconductors
D2	1	SMBJ22AHE3/5B	SMB	SMBJ22AHE3/5B	Vishay Semiconductors
L1	1	1µH, 7A	4020	MPIA4020V2-1R0-R	Eaton
L2	1	2.2µH, 9.2A	5030	XAL5030-222MEC	Coilcraft
L3	1	4.7µH, 6.7A	5030	XAL5030-472MEB	Coilcraft
R1, R6, R18	3	1MΩ/5%	0603	RC0603JR-071ML	Yageo
R4	1	220kΩ/1%	0603	ERJ-3EKF2203V	Panasonic
R5	1	20Ω/5%	0603	ERJ-3GEYJ200V	Panasonic
R7A	1	41.2kΩ, 1%	0603	ERJ-3EKF4122V	Panasonic
R8	1	7.68kΩ, 1%	0603	ERJ-3EKF7681V	Panasonic
R9, R16, R19	3	0Ω/5%	0603	AC0603FR-070RL	Yageo
R10	1	91kΩ/5%	0603	RC0603JR-0791KL	Yageo
R11	1	10kΩ/1%	0603	ERJ-3EKF1002V	Panasonic
R12	1	86.6kΩ/1%	0603	ERJ-3EKF8662V	Panasonic
R13	1	13kΩ/1%	0603	ERJ-3EKF1302V	Panasonic
R14, R15, R17	3	1kΩ/5%	0603	RC0603JR-071KL	Yageo
U1	1	MPQ4430	QFN-16	MPQ4430GLE-AEC1	MPS
U2	1	MPQ3426	QFN-14	MPQ3426DLE-AEC1	MPS

3.11 Recommended PCB Layout

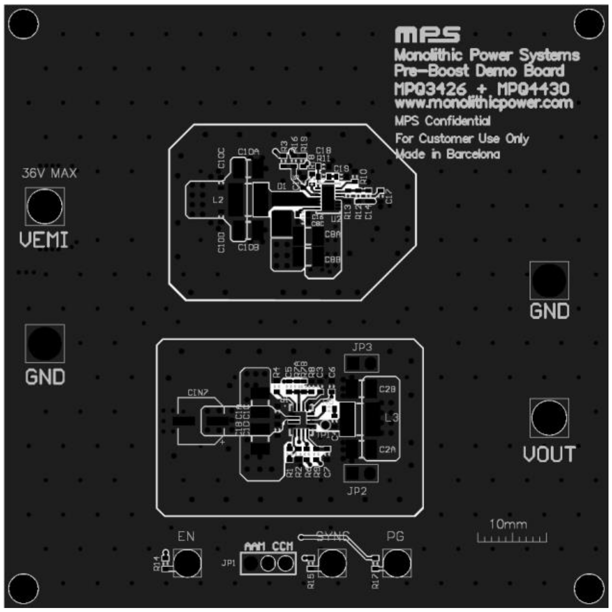


Figure 5: PCB Layer 1

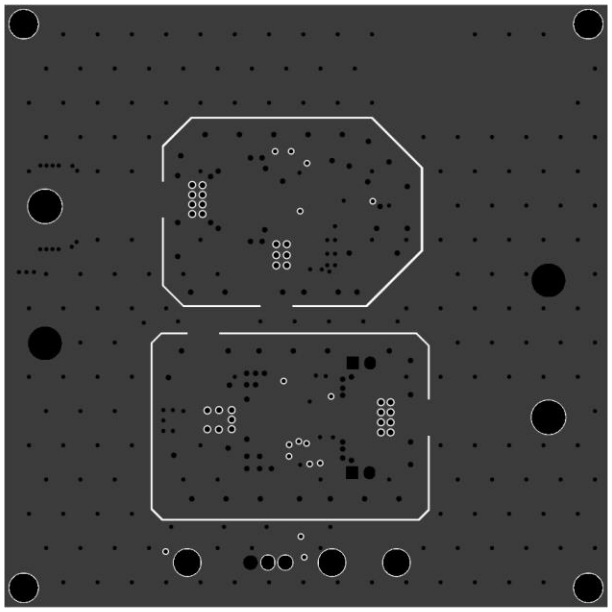


Figure 6: PCB Layer 2

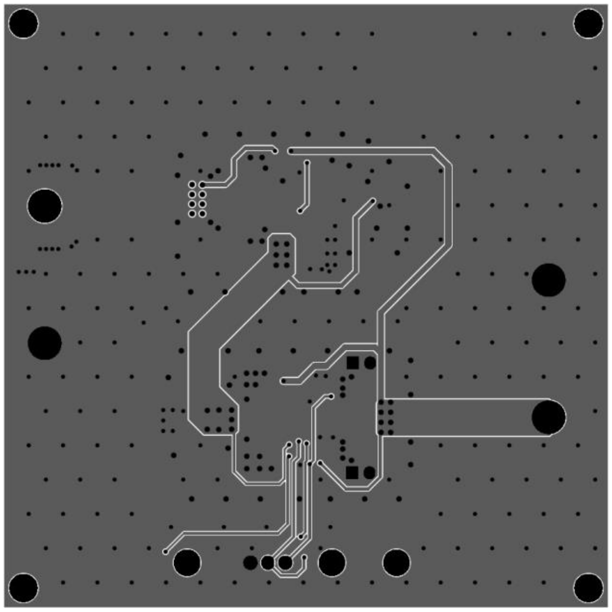


Figure 7: PCB Layer 3

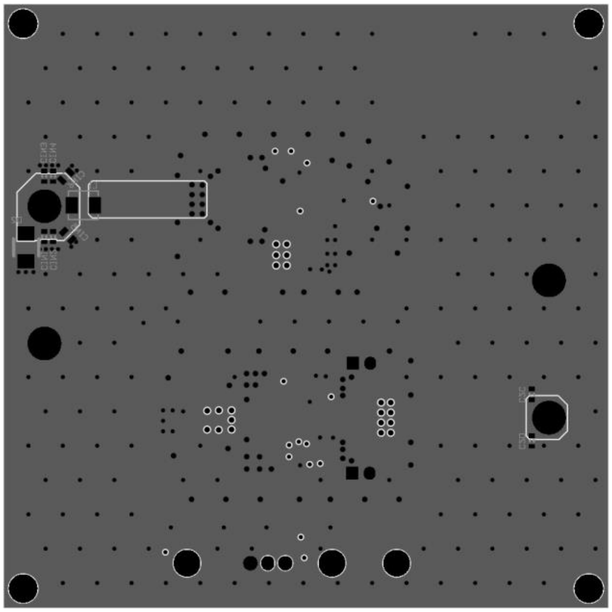


Figure 8: PCB Layer 4

3.12 PCB Layout Guidelines for the MPQ4430

1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Cut the PGND plane around the input capacitors and the IC to reduce the amount of noise that spreads to other traces. Connect PGND to the reference GND through vias.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to the VIN and PGND pins as possible to minimize EMI.

5. Place the VCC capacitor as close to VCC and GND as possible.
6. Route SW and BST away from sensitive areas, such as FB.
7. Place the feedback resistors close to the chip to ensure that the trace that connects to FB is as short as possible.
8. Use multiple vias to connect the GND planes to the internal layers.
9. Avoid placing non-GND vias too close together so that GND copper cannot flood between them.
10. Place an output capacitor on each side of the inductor to shield some of the noise that it emits.

3.13 PCB Layout Guidelines for the MPQ3426

1. Place symmetric input capacitors close to the inductor.
2. Cut the PGND plane around the output capacitors and the IC to reduce the amount of noise that spreads to other traces. Connect PGND to the reference GND through vias.
3. Ensure that the high-current paths at GND and SW have short, direct, and wide traces.
4. Keep the path between L1, D1, and C_{OUT} as short as possible.
5. Place the ceramic output capacitors, especially the small package size (0603) output capacitor, as close to the diode’s cathode and the IC’s PGND pins as possible to minimize EMI.
6. Place the VDD capacitor as close to VDD and GND as possible.
7. Place the VIN capacitor as close to VIN and GND as possible.
8. Route SW away from sensitive areas, such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the GND planes to the internal layers.
11. Avoid placing non-GND vias too close together so that GND copper cannot flood between them.

4 Test Results

4.1 Efficiency

V_{BATT} = 12V, V_{SYS} = 5V, L_{BOOST} = 2.2µH, L_{BUCK} = 4.7µH, T_A = 25°C, unless otherwise noted.

With input filter, protection diode, and pre-boost.

Figure 9: Efficiency vs. Load Current

AAM mode

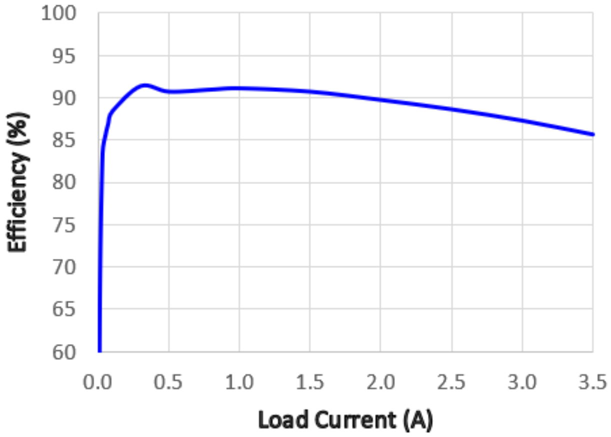
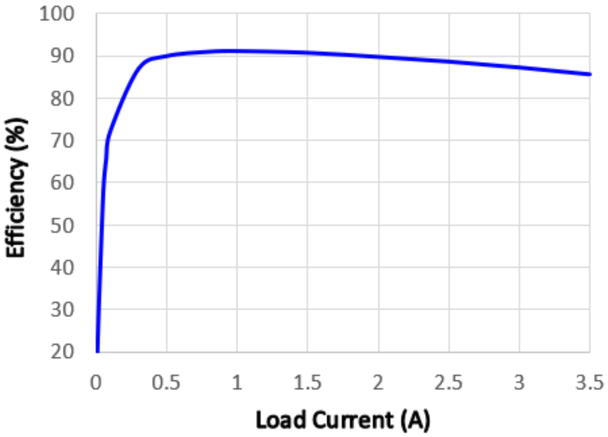


Figure 10: Efficiency vs. Load Current

CCM mode



4.2 Time-Domain Waveforms

V_{BATT} = 12V, V_{SYS} = 5V, L_{BOOST} = 2.2µH, L_{BUCK} = 4.7µH, T_A = 25°C, unless otherwise noted.

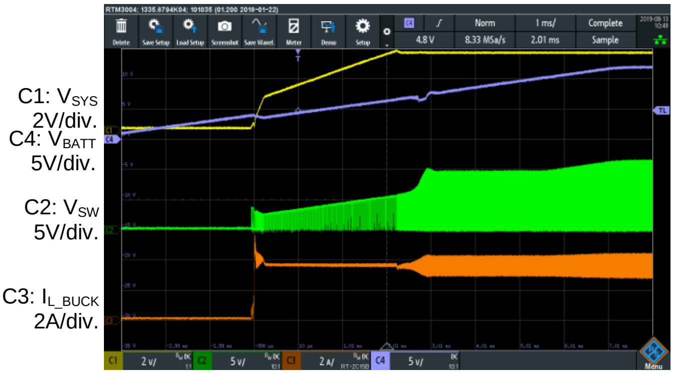
Figure 115: Steady State

I_{SYS} = 3.5A, AAM mode

2µs/div.

Figure 126: Start-Up through V_{BATT}

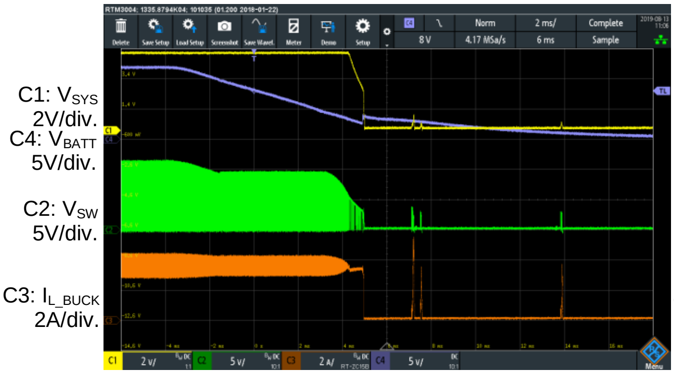
I_{SYS} = 3.5A, AAM mode



1ms/div.

Figure 137: Shutdown through V_{BATT}

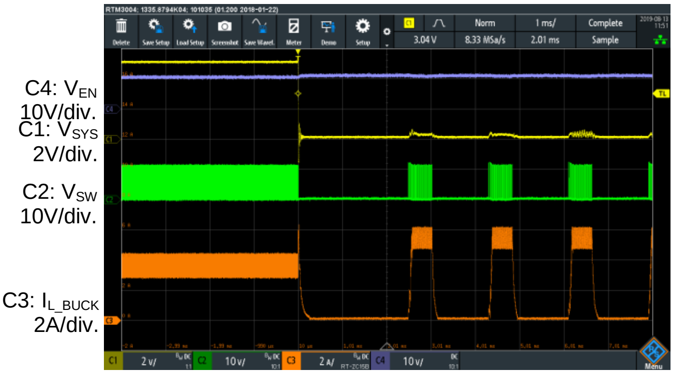
I_{SYS} = 3.5A



2ms/div.

Figure 148: SCP Entry

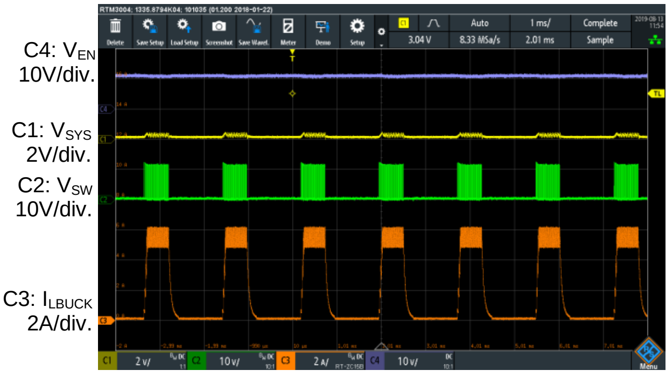
I_{SYS} = 3.5A to short circuit



1ms/div.

Figure 159: SCP Steady State

Load short-circuited



1ms/div.

Figure 1610: Load Transient

I_{SYS} = 1.75A to 3.5A, 2A/µs

200µs/div.

Figure 1711: Cold-Crank Transient Voltage

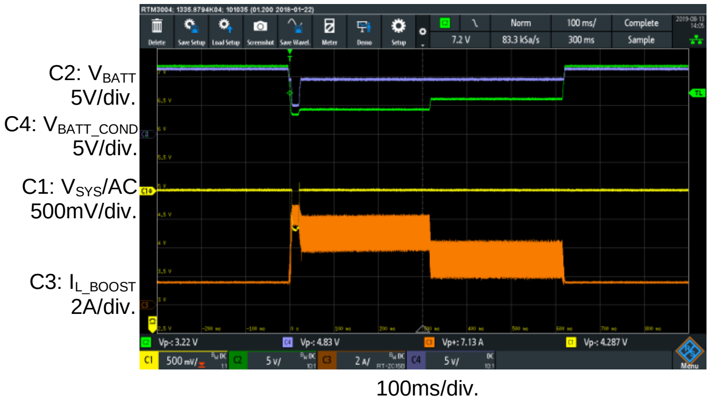
I_{SYS} = 2A, AAM mode

Figure 1812: Cold-Crank Transient Voltage

I_{SYS} = 2A, AAM mode

Figure 1913: Cold-Crank Transient Voltage

I_{SYS} = 3A, AAM mode



4.3 Thermal Measurements

V_{BATT} = 12V, V_{SYS} = 5V, I_{SYS} = 3.5A, L_{BOOST} = 2.2µH, L_{BUCK} = 4.7µH, T_A = 25°C, unless otherwise noted.

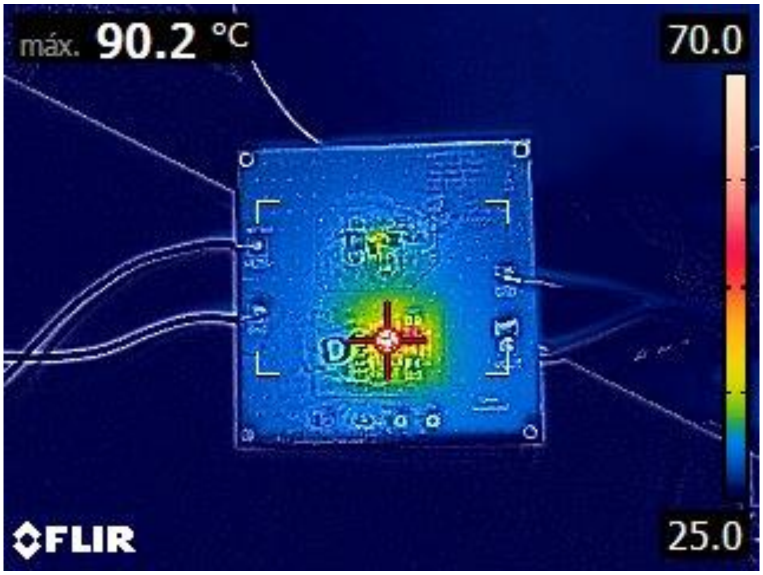


Figure 2014: Thermal Image in Steady State at Maximum Load

4.4 EMC Measurements

V_{BATT} = 12V, V_{SYS} = 3.3V, L_{BUCK} = 4.7µH, C_{OUT} = 44µF, f_{SW} = 400kHz, T_A = 25°C.

Figure 2115: CISPR25 Class 5 Conducted Emissions

150kHz to 108MHz

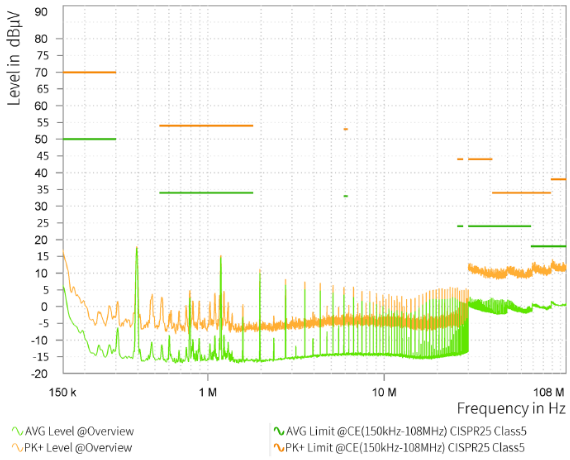
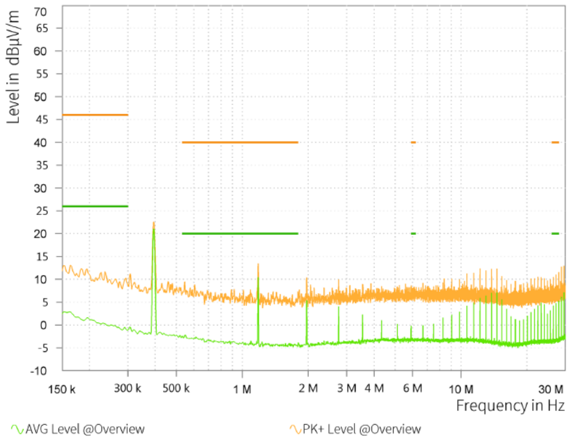


Figure 2216: CISPR25 Class 5 Radiated Emissions

150kHz to 30MHz



5 Start-Up

1. Preset the power supply to 12V. The evaluation board will tolerate up to 36V (load dump transient). Be aware that electronic loads represent a negative impedance to the regulator, and will trigger hiccup mode if set to too high of a current.
2. Turn off the power supply. If long cables are used between the source and the EVB (>0.5m), a damping electrolytic capacitor should be placed at the input terminals, especially when V_{IN} is greater than 24V.
3. Connect the power supply terminals to:
    a) Positive (+): VEMI
    b) Negative (-): GND
4. Connect the load to:
    a) Positive (+): VOUT
    b) Negative (-): GND
5. Turn the power supply on after making the connections.
6. To use the enable function, apply a digital input to the EN pin. Drive EN above 1.05V to turn the regulator on; drive EN below 0.93V to turn it off.
7. The oscillating frequency of the MPQ4430 can be programmed by an external resistor (R4). Calculate the value for this resistor with Equation (6):

$$R_4(k\Omega) = \frac{170000}{f_{SW}{}^{1.11}(kHz)} \tag{6}$$

8. To use the SYNC function, apply a 350kHz to 2.5MHz clock to the SYNC pin to synchronize the internal oscillator frequency to the external clock. The external clock frequency should be at least 250kHz higher than the one set by R4. The SYNC pin can also be used to select between forced CCM mode and AAM mode. To choose forced CCM mode, drive it high before the chip starts. To choose AAM mode, drive it low or leave it floating.
9. The system output voltage is set by the external resistor divider. The feedback resistor (R7) also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R7 to be about 40kΩ. R8 can then be calculated with Equation (7):

$$R_8(\Omega) = \frac{R_7(\Omega)}{\frac{V_{OUT}}{0.8V} - 1} \tag{7}$$

Where R7B can be used to quickly modify the output voltage by soldering the suited resistor in parallel to R7A.

Table 5 lists the recommended feedback resistor values for common output voltages.

Table 5: Recommended FB Resistor Values

V_{OUT} (V)	R7 (kΩ)	R8 (kΩ)
1.8	41.2 (1%)	33 (1%)
2.5	41.2 (1%)	19.6 (1%)
3.3	41.2 (1%)	13 (1%)
5	41.2 (1%)	7.68 (1%)

10. To place the boost converter’s protection diode, make a cut in the exposed SW trace between pins 4, 5, and 6 of the MPQ3426 and D1’s anode. Then solder a diode on top of it, with its cathode pointing toward the MPQ3426.

6 Testing Cold-Crank Transients

The board's response to cold-crank transients can be tested using specialized equipment. If the necessary equipment is not available, there are other ways to test its response.

6.1 Testing Cold-Crank Transients with a Programmable Power Supply

When using a programmable power supply, a voltage profile can be programmed to emulate a cold-crank transient. Figure 23 shows an example of a typical voltage profile for this test.

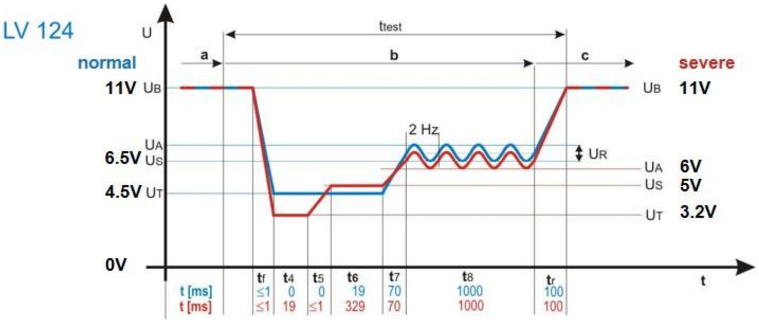


Figure 2317: Cold-Crank Voltage Profile

From this profile, the relevant data that will be extracted from the test is the response from t_f to t_7. The oscillation in t_8 can be omitted to make things easier.

6.2 Testing Cold-Crank Transients Using Two Power Supplies

1. Connect a power supply to VEMI that will supply 12V to the board.
2. Take a high-current diode and solder its cathode to VEMI.
3. Connect a secondary power supply (that can provide 8A) to the diode's anode, and set its output voltage so that the desired cold-crank voltage is measured in the diode's cathode.
4. Power on both supplies. The board should start working normally.
5. Power off the main 12V power supply. The voltage should decrease to the cold-crank voltage previously set. The slew rate of the voltage decrease can be adjusted using capacitors.

7 Disclaimer

Monolithic Power Systems (MPS) reserves the right to make changes to its products and to discontinue products without notice. The applications information, schematic diagrams, and other reference information included herein is provided as a design aid only and therefore provided as-is. MPS makes no warranties with respect to this information and disclaims any implied warranties of merchantability or non-infringement of third-party intellectual property rights.

MPS cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in an MPS product. No circuit patent licenses are implied.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage (“Critical Applications”).

MPS PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE SUPPORT APPLICATIONS, DEVICES OR SYSTEMS, OR OTHER CRITICAL APPLICATIONS.

Inclusion of MPS products in critical applications is understood to be fully at the risk of the customer.

Questions concerning potential risk applications should be directed to MPS.

MPS semiconductors are typically used in power supplies in which high voltages are present during operation. High-voltage safety precautions should be observed in design and operation to minimize the chance of injury.