Feasibility and Accuracy Analysis of Input Power Estimation for Boost PFC Converters without Additional Sensors

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***Abstract*—The most commonly used boost power factor correction (PFC) converters in the industry only sample input voltage, output voltage, and inductor current, and control the switching frequency and duty cycle. This paper discusses the feasibility of estimating real-time input power based on this basic and limited information in a boost converter. The influences of major non-ideal effects, including turn-on delay, turn-off delay, and current distortion caused by the parasitic oscillation in discontinuous conduction mode (DCM), are analyzed in detail, and an algorithm for accurate estimation is proposed accordingly. In contrast to the power metering implemented by input voltage and current sensors, this study provides an approach to monitor input power without introducing any additional system complexity, cost, or power loss. A 400W prototype has been built based on the HR1211GY digital PFC and LLC combo controller, and the feasibility and the accuracy of the theoretical analysis have been validated by experimental results.**

Keywords—PFC, power metering, multi-mode operation, parasitic effect

I. INTRODUCTION

PFC converters are widely used in the industry to provide DC output voltage from the main lines, and to maintain a high power factor (PF) and low current distortion at the same time. In some of these applications, such as telecom, server, workstation power supplies, and plug-in electric vehicles, the active input power needs to be measured in real time in order to monitor energy consumption, as well as to improve system efficiency and achieve intelligent system management. Dedicated voltage and current sensors are commonly adopted in front of the bridge rectifier to implement this power metering function. However, regardless of whether the additional sensors are shunt-based or Hall-effect based, they all add considerable cost, complexity, and power consumption to these power supplies.

According to the basic modeling of boost PFC converters[1], PFC controllers usually samples the input voltage, the output voltage, and the inductor current to control the switching frequency and the duty cycle. In this way, the output power is regulated and the input current is simultaneously shaped to achieved high PF and low total harmonic distortion (THD). Therefore, PFC controllers typically have the raw information that can be used for power estimation. Given that digital controllers have been widely adopted in the industry[2, 3, 4], this information is commonly accessible in real time through digital communication interfaces from PFC controllers. This creates a possible approach to monitor input power via indirect calculation instead of the conventional power metering implemented by additional voltage and current sensors.

Several key factors must be taken into consideration in order to get an estimation of the actual input power with acceptable accuracy. First, the passive components on the input, such as electro-magnetic compliance (EMC) components and the bridge rectifiers, make a difference between the power regulated in the boost converter and the actual input current. However, this is not the main problem, as the extra power introduced by passive components is straightforward to be modeled[5]. In other words, it can be directly calculated based on the designed circuit parameters, especially considering that high-frequency distortions are not the primary concern for the fundamental power metering requirements. However, some non-ideal effects introduce more complicated influences on the accuracy of inductor current estimation. The turn-on and turn-off delays deviate the actual inductor current and the switching frequency from the control targets. The parasitic oscillation in DCM introduces another variable to the inductor current. In addition, these influences all vary with operating conditions. Most practical applications have adopted a multi-mode control scheme[6, 7, 8, 9], due to its superior light-load performance over a conventional critical mode (CrM) control scheme or fixed-frequency continuous conduction mode (CCM) control scheme. In order to accurately estimate power, those non-ideal effects must be considered under various operating conditions. Based on the observability of the PFC model[10], the PFC control scheme can be implemented even without sensing the inductor current[11, 12]. Therefore, the current error introduced by the delays can also be compensated based on proper modeling of the other system states and parameters, e.g. the input and output voltage, and the PFC inductor. On the other hand, the parasitic oscillation in DCM can be modeled in the time domain[13, 14], based on which the corresponding error in each switching can also be deduced.

In this paper, the influences of these effects are analyzed in detail based on a multi-mode PFC control scheme, and an improved, easy-to-implement algorithm for input power estimation is proposed to achieve accurate active power estimation across a wide operating range. A prototype with 400W of rated power has been built based on the HR1211GY, a digital PFC and LLC combo controller. The controller implements a multi-mode PFC control scheme that smoothly switches between CCM and DCM operation. With the experimental results based on such a mainstream control scheme in the industry, the feasibility and the universal

applicability of the proposed estimation approach was verified.

II. Multi-Mode PFC Control Scheme

A boost converter with typical multi-mode PFC control scheme, as shown in Fig.1, enables smooth transition between CCM and DCM to achieve high efficiency across a wide operating range. Operating in CCM can minimize both the peak current and RMS current under heavy-load conditions, which helps reduce the size of the magnetic components and makes it suitable for higher-power applications with good efficiency. Operating in DCM with a reduced switching frequency can minimize switching loss to achieve better power saving under light-load conditions. Furthermore, the hybrid operation of CCM and DCM under medium-load conditions optimizes the balance between conduction loss and switching loss to achieve better average efficiency. This hybrid is the emerging control scheme, and has been well recognized in the industry recently, because both full-load efficiency and light-load efficiency are equally important for most practical applications.

The control scheme, as shown in Fig.1, samples the output voltage V_O and compares it to the output reference V_{O_REF} to derive the internal compensation state $v_{COMP}(n)$ through the PI loop regulator. Accordingly, an inner current loop generates the reference for the inductor current control, as in

$$i_{REF}(n)=\frac{v_{IN}(n)v_{COMP}(n)}{V_{IN\_PK}^2} \tag{1}$$

where $v_{IN}(n)$ is the sampled instant input voltage, and V_{IN_PK} is the peak voltage in a line cycle.

By comparing $2i_{REF}(n)$ to the inductor peak current $i_{PK}(n)$, which can be sampled right before the MOSFET turns off during each switching cycle, the control scheme is able to determine whether the converter should be operating in CCM or DCM. If it operates in CCM, the switching frequency f_S is regulated at the maximum switching frequency f_{S_MAX} as a steady state. And in order to keep the average current in every switching cycle equal to $i_{REF}(n)$, the MOSFET always turns on when the inductor current i_L decreases to the targeted valley i_{Vally}, as in

$$i_{Vally}(n)=2i_{REF}(n)-i_{PK}(n) \tag{2}$$

At the same time, in order to guarantee the magnetizing balance of the PFC inductor, the on-time $T_{ON}(n)$ is controlled as

$$T_{ON}(n)=\frac{V_{O\_REF}-v_{IN}(n)}{V_{O\_REF}f_{S\_MAX}} \tag{3}$$

If it operates in DCM, the on-time is still controlled in the same way, but the switching frequency is reduced to keep the average current equal to $i_{REF}(n)$. In general, the switching frequency is controlled as

$$f_S(n)=\begin{cases} f_{S\_MAX}, & i_{PK}(n)<2i_{REF}(n),\text{CCM} \\ \dfrac{2i_{REF}(n)}{i_{PK}(n)}f_{S\_MAX}, & i_{PK}(n)\geq 2i_{REF}(n),\text{DCM} \end{cases} \tag{4}$$

In this way, the average i_L in one switching cycle is always equal to i_{REF}. Ideally, i_{REF} can be used to calculate the input power. However, as shown in the following sections, without compensating for the non-ideal effects, estimation accuracy cannot be guaranteed.

III. Current Control Error Caused by Parasitic Effects

The main parasitic effects that lead to error between the actual current and the control target in the boost converters are switching delays and current oscillation. The effects are related to converter parameters and vary with operating conditions.

In CCM, as shown in Fig.2, the error is mainly introduced via the turn-on delay T_{D_ON} and the turn-off delay T_{D_OFF}. The turn-on delay results in an undershoot below the targeted current valley, while the turn-off delay deviates the sampling point away from the actual peak point on the inductor current. The average error in one switching cycle can be calculated as

$$\begin{aligned}\left\langle \tilde{i}_{L\_CCM}(n)\right\rangle_{T_S} &= i_{CCM\_D\_ON}(n)+i_{CCM\_D\_OFF}(n) \\ &= \frac{v_{IN}(n)T_{D\_ON}}{2L}-\frac{\left[V_O-v_{IN}(n)\right]T_{D\_OFF}}{2L}\end{aligned} \tag{5}$$

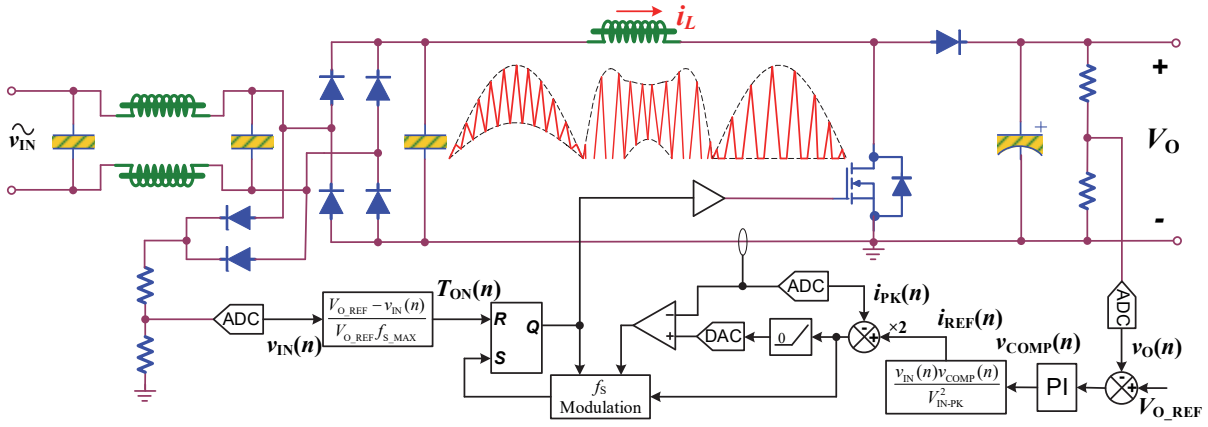


Fig. 1. *Boost converter with a multi-mode PFC control scheme.*

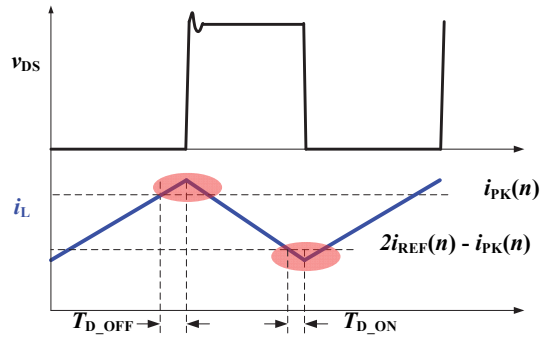


Fig. 2. *Main causes of current error in CCM*

where L is inductance of the PFC inductor.

In DCM, as shown in Fig.3, the inductor current always starts from zero, so the turn-on delay does not affect the inductor current anymore. However, the turn-off delay still has a similar effect on the peak sampling of the inductor current. The error model is different from that in CCM, because it has influence on both the peak and duty of the current. The average error in one switching cycle caused by the turn-off delay in DCM can be obtained as

$$\left\langle \tilde{i}_{L\_DCM\_D}(n) \right\rangle_{T_S} = \frac{v_{IN}(n) T_{D\_OFF} f_S(n)}{L} \left[\frac{1}{f_{S\_MAX}} + \frac{V_O T_{D\_OFF}}{2\left[V_O - v_{IN}(n)\right]} \right] \tag{6}$$

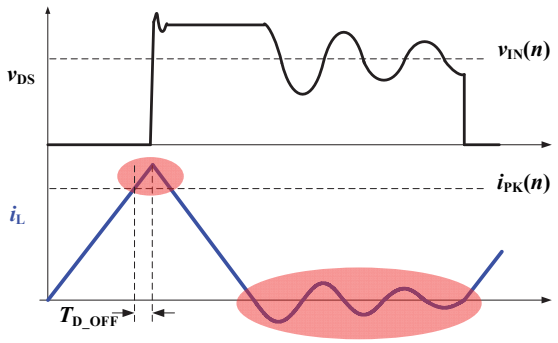
In addition, DCM oscillation is another main cause of the current error. When the PFC inductor current drops to zero, the inductor oscillates with the equivalent parasitic capacitance of the MOSFET and the freewheeling diode. The initial states of the oscillation are with the zero inductor current and the drain-source voltage v_{DS} at V_O. Due to the clamping effect of the body diode of the MOSFET, there are two possible scenarios for the oscillation, depending on whether v_{DS} oscillates to zero.

When v_{IN} exceeds V_O / 2, as shown in Fig.3 (a), the oscillation runs in a free damping way without being clamped on any point. Therefore, the average oscillating current in one switching cycle is

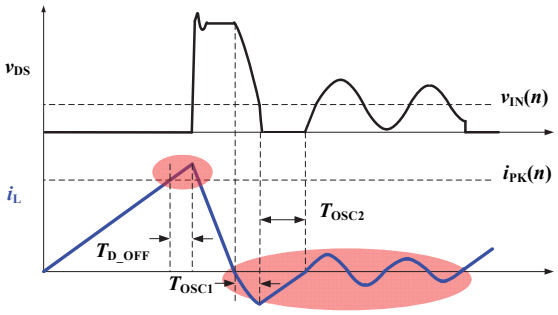
$$\left\langle \tilde{i}_{L\_DCM\_OF}(n) \right\rangle_{T_S} = f_S \int_0^{\frac{1}{f_S} - \frac{1}{f_{S\_MAX}}} \frac{v_{IN}(n) - V_O}{L\omega_P} e^{-\zeta t} \sin(\omega_P t) dt \tag{7}$$

Where ω_P and ζ are the angular frequency and the damping coefficient of the oscillation.

When v_{IN} is below V_O / 2, as shown in Fig.3 (b), the oscillation is clamped by the body diode when v_{DS} drops to zero. During the clamping period, the inductor current ramps up with a constant slew rate until the current polarity is reversed again. Then, free oscillation resumes. Therefore, the oscillation in this scenario is composed of three sections, and the durations of the first two can be respectively calculated as



(a) $2v_{IN}(n) \geqslant v_O$



(b) $2v_{IN}(n) < v_O$

Fig. 3. *Main causes of current error in DCM*

$$T_{OSC1} = \frac{1}{\omega_P} \arccos \frac{v_{IN}(n)}{v_{IN}(n) - V_O} \tag{8}$$

$$T_{OSC2} = \frac{\sqrt{V_O\left(V_O - 2v_{IN}(n)\right)}}{v_{IN}(n)\omega_P} \tag{9}$$

Accordingly, the average oscillating current in one switching cycle can be obtained as

$$\begin{aligned} \left\langle \tilde{i}_{L\_DCM\_OC}(n) \right\rangle_{T_S} = & \\ & f_S \int_0^{T_{OSC1}} \frac{v_{IN}(n) - V_O}{L\omega_P} e^{-\zeta t} \sin(\omega_P t) dt + \\ & f_S \int_{T_{OSC1}}^{T_{OSC1}+T_{OSC2}} \left[\frac{v_{IN}(n)}{L} t - \frac{\sqrt{V_O\left(V_O - 2v_{IN}(n)\right)}}{L\omega_P} \right] dt + \\ & f_S \int_{T_{OSC1}+T_{OSC2}}^{\frac{1}{f_S} - \frac{1}{f_{S\_MAX}}} \frac{v_{IN}(n)}{L\omega_P} e^{-\zeta t} \sin\left[\omega_P (t - T_{OSC1} + T_{OSC2})\right] dt \end{aligned} \tag{10}$$

Based on this, the general current error in DCM is

$$\left\langle \tilde{i}_{L\_DCM}(n) \right\rangle_{T_S} = \begin{cases} \left\langle \tilde{i}_{L\_DCM\_D}(n) \right\rangle_{T_S} + \left\langle \tilde{i}_{L\_DCM\_OF}(n) \right\rangle_{T_S}, v_{IN}(n) \geq \dfrac{V_O}{2} \\ \left\langle \tilde{i}_{L\_DCM\_D}(n) \right\rangle_{T_S} + \left\langle \tilde{i}_{L\_DCM\_OC}(n) \right\rangle_{T_S}, v_{IN}(n) < \dfrac{V_O}{2} \end{cases} \tag{11}$$

The current error caused by the parasitic effects in each operating condition is formulated in (5) through (11). However, in order to make a universal current error compensation algorithm for practical application use, the boundaries between each condition must also be carried out. Assuming the transition angular between CCM and DCM in the first quarter of an AC input line cycle is θ_T, the input voltage and the reference current at the boundary conduction are

$$\begin{cases} v_{IN}\big|_{Trans.} = V_{IN\_PK}\sin\theta_T \\ i_{REF}\big|_{Trans.} = I_{REF\_PK}\sin\theta_T \end{cases}, 0 \le \theta_T \le \frac{\pi}{2} \tag{12}$$

where I_{REF_PK} is the peak reference current in a complete line cycle, and can be derived from v_{COMP} based on (1). The transition angulars in each quarter of an AC input line cycle are symmetrical to each other.

Since the inductor current is also in boundary conduction at the transition point, there is equation

$$2i_{REF}\big|_{Trans.} = \frac{v_{IN}\big|_{Trans.} \cdot T_{ON}(n)}{L} \tag{13}$$

Based on (2), (12), and (13), it can be deduced that

$$\theta_T = \begin{cases} 0, I_{REF\_PK} > \dfrac{V_{IN\_PK}}{2Lf_{S\_MAX}} \\ \left(\arcsin\dfrac{V_O(V_{IN\_PK} - 2I_{REF\_PK}Lf_{S\_MAX})}{V_{IN\_PK}^2}, \right. \\ \left. \dfrac{V_{IN\_PK}}{2Lf_{S\_MAX}} < I_{REF\_PK} < \dfrac{V_O V_{IN\_PK} - V_{IN\_PK}^2}{2V_O Lf_{S\_MAX}} \right) \\ \dfrac{\pi}{2}, I_{REF\_PK} < \dfrac{V_O V_{IN\_PK} - V_{IN\_PK}^2}{2V_O Lf_{S\_MAX}} \end{cases} \tag{14}$$

Accordingly, the distribution of θ_T is plotted in Fig.4. When θ_T is equal to 0, the converter only operates in CCM. When θ_T is equal to π / 2, the converter only operates in DCM. When θ_T is between 0 and π / 2, the converter operates in both CCM and DCM during one AC input line cycle, and there is more portion of time in CCM as the load increases or the input voltage decreases.

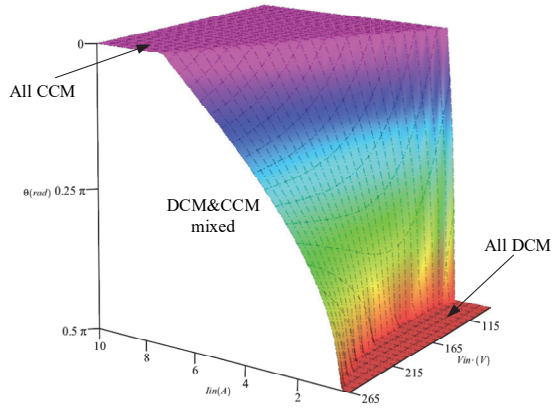


Fig. 4. *CCM and DCM distribution vs. input and load conditions*

IV. Active Input Power Estimation

The active input current can be accurately estimated by compensating the parasitic effects in various operating conditions, as shown by the analysis in Section III. In order to derive the active input power, the power loss introduced by the passive components on the input must also be addressed.

Taking the schematic illustrated in Fig.1 as a typical example, the passive components on the input of the PFC converter mainly include LC filters and bridge diodes. Considering that the reactive current flowing through the filter capacitors does not contribute to active power and that the leakage current of capacitors is small enough, the filter capacitors have little influence on the active power estimation. On the other hand, the voltage drop introduced by the bridge diodes and the parasitic resistance of the filter inductors leads to considerable power loss, and must be included in the power estimation. The input voltage in front of the passive components can be derived as

$$v_{IN}^*(t) = v_{IN}(t) + R_L i_{REF}(t) + 2V_{F\_BD} \tag{15}$$

where V_{F_BD} is the forward voltage of one bridge rectifier diode, R_L is the total equivalent resistance of all the filter inductors, $v_{IN}(t) = V_{IN\_PK}\sin\omega_L t$ is the reconstructed voltage based on the sampled input voltage $v_{IN}(n)$ in the PFC control scheme, and ω_L is the input line frequency.

Combing all the analysis above, the active input power can be estimated as

$$\begin{aligned} P_{IN} = \frac{2\omega_L}{\pi}\Big[& \int_0^{\frac{\pi}{2\omega_L}} v_{IN}^*(t) i_{REF}(t)dt + \int_0^{\frac{\theta_T}{\omega_L}} v_{IN}^*(t)\tilde{i}_{L\_DCM}(t)dt \\ & + \int_{\frac{\theta_T}{\omega_L}}^{\frac{\pi}{2\omega_L}} v_{IN}^*(t)\tilde{i}_{L\_CCM}(t)dt \Big] \end{aligned} \tag{16}$$

V. Experimental Verification

In order to verify the analysis and the proposed estimation of the input power, a 400W prototype has been built and tested. The prototype is designed and implemented based on the HR1211GY, a digital multi-mode PFC and LLC combo controller. The circuit and the control scheme of the PFC stage are the same as that shown in Fig.1, and Fig.5 shows a photo of the prototype. The specifications and key component parameters of the PFC stage include V_{IN_RMS} = 90V - 265V, f_L = 50Hz, R_L = 100mΩ, V_{F_BD} = 0.75V, V_O = 400V, f_{S_MAX} = 100kHz, L = 190μH, IPP60R099C7XKSA1 being the primary MOSFET, STPSC406D being the freewheeling diode, $\omega_P = 5.93\times10^6$rad/s, T_{D_ON} = 300ns, T_{D_OFF} = 150ns. And the other instant states required for the power estimation, including v_{COMP}, V_{IN_PK} and V_O, are all accessible through the integrated UART interface of HR1211GY in real time.

The input current and the PFC inductor current waveforms are presented below. Fig.6 shows that the PFC converter fully operates in CCM under low-line and full-load conditions. The switching frequency is fixed as f_{S_MAX}, and both the current peak and current valley are regulated in sinusoidal wave.

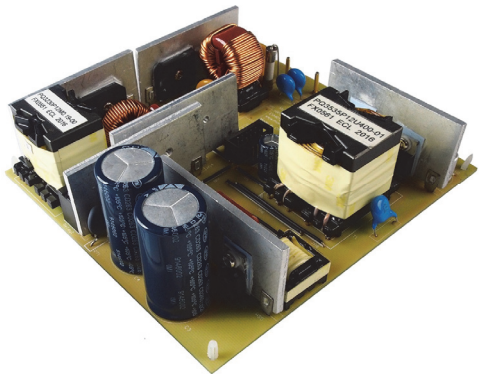


Fig. 5. *400W prototype based on the HR1211GY for the experiment*

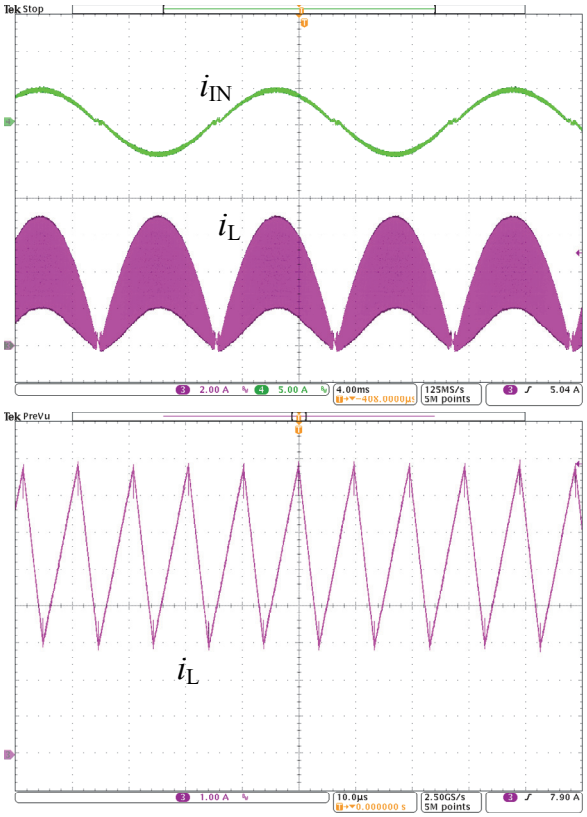


Fig. 6. *Experimental waveforms at V_{IN_rms} = 110V and P_O = 400W*

Under high-line and full load conditions, the PFC converter operates in mixed CCM and DCM, as shown in Fig.7. The waveform shows the transition between CCM and DCM in the inductor current. In this way, the peak inductor current is lower at the peak of the input line, but the switching-cycle-average of the inductor current is still regulated to be sinusoidal by the controller.

Under light-load conditions, the PFC converter fully operates in DCM, as shown in Fig.8. The switching frequency becomes lower as the load decreases.

With the proposed power estimation approach, the input power from 10% to 100% load is calculated based on the parameters of this prototype illustrated above and the instant states read from the digital controller HR1211GY. Fig.9 shows the calculated results compared to the actual measured

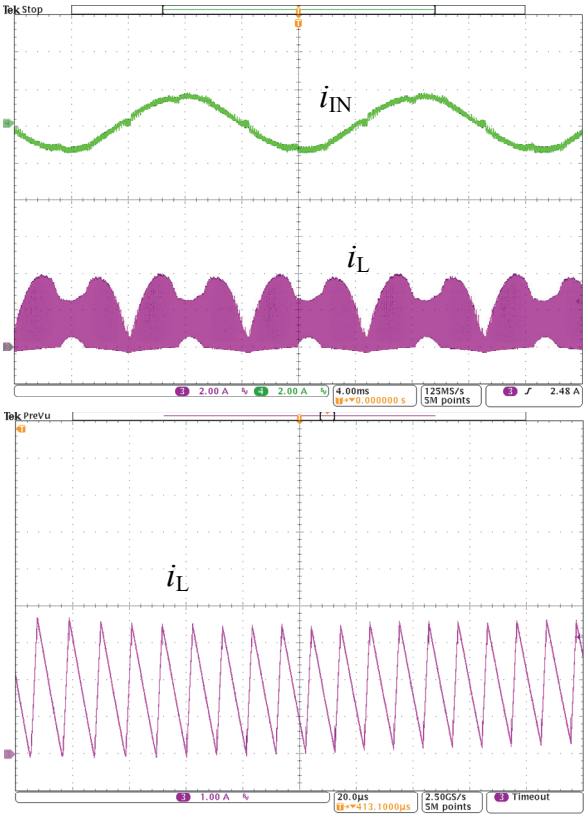


Fig. 7. *Experimental waveforms at V_{IN_rms} = 230V and P_O = 400W*

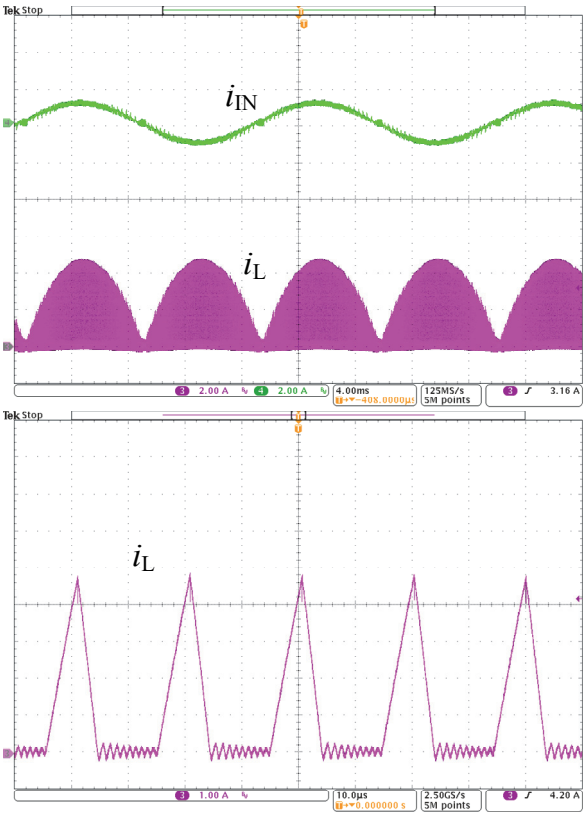
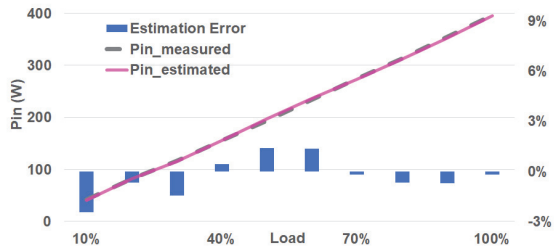


Fig. 8. *Experimental waveforms at V_{IN_rms} = 110V and P_O = 100W*

data using a WT310E power meter. It can be seen that the estimation error is smaller than 3% across a wide load range. In addition, different input conditions are covered by the same estimation algorithm.



(a) V_{IN_rms}=*110V*

(b) V_{IN_rms}=*230V*

Fig. 9. *Constrast between the calcuated input power and the measured input power*

VI. Conclusions

This paper studied the feasibility of implementing active input power estimation without any additional sensors for boost PFC converter. The analysis in this paper accounts for the influence of parasitic effects, such as turn-on and turn-off delays, DCM oscillation, transition between DCM and CCM, and active power loss on passive components. Based on the mathematical modeling of the system and parasitic effects, an algorithm for accurately estimating the input power has been proposed. It takes the characteristics of the mainstream multi-mode PFC control scheme into consideration, and is able to support a wide operating range. The proposed estimation approach has been verified by experimental results on a 400W boost PFC prototype based on the HR1211GY. As digital PFC controllers are becoming more and more popular in practical applications, this study provides a possible approach to reduce system complexity and cost, as well as to improve reliability for power supply products in the future, by implementing basic power metering functions without adding any additional sensors.

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