Stability Analysis in Time Domain

No Bode, No Problem! Ensure Stability of Automotive DC-DC Converters through Time-Based Analysis

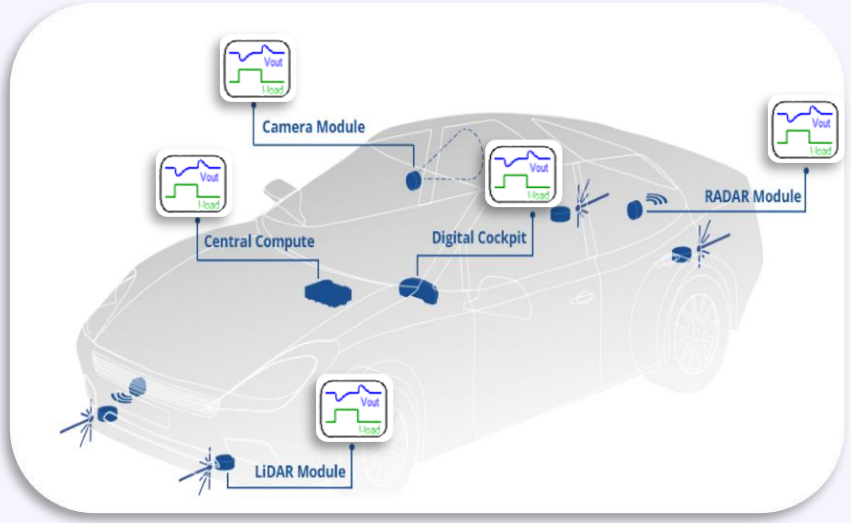
Why Load Transients Matter?

- Load Transients are critically important in Automotive System applications like **ADAS, Infotainment and powertrain control.**

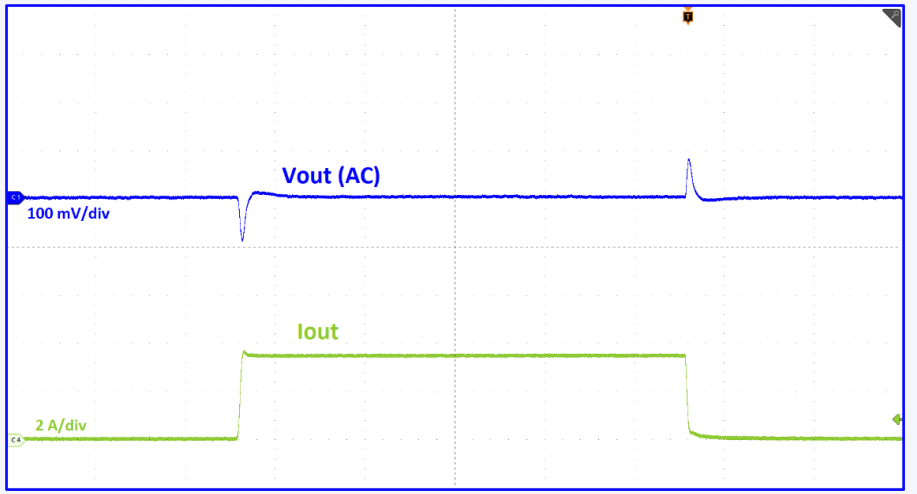
- Load Transients occur due to real-time system demands. For example: **Activation of ADAS modules, Turning on headlights, electric steering or infotainment system etc. can cause sudden current demands.**

- **Why it matters? –** If regulation isn't stable during transients, it can lead to malfunctions, data corruption, or even system resets.

Systems Designers need to ensure the DC-DC converter is stable during these dynamic load transient conditions.



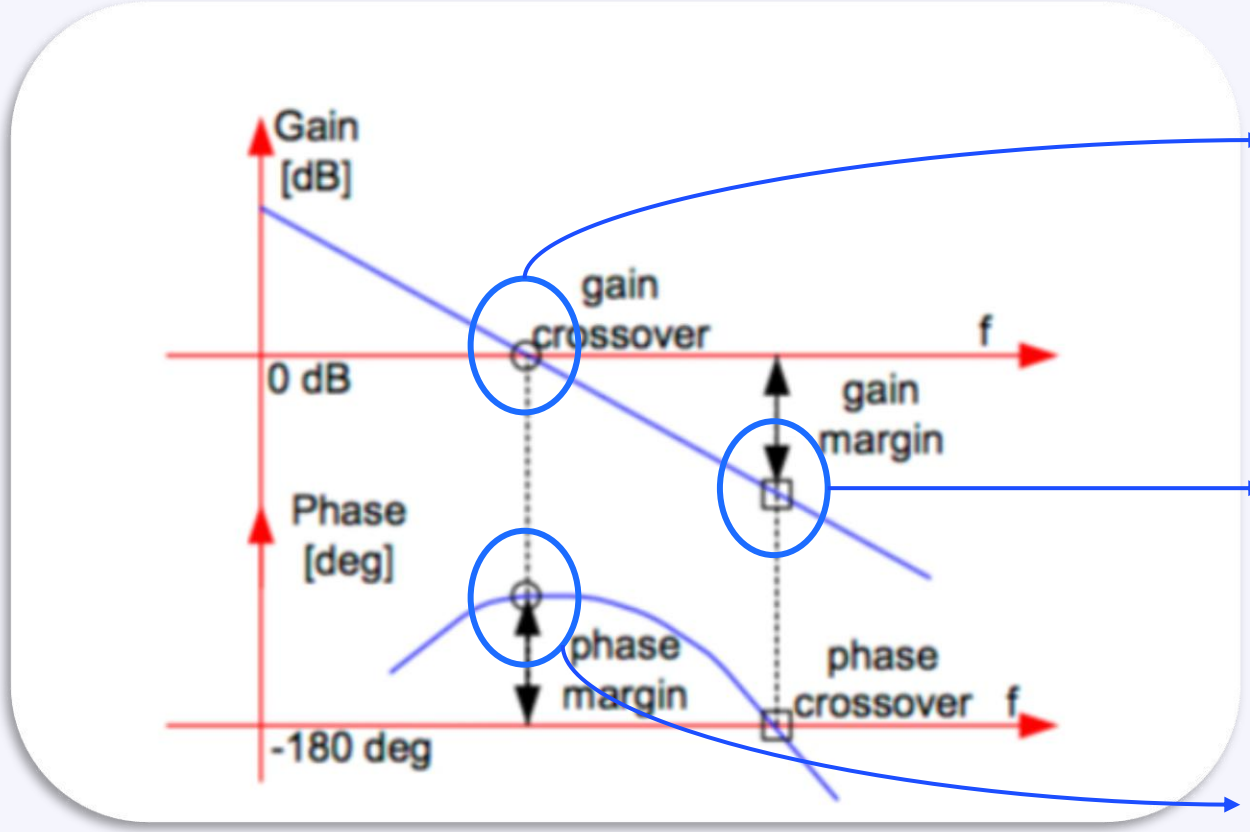
Example Load Transient Waveform



Parameters defining DC-DC converter Stability

- Control loop stability refers to the system ability to maintain a desired state despite external disturbances or changes in system parameters.

- Key parameters that define stability in DC-DC converters: **Bandwidth (Crossover Frequency), Phase Margin and Gain Margin**

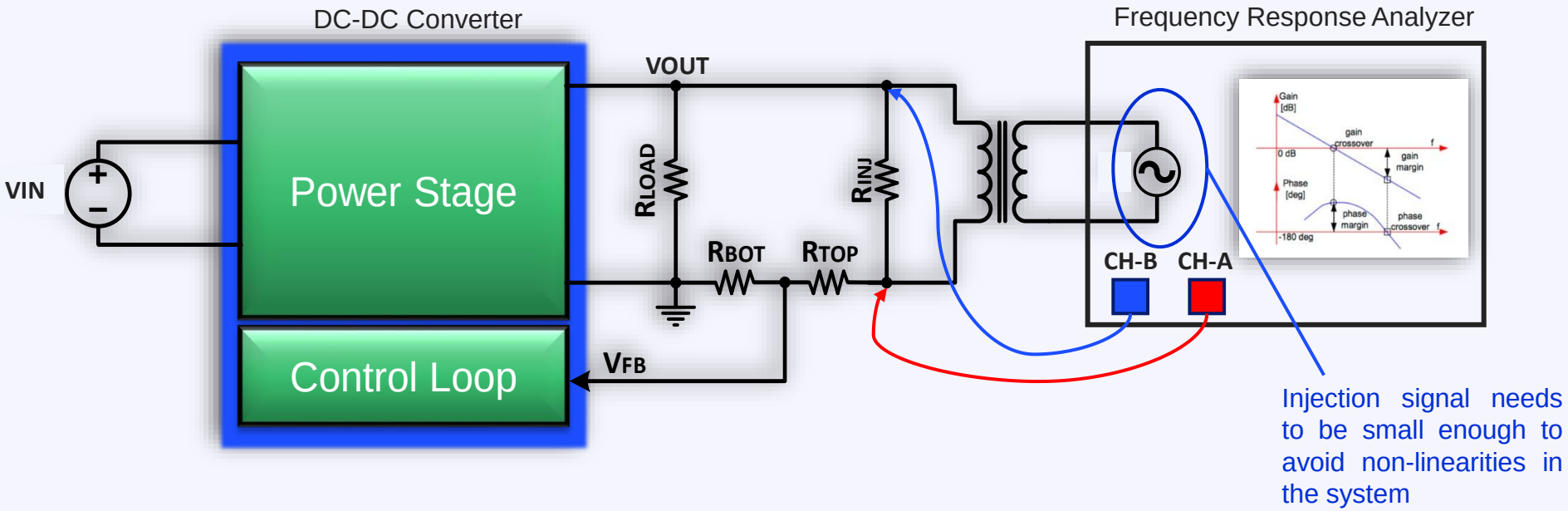


Bandwidth or cross-over frequency is frequency when the system gain = 0dB. Indicates how fast the system reacts to system transients. Bandwidth target for Automotive: ~1/10th -1/5th of switching frequency.

Gain margin is the gain of the system when the phase = 0 degrees. Indicates how much the gain of the control loop can be increased before the system becomes unstable. A typical gain margin for a stable system is lower than -10dB.

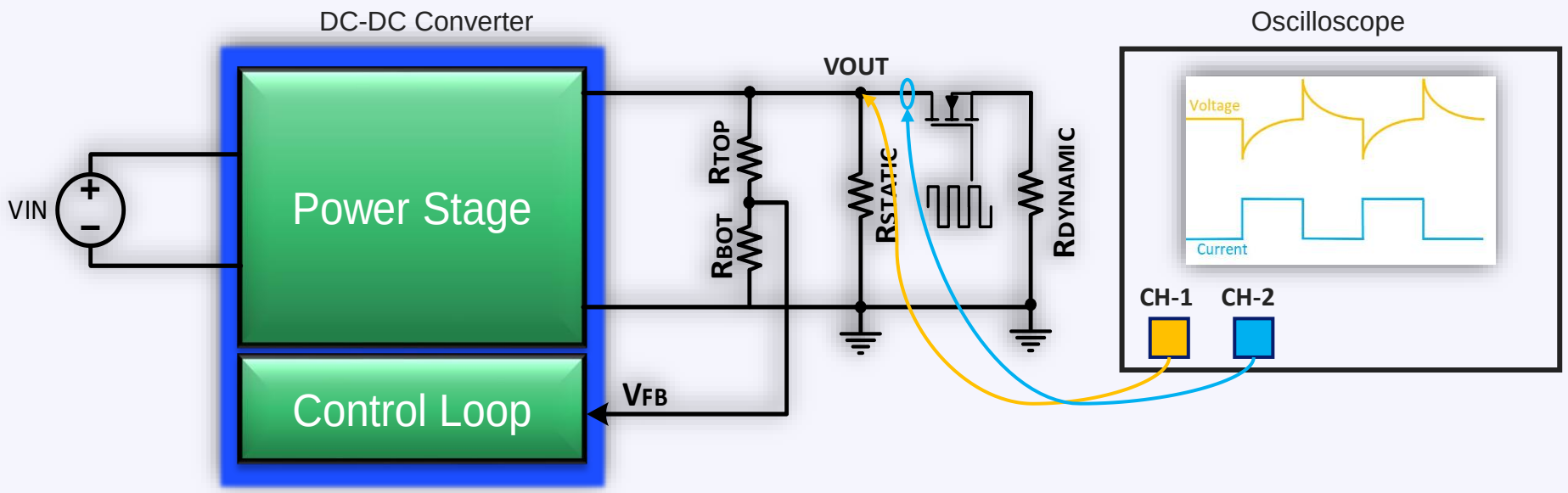
Phase margin is the phase of the system when the gain = 0dB. Indicates the stability of the system. Acceptable phase margin for Automotive applications is 45 degrees or greater.

Loop Stability Check – Frequency Domain



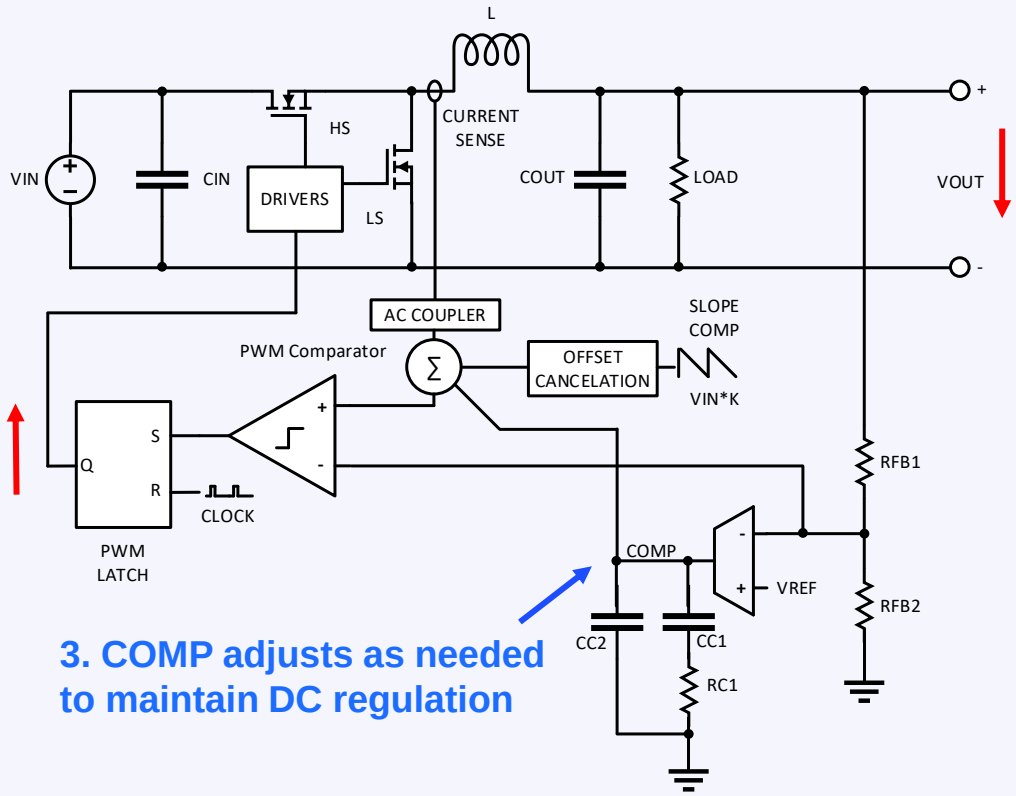
- ❑ Clear visualization of frequency response
- ❑ Easy determination of cross-over frequency and phase margin
- ❑ Prone to noise and non-linearities in the system
- ❑ Applies only to linear time-invariant systems
- ❑ Requires expensive analyzers with advanced capabilities

Loop Stability Check – Frequency Domain



- Easy and quick measurement with oscilloscope
- Can show the various the converter response and behavior
- Applies to both linear and non-linear systems
- Need good knowledge to interpret the waveforms

Zero-Delay PWM (ZDP™)



1. Sudden load current increase causes VOUT to drop

2. VOUT dropping directly and immediately causes duty cycle to increase

3. COMP adjusts as needed to maintain DC regulation

Legend

Fast Change:

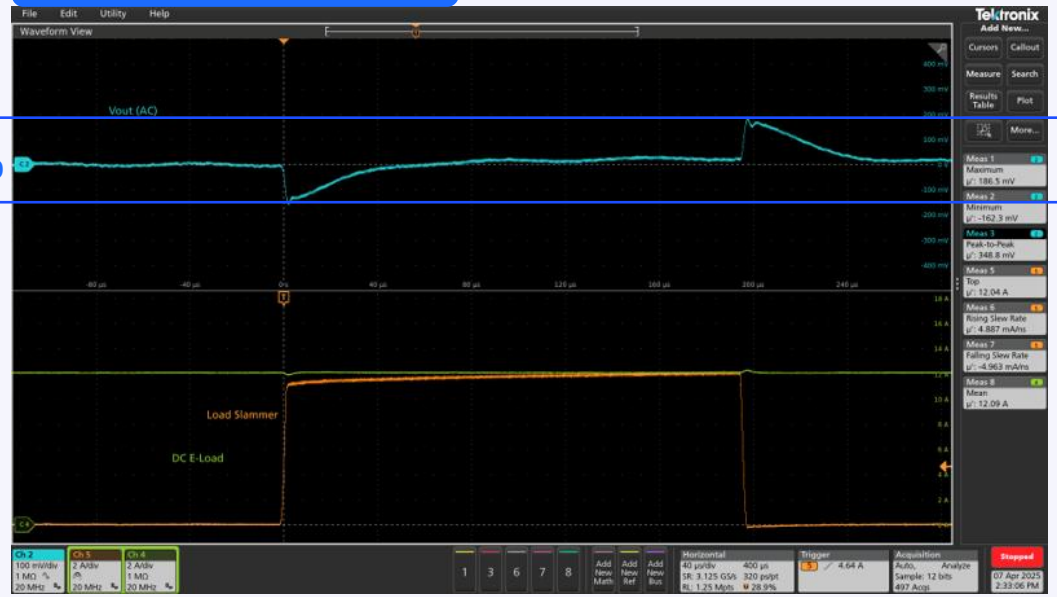
Slow change:

Zero Delay PWM(ZDP™) - Link to Web ZDP™ App Note

- Fixed-frequency power supply control method
- Improves transient response compared to a common fixed-frequency control method (e.g. voltage mode control or peak current mode control)

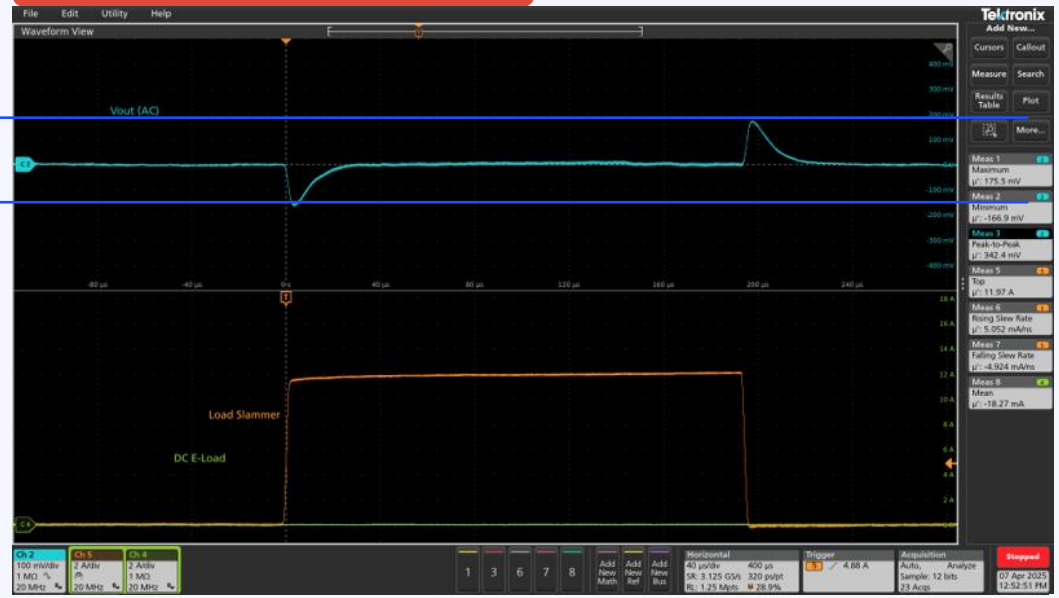
ZDP™ | Reducing Output Capacitance

MPQ4385 (ZDP™)

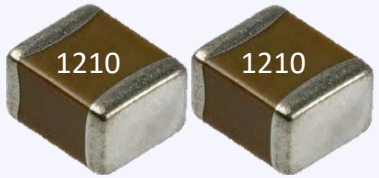


±3%

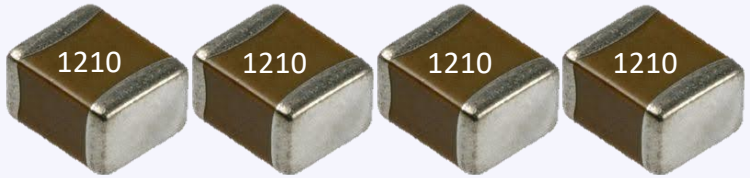
COMPETETION (PCMC)



2x 47uF (1210)



4x 47uF (1210)

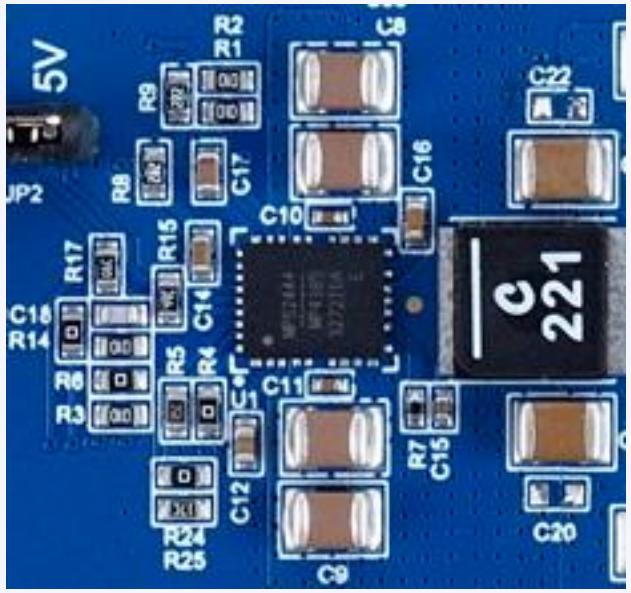


16mm² footprint saving

MPQ4385 Evaluation Board

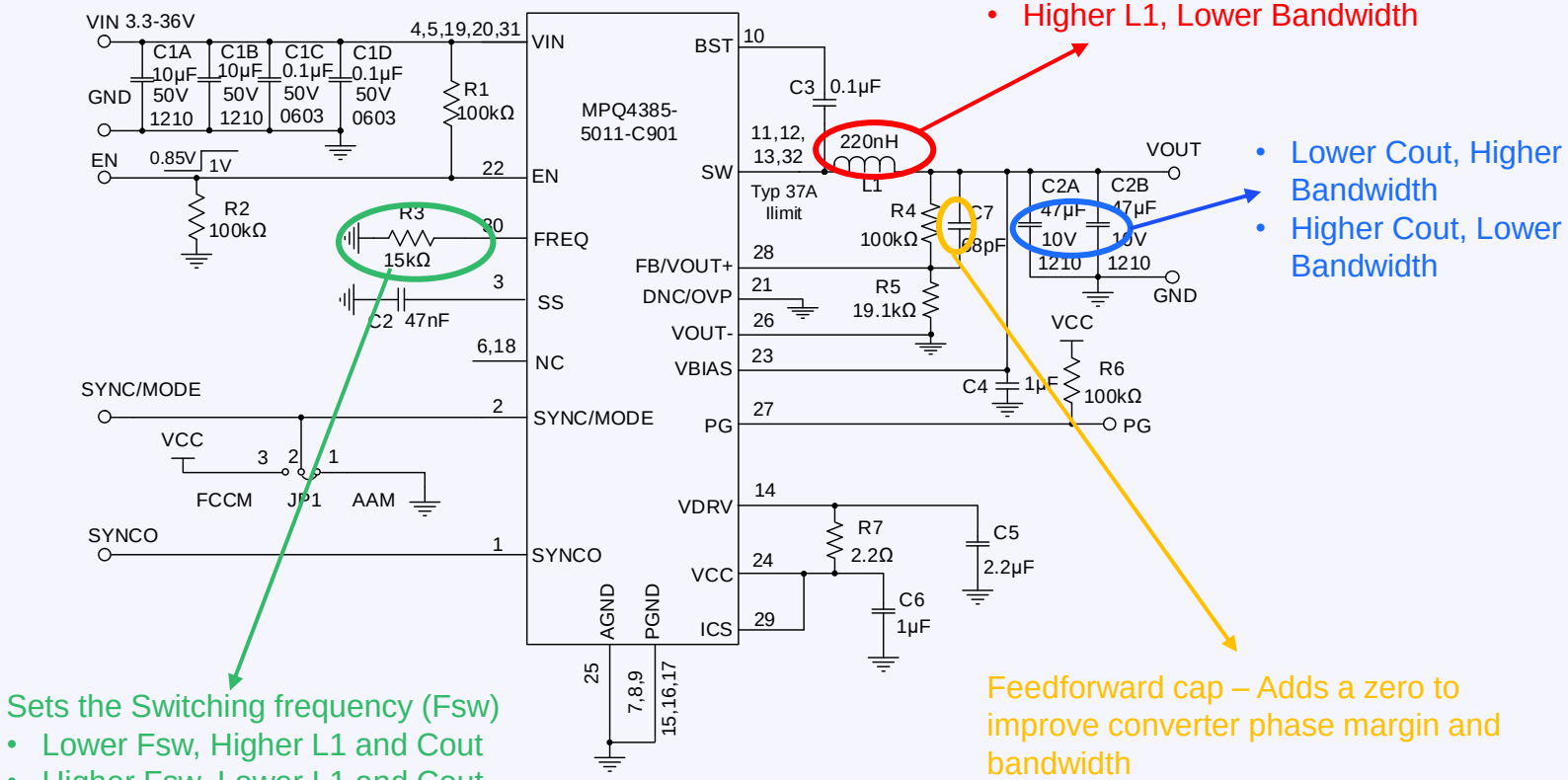
MPQ4385

40V 25A Buck w/ ZDP™



BOM ~ 300mm²

Components that influence the MPQ4385 control loop stability

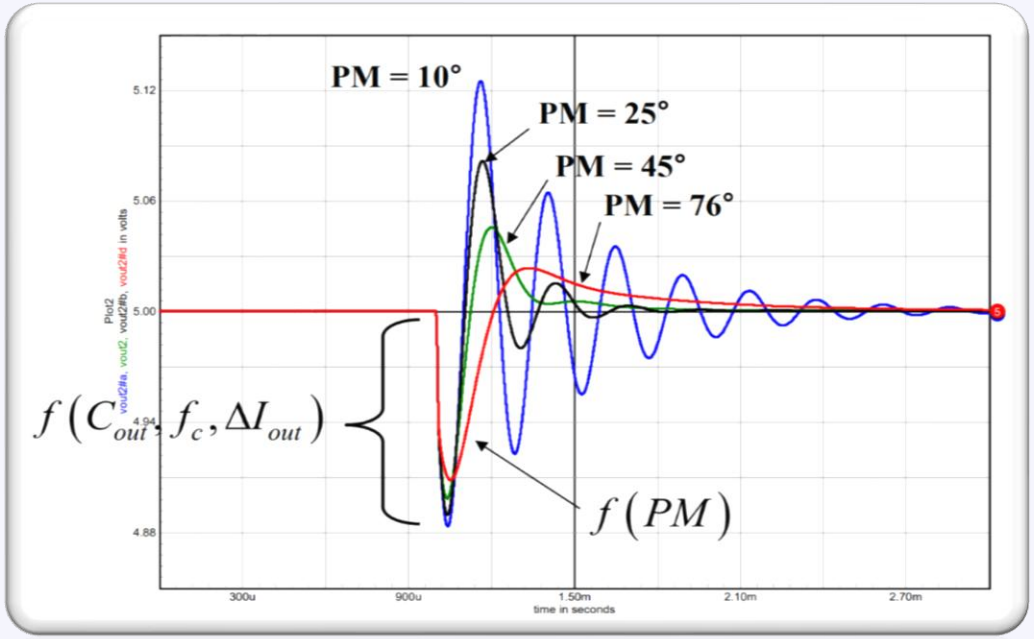


Phase Margin Analysis in Time Domain

What is Ringing and How does it relate to Phase Margin Analysis?

- ❑ Ringing is observed on the Vout due to a load transient.
- ❑ In time domain, the load step response of the system indicates how fast the system responds.
- ❑ As shown in the figure:
  - ✓ Lower Phase Margin > More Ringing > Longer Settling Time > Unstable System
  - ✓ Higher Phase Margin > Less/No Ringing > Smaller Settling Time > Stable System

Relationship between Ringing and Phase Margin (1)



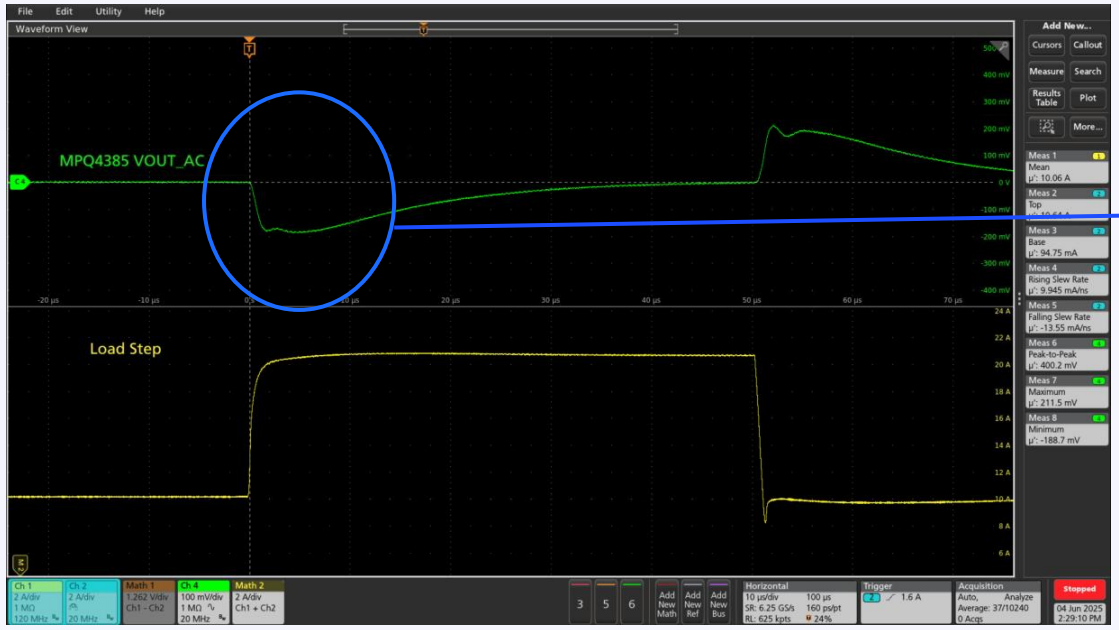
Phase Margin and Number of Output Rings after Load Step

Phase Margin	10°	25°	45°	>60°
No of Rings	7	3	1	0

(1) Tutorial on “DC-DC Converters Feedback and Control”, On Semiconductor, 2008

Practical Example - Phase Margin Analysis in Time Domain

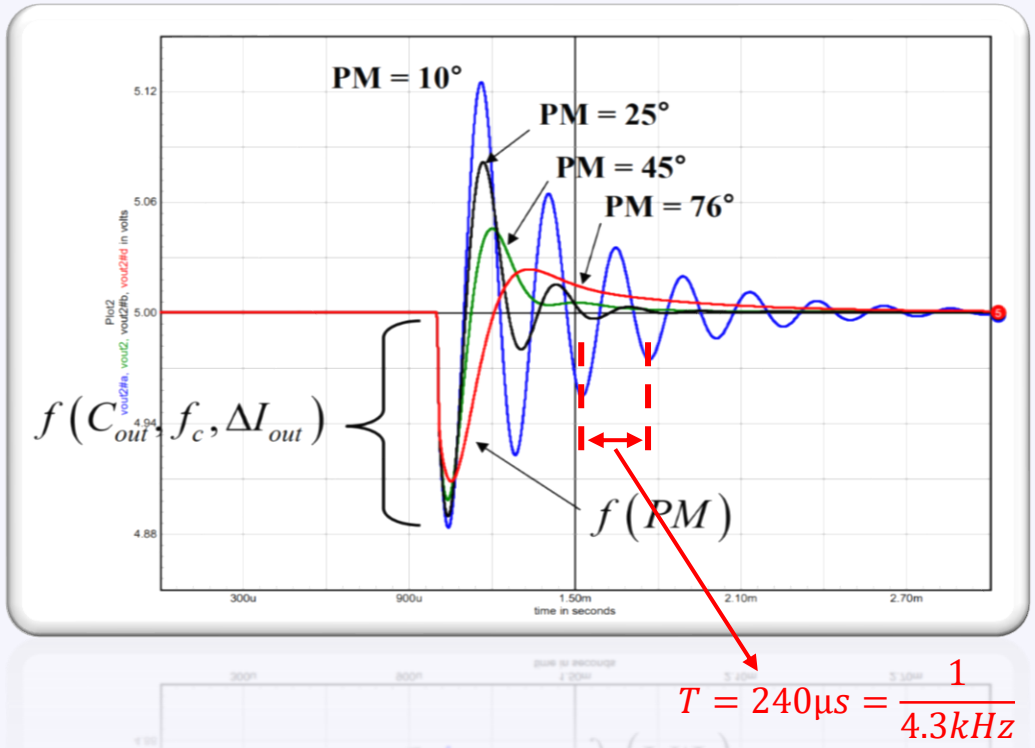
Vin = 12.5V, Vout = 5V, Fsw = 2.2MHz, L = 220nH, Cout = 2x22uF (1206,10V), Load Step = 10A <-> 20A @ 10A/us



- One ring Observed
- Corresponds to 45° Phase Margin (Acceptable Stability)
- Critically Damped Response

What Else You Can Decipher In Time Domain?

- The bandwidth of the DC-DC converter can also be estimated from the load transient waveform.
- The converter bandwidth is closely related to how fast it responds to changes in time domain.
- Quick way to estimate is from the ringing frequency.
  - ✓ Not very useful for critically damped or high phase margin systems.



How to measure the Bandwidth that is applicable for all PM cases?

One can easily estimate the converter bandwidth by the following:

- Response time method
- Undershoot based energy method

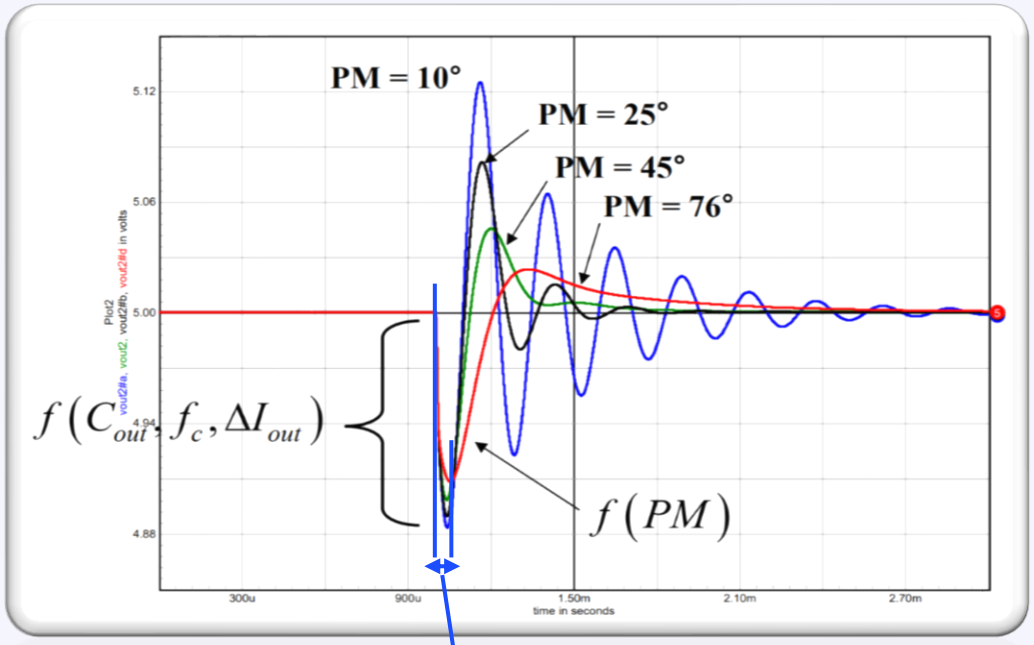
Bandwidth Analysis in Time Domain

Response Time Method

- Estimating DC-DC converter bandwidth from response time is a practical method in time domain analysis.
- Response time T_r is approximate indication of control bandwidth. Defined as the time it takes to go from 10% to 90% of the final output value.
- For well-compensated power converter, the bandwidth can be estimated by the following:

$$Bandwidth(BW) = \sim \frac{0.35}{T_r}$$

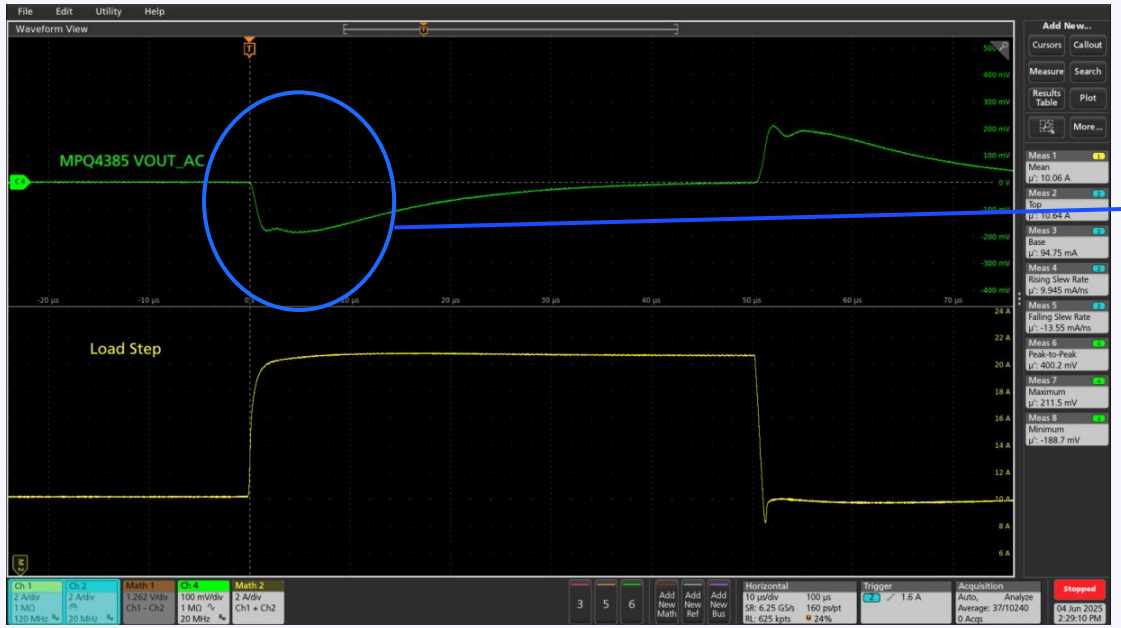
The above equation comes from the relationship between the rise time and bandwidth in a first order or single-pole low-pass system, which is a common model for well compensated DC-DC converter.

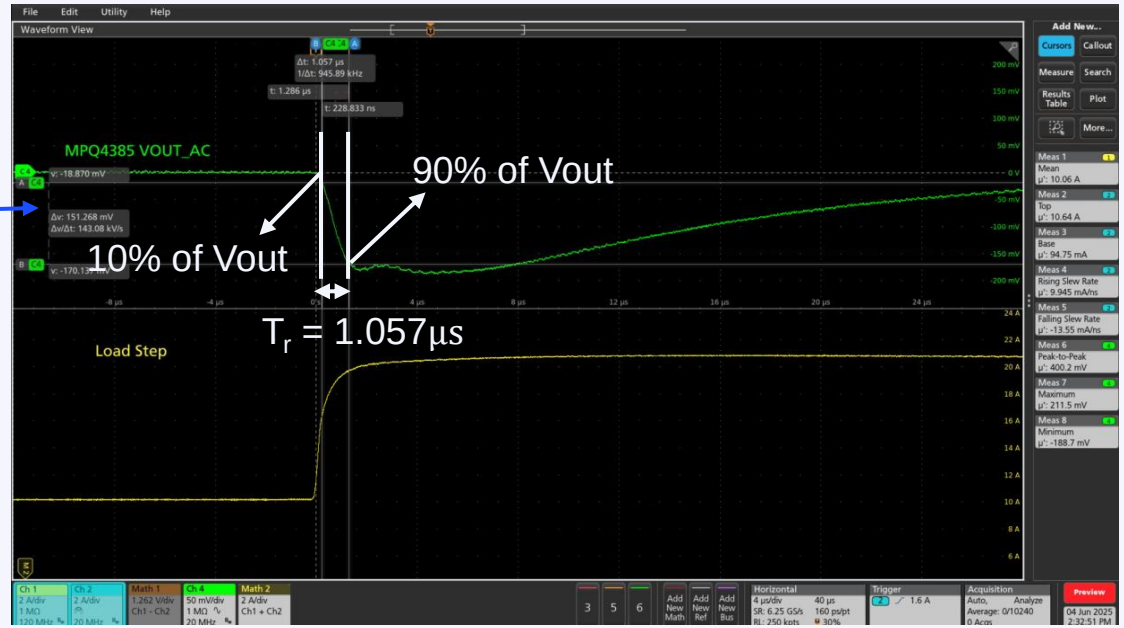


Practical Example - Bandwidth Analysis in Time Domain

Response Time Method

Vin = 12.5V, Vout = 5V, Fsw = 2.2MHz, L = 220nH, Cout = 2x22uF (1206,10V), Load Step = 10A <-> 20A @ 10A/us





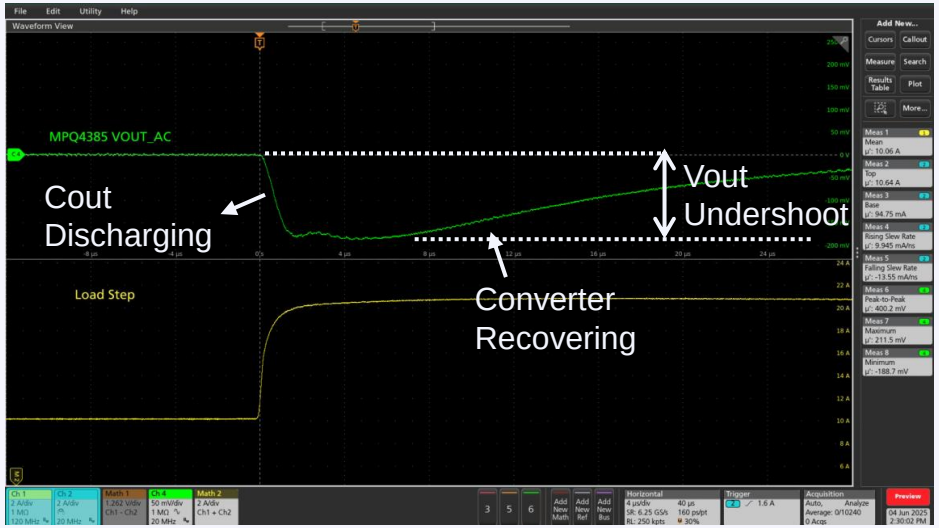
In this example:

- T_r = 1.057µs
- BW = 0.35/ 1.057µs = ~331kHz

Bandwidth Analysis in Time Domain

Undershoot Based Energy Method

- Undershoot refers to temporary dip in the output voltage when a sudden increase in load current.
- Undershoot is caused by a deficit of charge in the output capacitor.
- The bandwidth of the converter can be estimate from the following equation:



$$\Delta Vout = \frac{\Delta Iout}{2*\pi*f_0*Cout}$$

Where ΔV_{OUT} is the output undershoot, ΔI_{OUT} is the load step current, f_0 is the loop bandwidth, and C_{OUT} is the output capacitance.

This equation comes from the capacitor current equation:

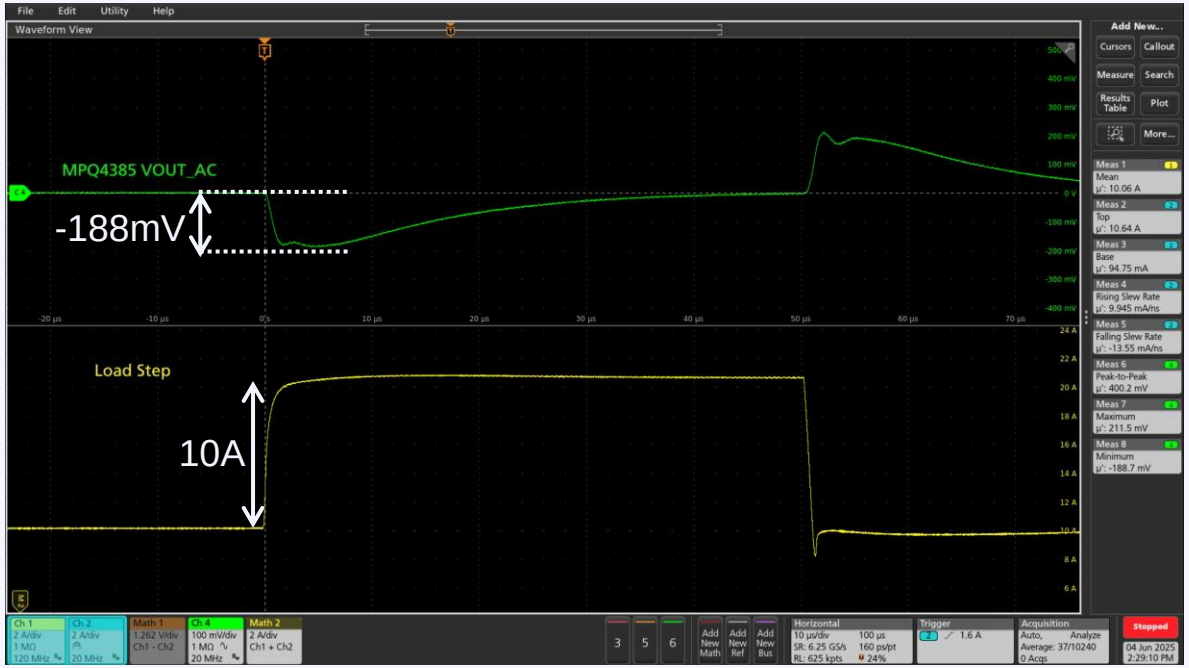
$$I = C\frac{dV}{dT}$$

Where $dT \approx \frac{1}{2\pi f_0}$,

Practical Example - Bandwidth Analysis in Time Domain

Undershoot Based Energy Method

Vin = 12.5V, Vout = 5V, Fsw = 2.2MHz, L = 220nH, Cout = 2x22uF (1206,10V), Load Step = 10A <-> 20A @ 10A/us



$$f_0 = \frac{\Delta Iout}{2*\pi*\Delta Vout*Cout}$$

In this example:

- ΔIout = 10A
- ΔVout = -188mV
- Cout = 2x22μF
- $F_0 \approx 192kHz$

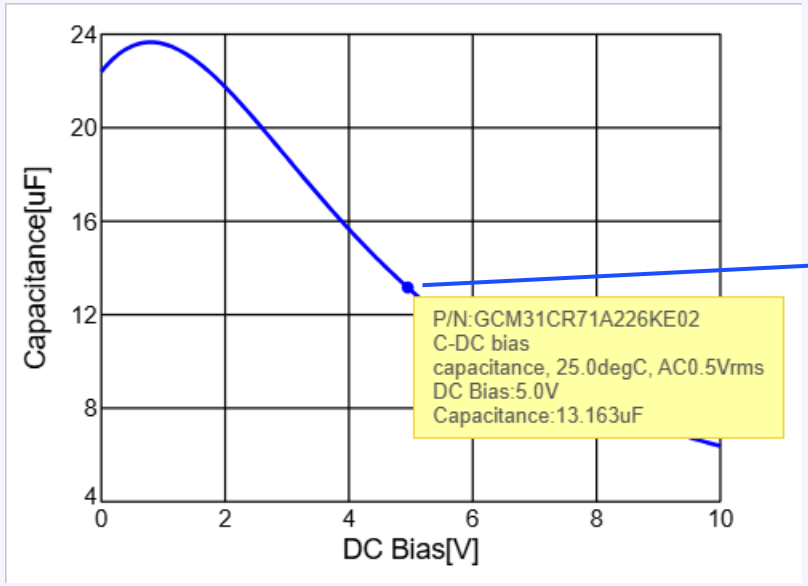
The bandwidth estimated doesn't match with estimated bandwidth from the response time method ☹ ☹

Practical Example - Bandwidth Analysis in Time Domain(Cont'd)

Undershoot Based Energy Method – Output Capacitor Influence

❑ Actual example application we used two **22μF / 10V 1206 Murata GCM31CR71A226KE02** in parallel.

Be aware of MLCC capacitor DC bias characteristics!!!



Source:
https://ds.murata.co.jp/simsurfing/mlcc.html

Only 13.16μF at 5V DC

Actual capacitance = 2*13.16μF ≈ 26.4μF

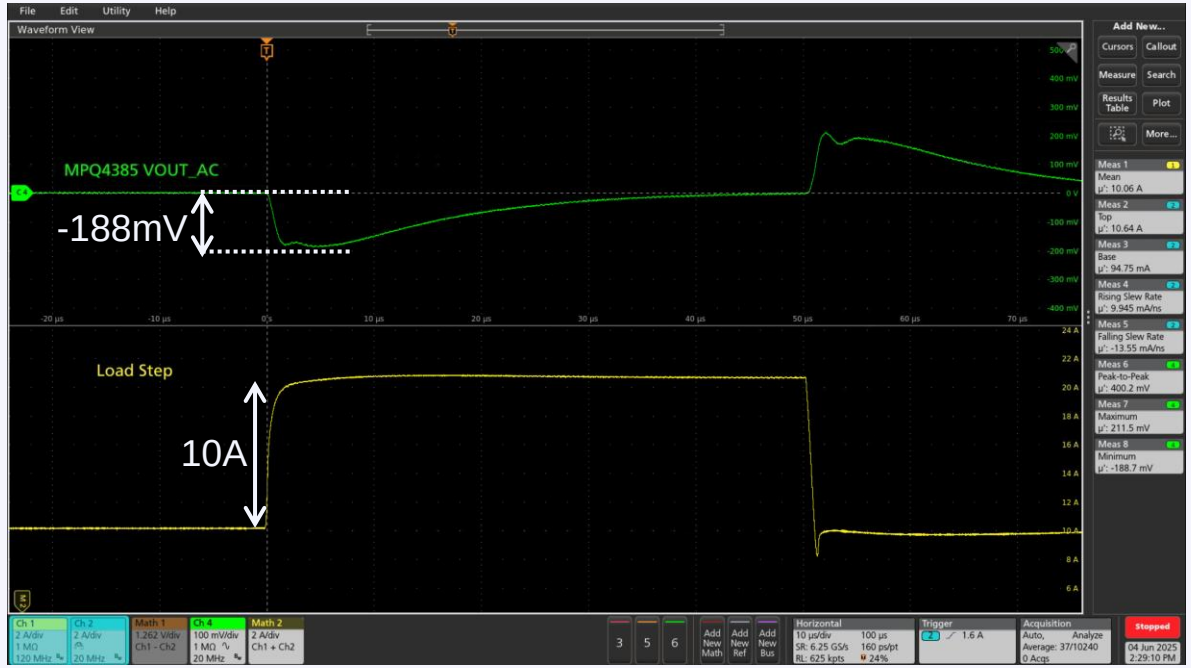
(if DC bias effect is not specified for the specific capacitor type, ask for it)

✓ Always use the actual effective capacitance when design the control loop or performing loop related calculations

Practical Example - Bandwidth Analysis in Time Domain(Cont'd)

Undershoot Based Energy Method - Output Capacitor Influence

Vin = 12.5V, Vout = 5V, Fsw = 2.2MHz, L = 220nH, Cout = 2x22uF (1206,10V), Load Step = 10A <-> 20A @ 10A/us



Effective capacitance = 2*13.16μF ≈ 26.4μF

$$f_0 = \frac{\Delta Iout}{2*\pi*\Delta Vout*Cout}$$

In this example:

- ΔIout = 10A
- ΔVout = -188mV
- Cout_effective =26.4μF (assuming DC-Bias derating)
- $F_0 \approx 326kHz$

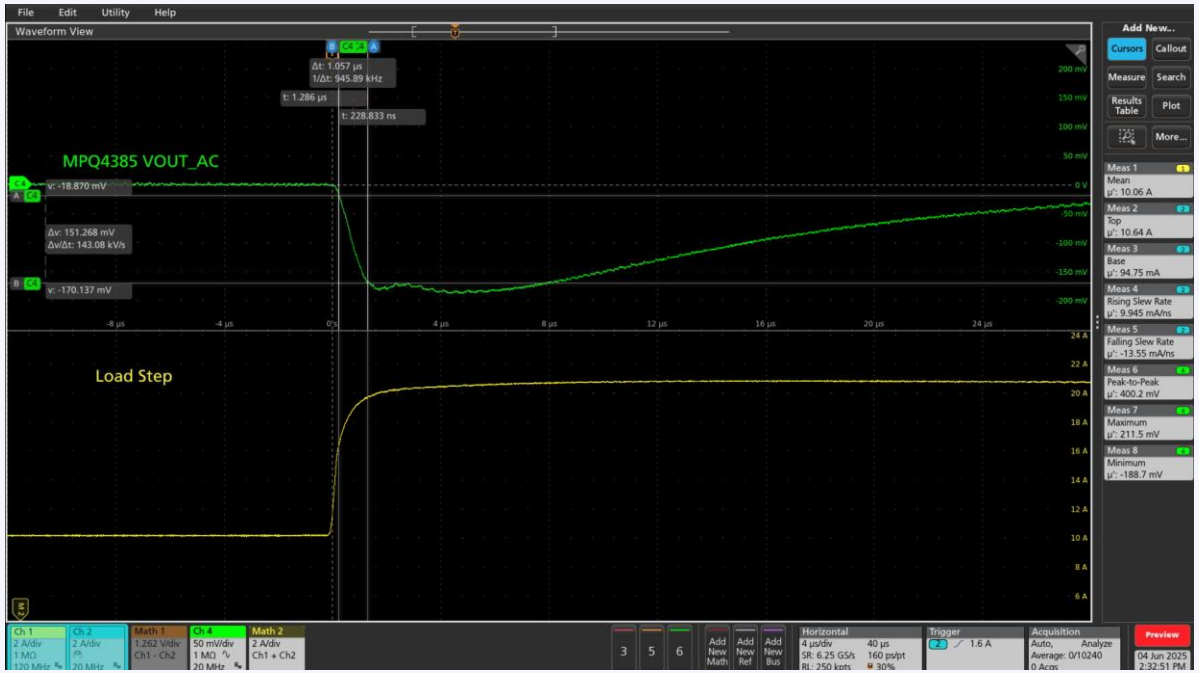
Always use the actual effective capacitance when design the control loop or performing loop related calculations ☺☺

Summary – Bandwidth Analysis in Time Domain

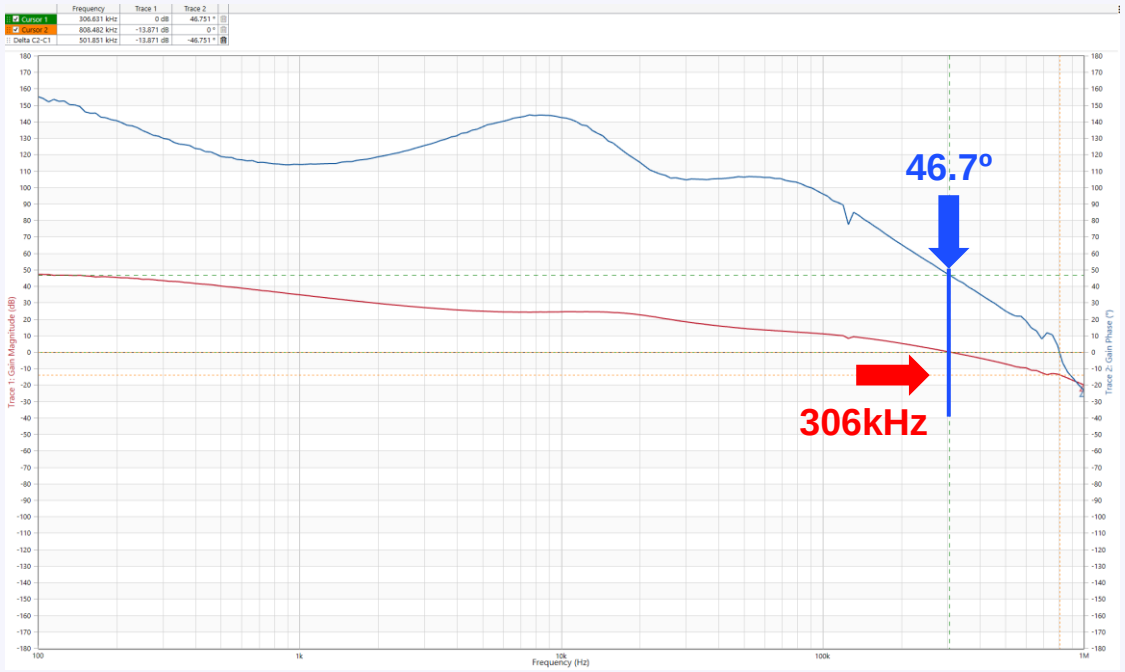
- There are several ways to estimate the converter bandwidth.
  - **Estimation from Ringing Frequency**
    - ✓ Quick visual feedback from oscilloscope
    - ✓ Not very useful for critically damped or high phase margin systems
  - **Estimation from response time**
    - ✓ Quick visual feedback and real time monitoring
    - ✓ Requires clean measurements
  - **Undershoot-based energy method**
    - ✓ Intuitive - shows direct relationship between output capacitor and response time
    - ✓ Need to have proper information about output capacitor characteristics

Practical Example Comparison - Frequency Domain vs Time Domain

Time Domain

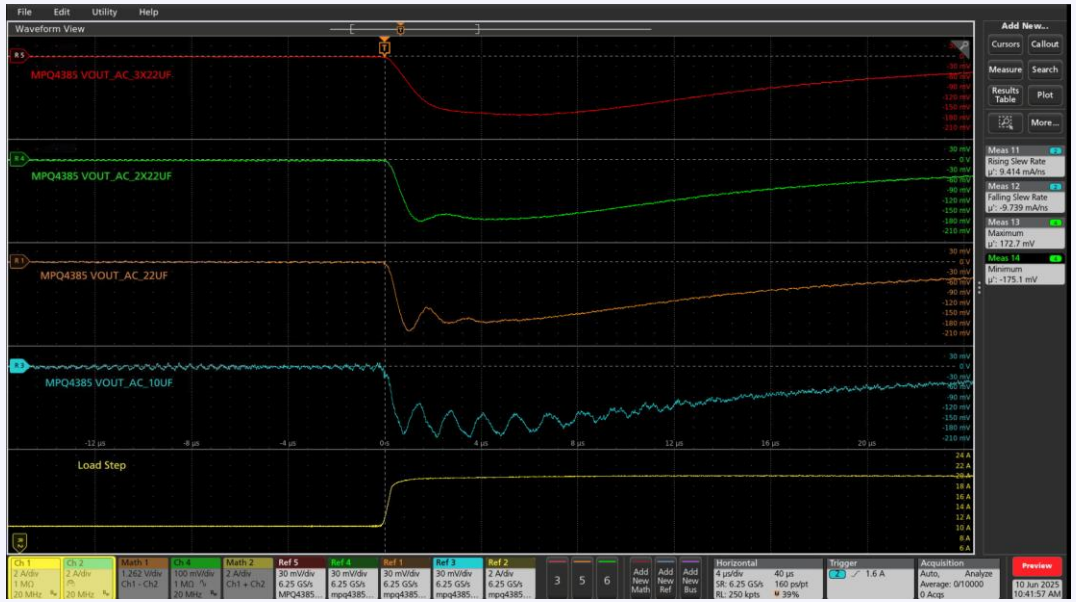


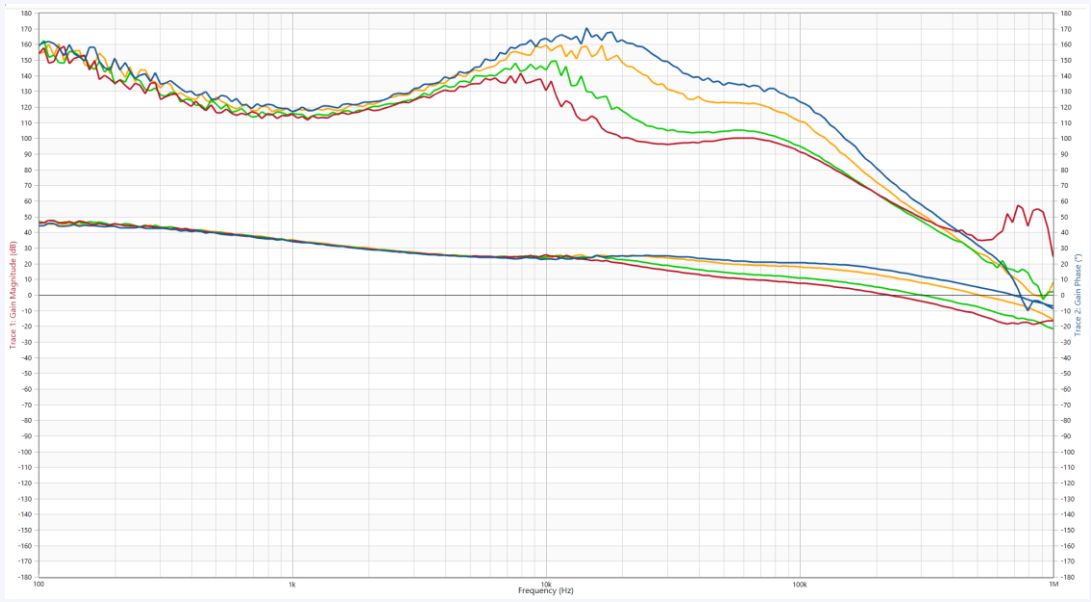
Frequency Domain



Case	Frequency Domain		Time Domain		
	Phase Margin	Bandwidth	Phase Margin	Bandwidth (Response Time)	Bandwidth (Undershoot based energy method)
Cout = 2x22µF	**46.7º**	**306kHz**	**~45º**	**~331kHz**	**~320kHz**

Comparison - Frequency Domain vs Time Domain

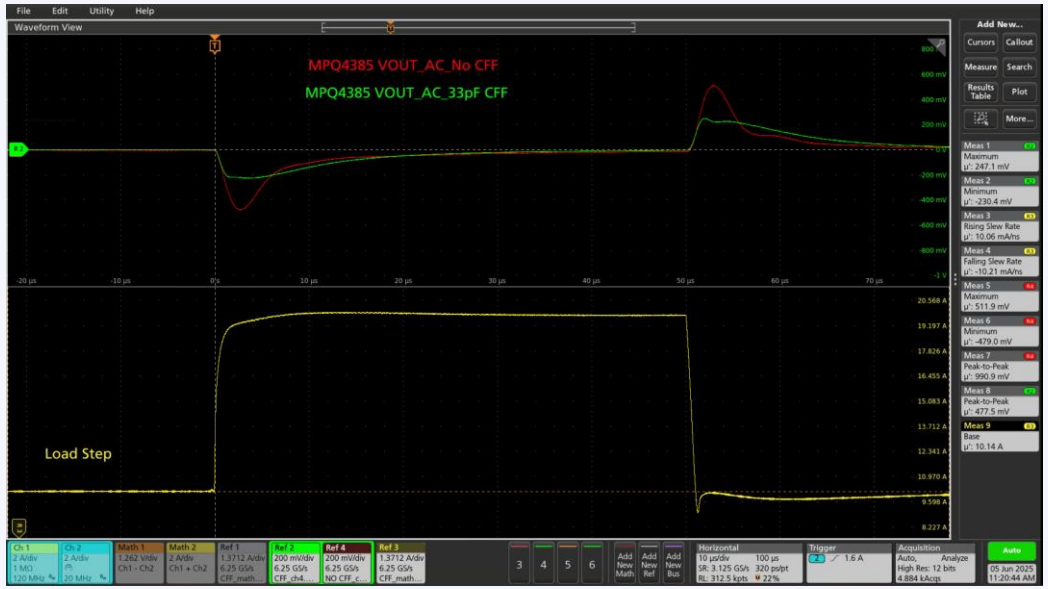




Case	Frequency Domain		Time Domain		
	Phase Margin	Bandwidth	Phase Margin	Bandwidth (Response Time)	Bandwidth (Undershoot based energy method)
Cout = 3x22µF	60.3º	224kHz	≥60º	~215kHz	~216kHz
Cout = 2x22µF	46.7º	306kHz	~45º	~331kHz	~320kHz
Cout = 22µF	28º	515kHz	~25º	~550kHz	~564kHz
Cout = 10µF	9.7º	695kHz	~10º	~730kHz	

Transient Response optimization for DC-DC converters

- ❑ Internally compensated converters have limited transient response.

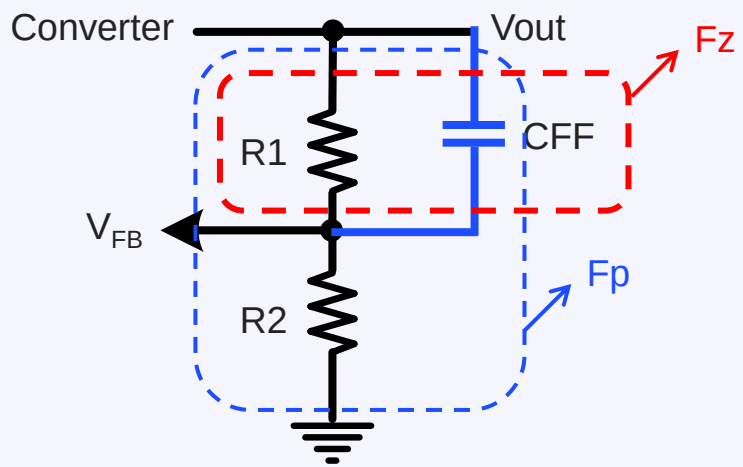


How to improve the transient response?

- ✓ Adding a feed-forward capacitor (CFF) in the feedback networks boosts converter bandwidth with acceptable phase margin.

- ✓ CFF introduces a zero in the feedback loop and provides a phase boost which is maximum between the pole and zero frequencies.

$$Fz = \frac{1}{2\pi * R1 * CFF} \quad (1) \qquad Fp = \frac{1}{2\pi * CFF}\left(\frac{1}{R1} + \frac{1}{R2}\right) \quad (2)$$



- ✓ A too large CFF causes bandwidth too high resulting in lower phase margin or instability.

Transient Response optimization for DC-DC converters

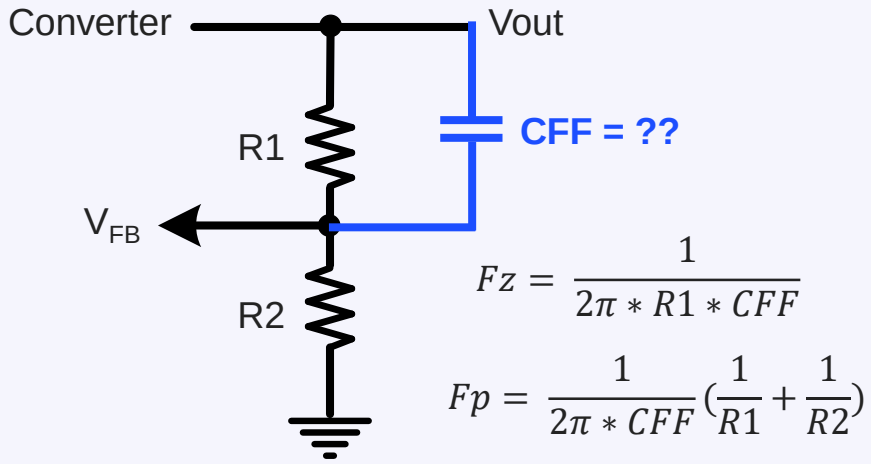
Practical Example - Design Procedure for CFF

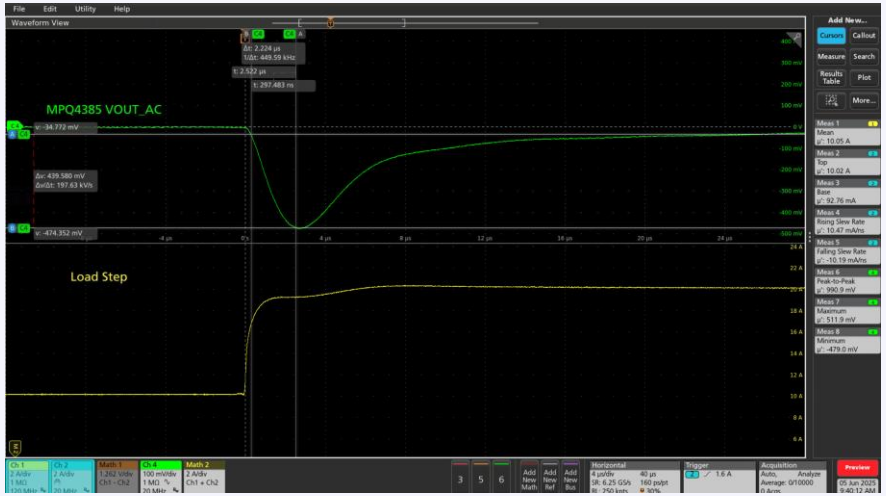
- Identify feedback resistor values to set the desired output.
  - **Referring to MPQ4385 schematic, R1 = 100kΩ and R2 = 19.1kΩ.**
- Determine the converter bandwidth without the CFF.
  - **In this example, the bandwidth is measured to be ~139kHz.**
- The geometric mean of the feedback networks's zero and pole frequency is used to determine the frequency where phase boost is required.
  - **The geometric mean frequency equal to the converter crossover frequency with no CFF.**

$$F_{BW\_NOCFF} = \sqrt{(Fz * Fp)}$$

Plugging Fz and Fp and solving for CFF, CFF = 28.6pF

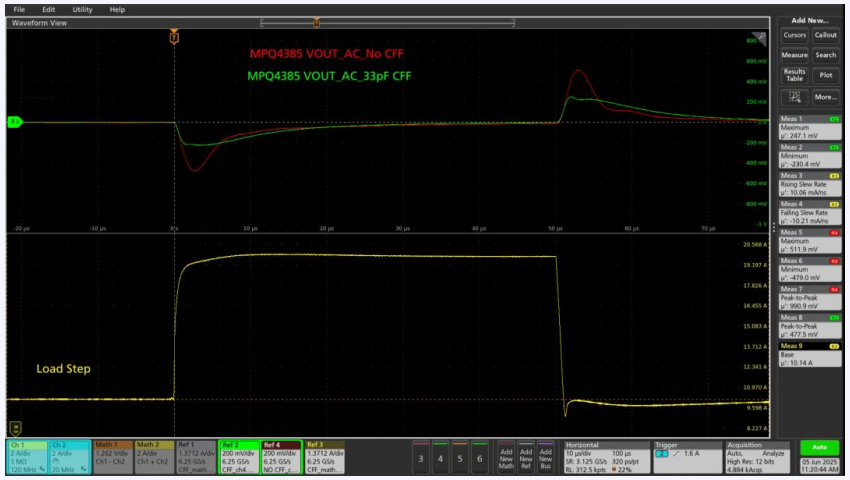
Rounding the CFF value to the nearest standard capacitor value, CFF = 33pF

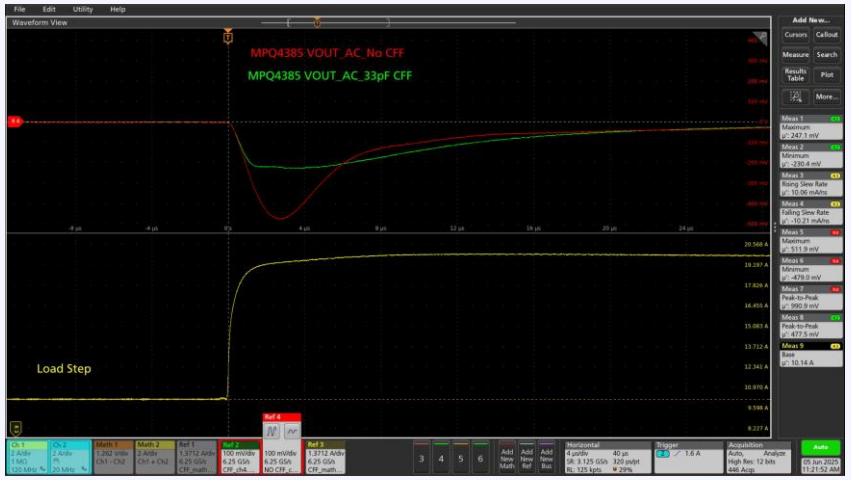


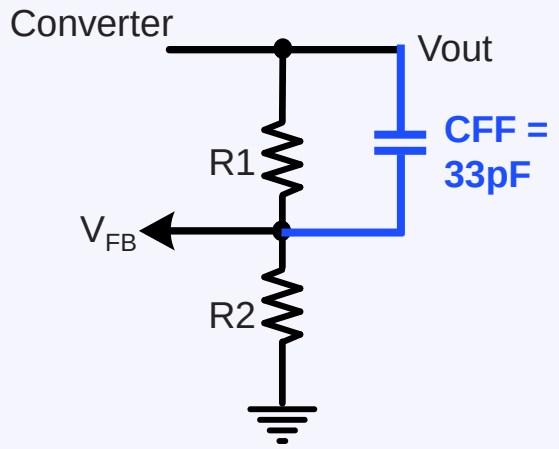


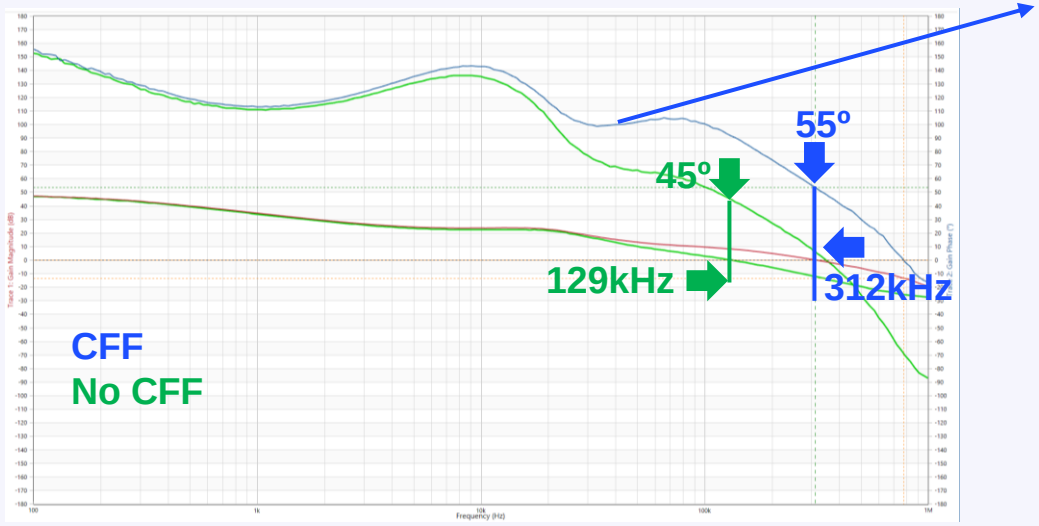
Transient Response optimization for DC-DC converters

Practical Example with calculated CFF









- Zero added between ~40kHz and 50kHz range
- Provides phase boost
- Bandwidth rolls off at higher frequency with acceptable phase margin
- 2x faster transient response

For most applications, this is an optimal placement of CFF.
Increasing CFF, increases the bandwidth results in lower overall phase margin.
Decreasing the CFF has the opposite effect.

Too small CFF, injects zero and pole frequencies too high resulting in no performance improvements!!!!

By adding an external feedforward capacitor, designers can fine-tune the control loop and optimize performance.

Summary

Comparison of Time Domain vs Frequency Domain

Frequency Domain	Loop Bandwidth (kHz)	Phase Margin (Degrees)	Gain Margin (dB)
Time Domain	Magnitude of output voltage undershoot (mV)	Output voltage behavior after load step (whether it has damped or oscillatory response)	Does not show up in the load transient response

- Quick way to estimate the loop response is to measure load transient response.
- Phase Margin in time domain is estimated whether the response has damped or oscillatory response.
- Control loop bandwidth can be measured in several ways. The response time method and undershoot based energy method-based estimations co-relates closely with Bode measurements.
- Too slow load steps cannot excite the converter loop over a sufficiently wide frequency range and will not always highlight stability problems. A fast load step with rise time << 1/fbw should be used for detecting stability problems in DC/DC converters.
- Effective output capacitance plays a critical role in the control loop.
- By adding an external feedforward capacitor, designers can fine-tune the control loop and optimize performance for internally compensated DC-DC converters.

Thank You

Questions???