Solutions for Powering Intel and AMD SoCs

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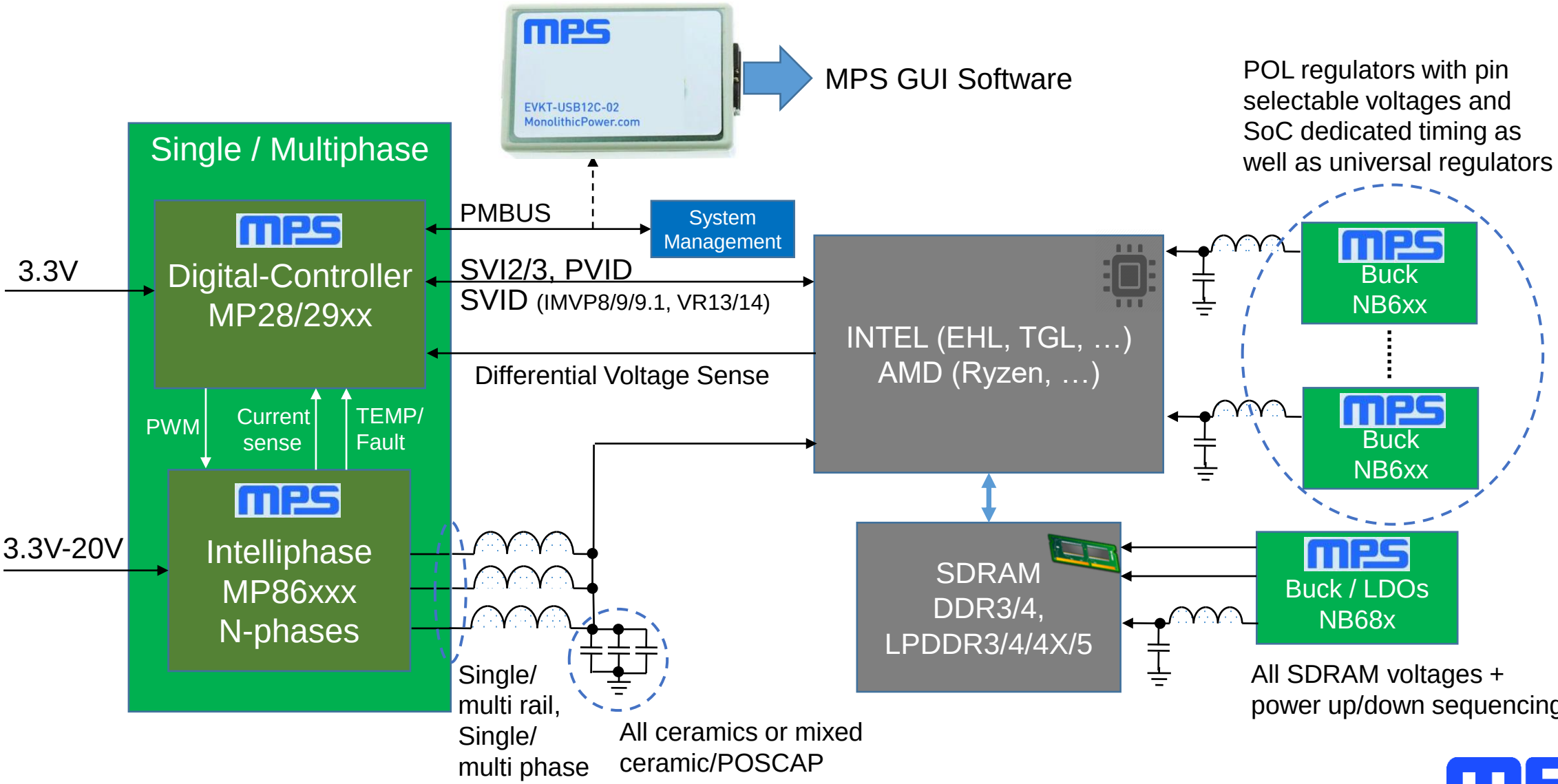
Agenda

Solutions for Powering Intel and AMD SoCs

- Solution Overview
- Digital Multi-Phase Controller
- Powerstage / DrMOS / IntelliPhase
- Design Tools
- TGL-UP3 Example
- Summary
- Q&A

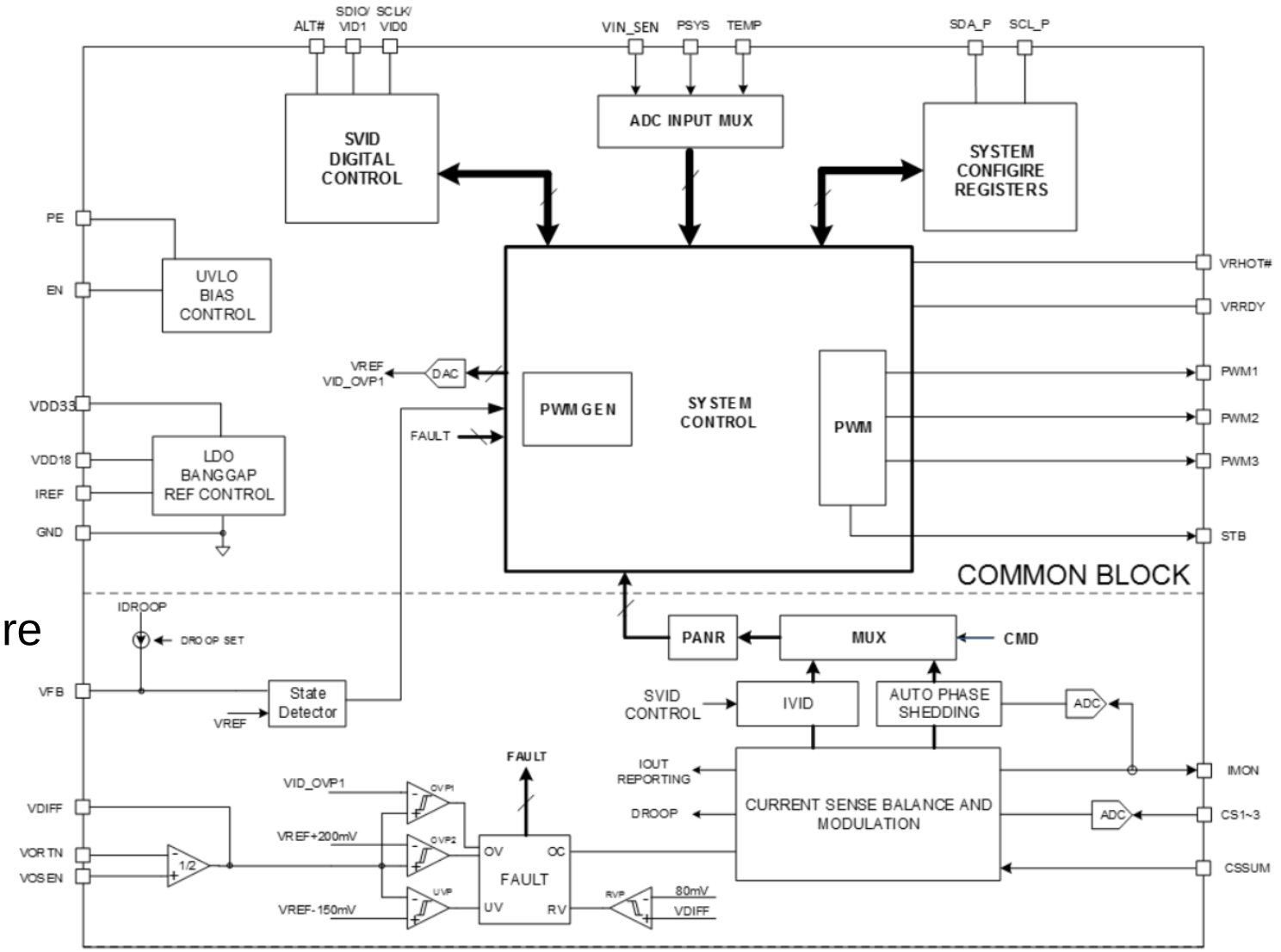
MPS Solution Overview



Digital Multi-Phase Controller

FEATURES

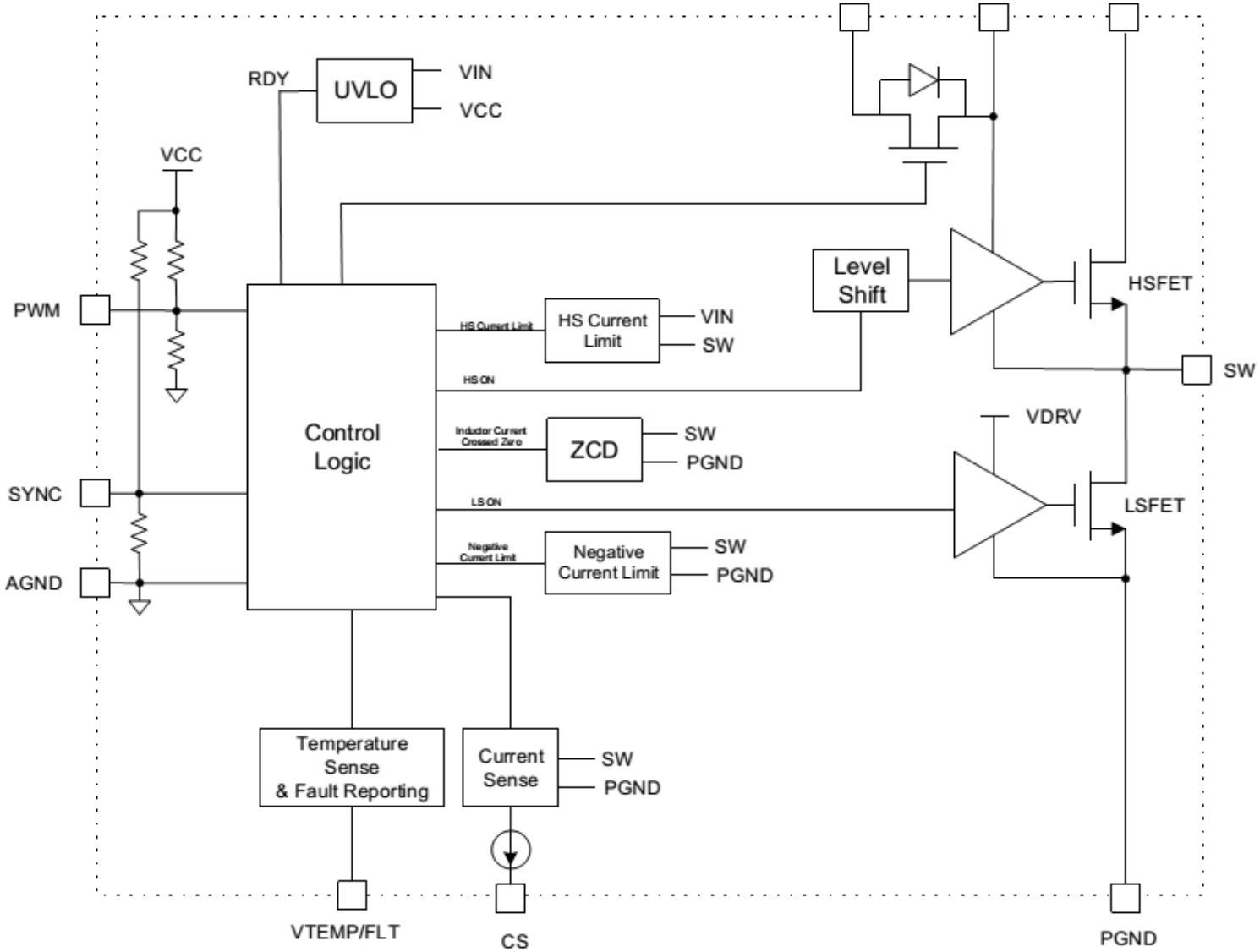
- **Single/Multiple Loop (Flexible Phase Assignment)**
- **Patented Constant on-time Control: Best Transient in the Market**
- **All Digital Control via PMBUS**
- **Minimal External Components**
- **Telemetry**
  - Vin, Vo, Iin, Iout, Pin, Pout, Temperature
  - Peak Current Detection
- **Advanced Fault Handling**
  - OCP, OVP, UVP, OTP
  - Cycle-by-cycle OC/UC
  - Catastrophic Failure Protection



Powerstage / DrMOS / IntelliPhase

FEATURES

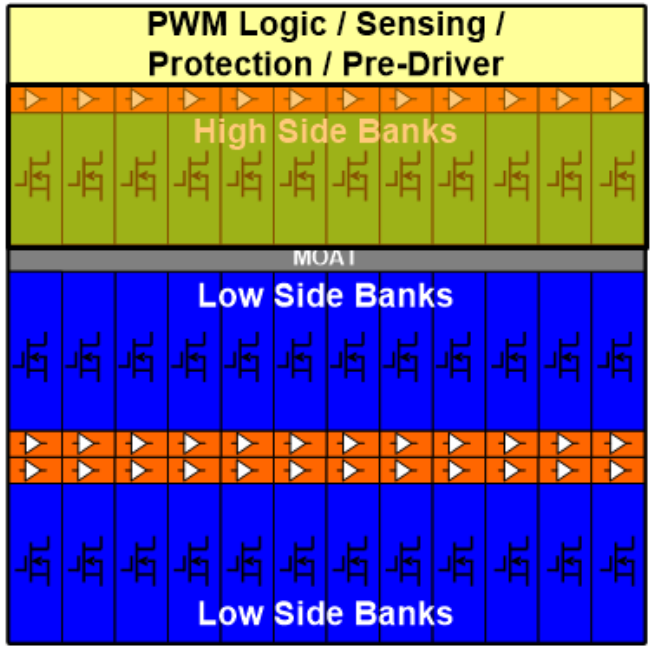
- Continuous Current up to 80A, Peak Current up to 125A (MP86998)
- Package Options:
  - Common Footprint (CFP)
  - MPS Proprietary Footprint
- Supports Wide Fsw Range
  - From 100kHz to 3MHz
  - Balanced Between Transient and Efficiency
- Built-In ZCD, OCP, NOCP, OTP, SCP
- Current Sense Tolerance ±3%
- Single-End Current Sensing Output
  - Minimal External Components
  - Immune to Noise



Powerstage / DrMOS / IntelliPhase

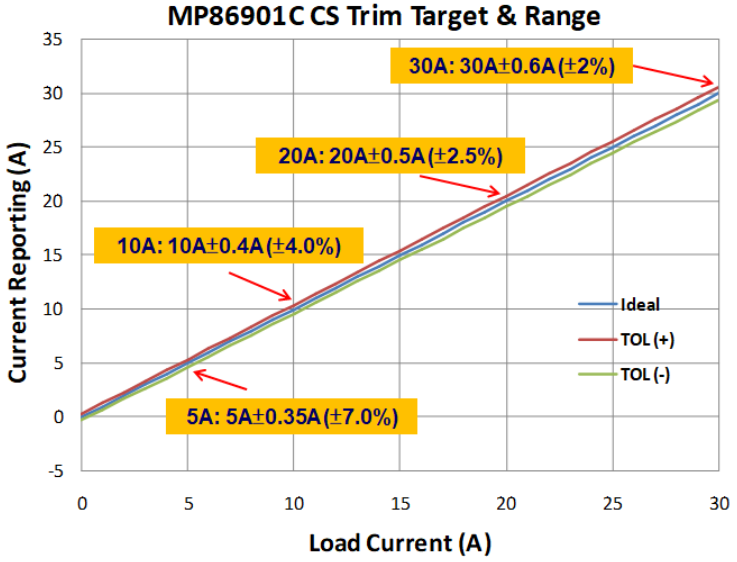
Monolithic Design

- Distributed Gate Driver (*DGD*) minimizes the Gate Delay, significantly reduces the dead time
- Minimized path from driver to FET cells, strong driving capability with fast turn-on/off speed



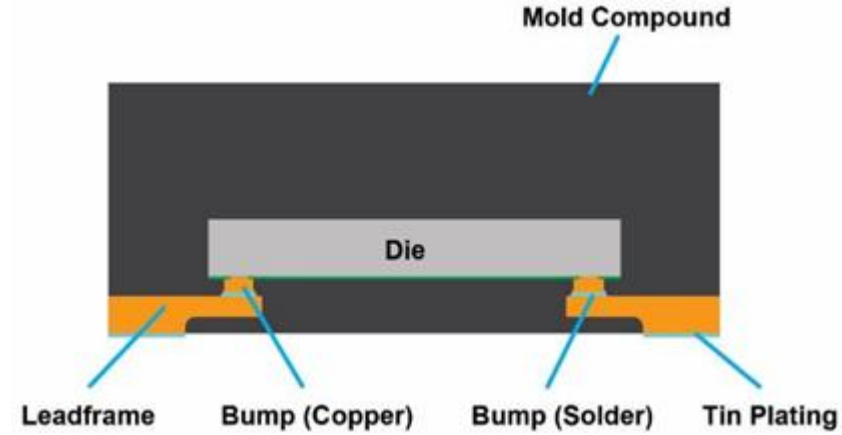
On-Die Current Sensing

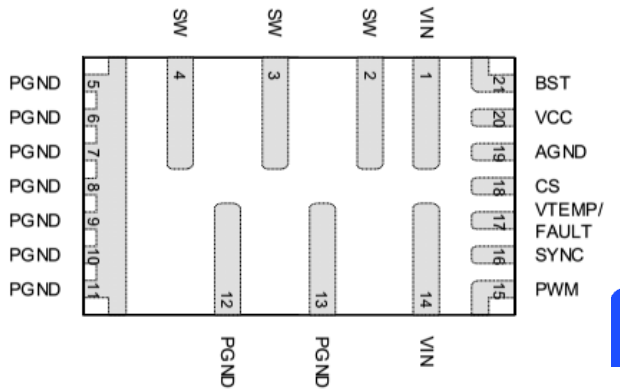
- CS pin is a current output of 10μA x Iout
- Tracks current cycle by cycle
- Independent of the Temperature, Rdson, and Inductor DC resistance variations (±3%)
- No thermal compensation needed



Flip-Chip Package

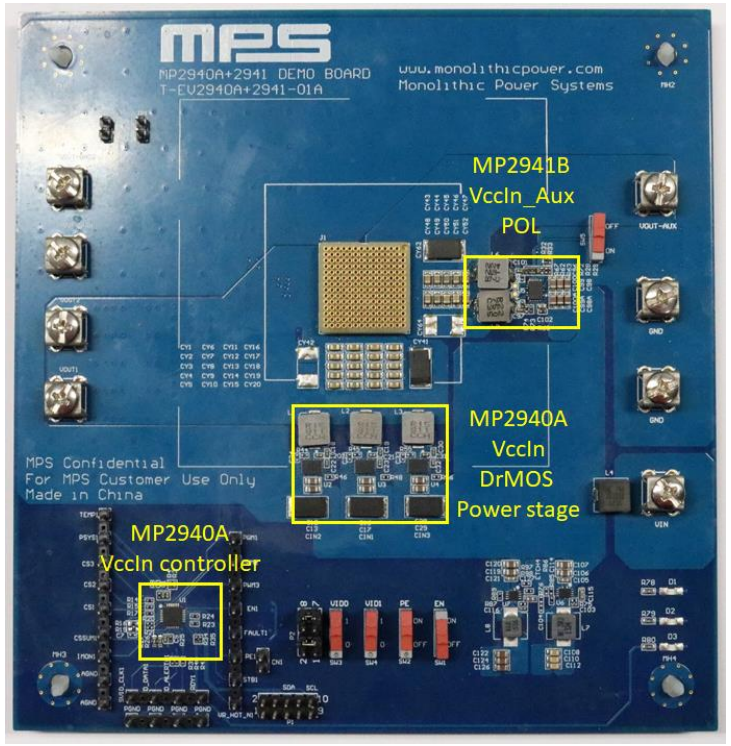
- High Reliability
- Small Form Factor
- Good Thermal Design
- Low Parasitic Inductance

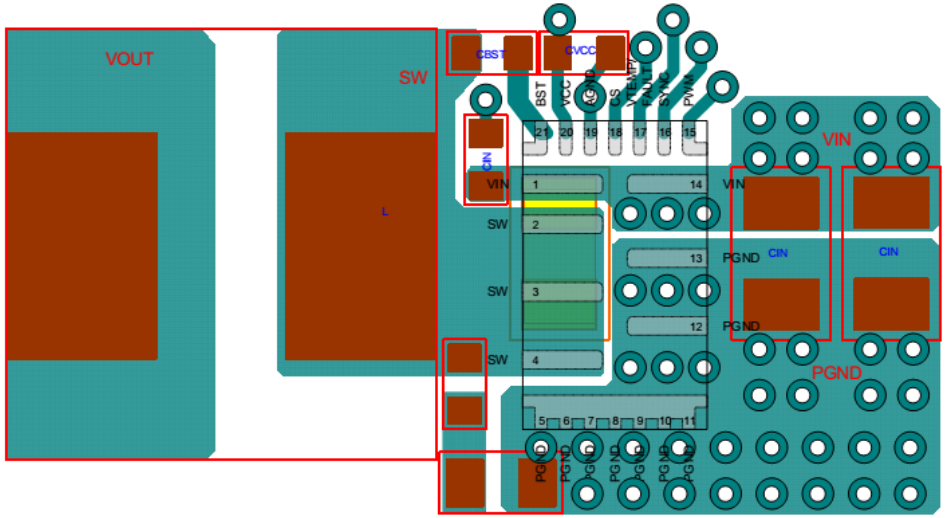


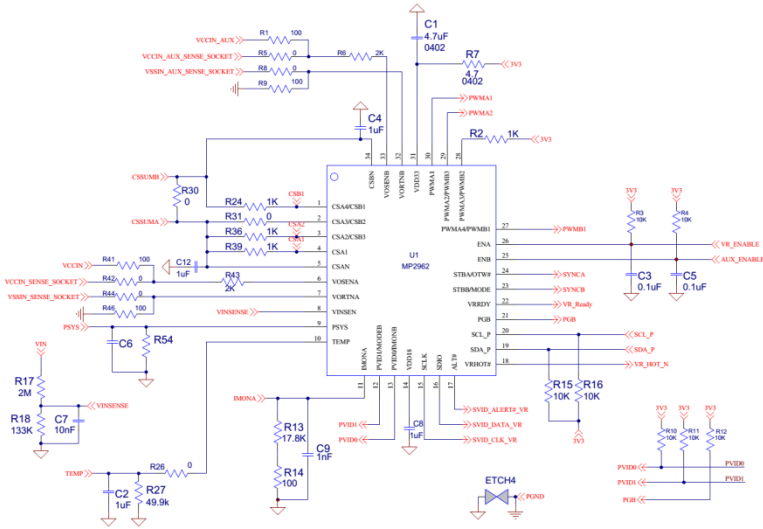


Design Tools : Reference Designs / Layout Guidelines and EVBs

- Reference schematic for most SoCs from Intel/AMD
  (either from MPS or SoC vendor)
- Proven and detailed layout guidelines in each DrMOS/POL regulator datasheet
- Evaluation Boards for many digital controller/DrMOS and POL regulator







Input Capacitor: 0805 package (top side & bottom side)
Inductor: 6.5 × 6.5 (mm)
VCC/BST capacitor: 0402 package
Via size: 20/10 mils

Design Tools : Digital Controller Configuration

- MPS provides design/SoC specific initial configuration for digital controller
  - Based on experience, validated with SoC vendor tools on MPS evaluation boards (e.g. Intel VRTT)
- Customer can further optimize the design with MPS Excel Design tool and GUI software

11	Controller	MP2940A	
12	4-digital code		HEX
13	Code Revision	01	HEX
14	PMBus Address	20	HEX
15	SVID Address	0	HEX
16	PMBus Address Control Mode	Register Set	
17	VIN_min	11.375	V
18	VIN_typ	12	V
19	VIN_max	12.625	V
20	*VIN UVLO & OVP*		
21	VIN Protection	Enable	
22	VIN OVP Mode	Latch OFF	
23	VIN UVP Mode	Latch OFF	
24	VIN UVLO Rising Threshold	8	V
25	VIN UVLO Falling Threshold	7	V
26	VIN OVP Threshold	15	V
27	VIN UV warning Threshold	9	V
28	*OTP*		
29	OTP Temperature Protection Mode	No Action	
30	Over Temperature Protection(OTP) Limit	130	°C
31	OTP Hysteresis	30	°C
32	*Configuration*		
33	Control Mode	SVID	
34	VID_SETP	10	mV/LSB
35	Vboot	1.8	V
36	VOUT_VID_Typ	1.8	V
37	VOUT_MAX	FF	V
38	VR Phase Number	1	phases
39	DrMOS or Driver	MP86901C	
40	CS Gain	10	uA/A
41	User Input CS Gain	10	uA/A

Design Target | Detailed Configuration | Tuning guide | Register_GUI_Output | Register_T

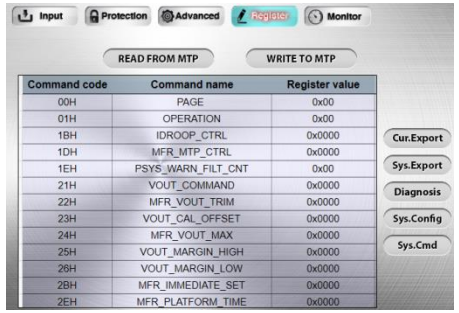
Configuration File

	Device Address	Command code	Command name	Byte	W/R	Value
2	0x20	0x00	PAGE	1	WR	0x00
3	0x20	0x01	OPERATION	1	WR	0x80
4	0x20	0x1B	IDROOP_CTRL	2	WR	0x0045
5	0x20	0x1D	MFR_MTP_CTRL	2	WR	0x0000
6	0x20	0x1E	PSYS_WARN_FILT_CNT	1	WR	0x02
7	0x20	0x21	VOUT_COMMAND	2	WR	0x1EA1
8	0x20	0x22	MFR_VOUT_TRIM	2	WR	0x0000
9	0x20	0x23	VOUT_CAL_OFFSET	2	WR	0x0000

Excel Design File

- Design Target Specification
- Detailed Configuration (Design Tuning)

GUI Software (Windows)

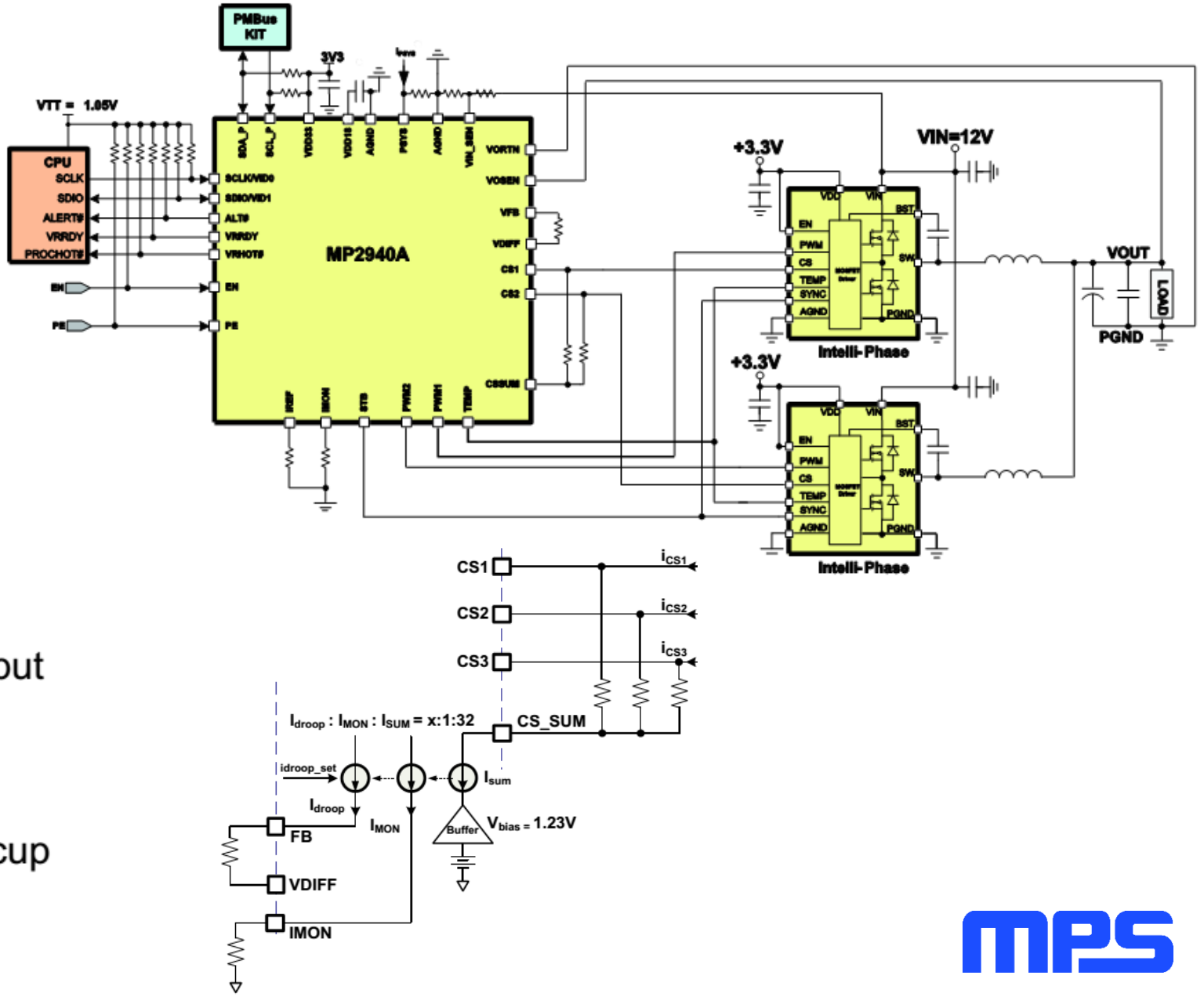


Programming Adapter

Digital Controller Example : MP2940A (INTEL IMVP8/9)

FEATURES

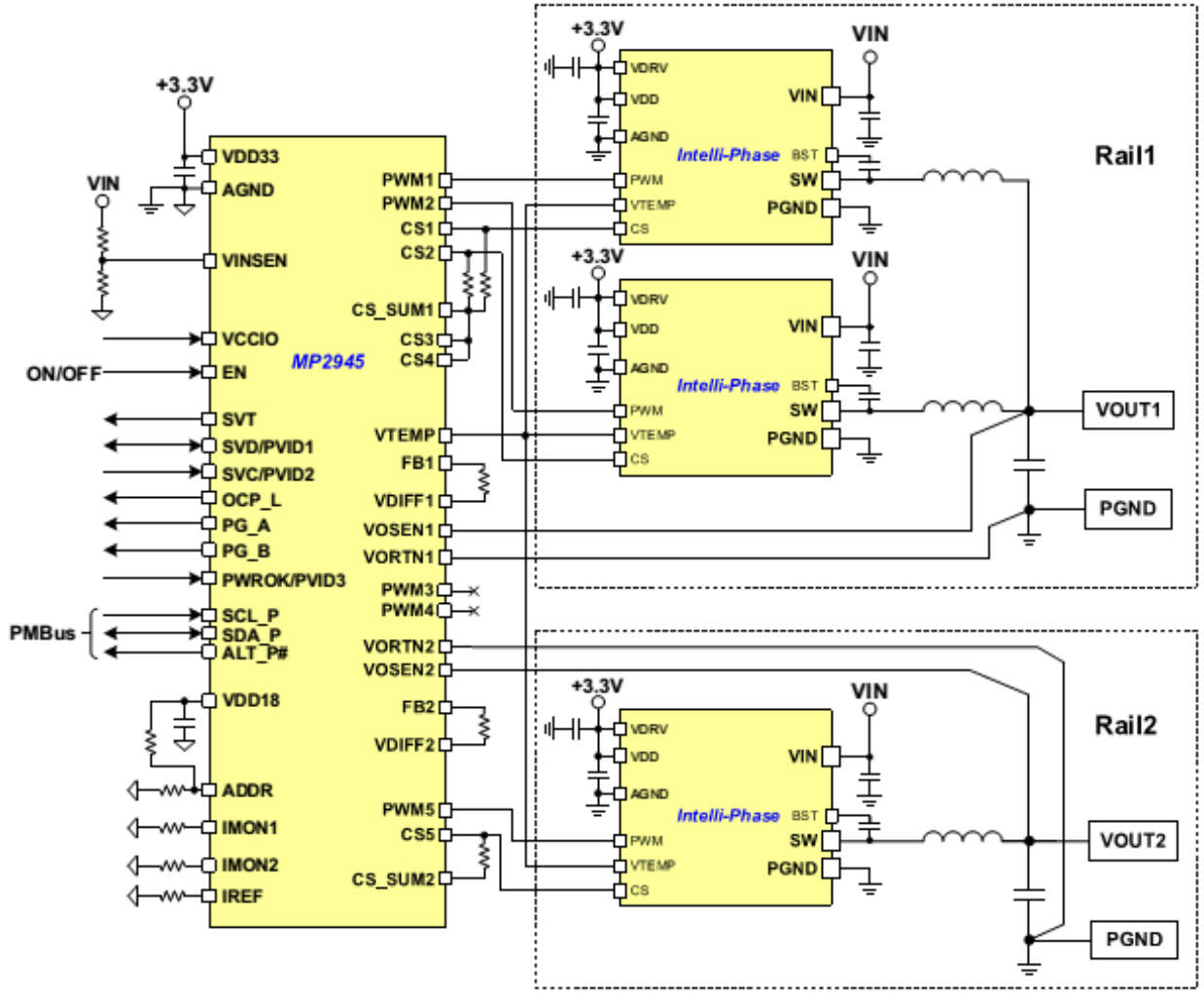
- Configurable Phase Number
- Intel IMVP8 and IMVP9 Compliant
- PVID Interface to Support VccAUX
- PMBus Compliant
- Serial VID Interface for Programming and Monitoring
- Built-In MTP to Store Customer Configuration
- Automatic Loop Compensation
- Auto Phase-Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing
- Input/Output Voltage and Power, and Output Current Monitoring
- Regulator Temperature Monitoring
- UVLO/OVP/UVP/OCP/OTP/RVP with Options of No Action, Latch, Retry, or Hiccup
- Digital Programmable Load Line
- RoHS Compliant 4x4 TQFN-28



Digital Controller Example : MP2945 (AMD SVI2)

FEATURES

- Multi-Phase, Dual-Output, Digital Controller
- AMD SVI 2.0 Compliant
- Supports 3-Bit PVID Mode
- PMBus™/I²C Compliant (1MHz Bus Speed)
- Pin Programmable for PMBus™ Address
- Built-In EEPROM to Store Custom Configurations
- Switching Frequency Range from 200kHz to 3MHz
- Digital Load-Line Regulation
- Over-Clocking Mode by Adding Offset to Output Voltage
- Automatic Loop Compensation
- Fewer External Components than a Conventional Analog Controller
- Best Transient Performance with Non-Linear Digital Control
- Flexible Phase Assignment for Dual Rails
- Auto-Phase Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Programmable Offsets for Thermal Balance
- Input and Output Voltage, Current, and Power Monitoring
- Regulator Temperature Monitoring
- V_{IN} UVLO, Output OVP/UVP, OCP_TDC/OCP_SPIKE, OTP with No Action, Latch, Retry, or Hiccup Options
- Detection for Intelli-Phase MOSFET Fault Type
- Auto-Recording VR Fault Type to EEPROM
- Available in an RoHS Compliant QFN-40 (5mmx5mm) Package



MP2945
5-phase/2rail Controller
5x5 PKG

MP2845
6-phase/4-rail SVI3
Next Gen AMD

AMD Has Chosen MPS As SVI3 Development Partner!

DrMOS Examples

50A

25A

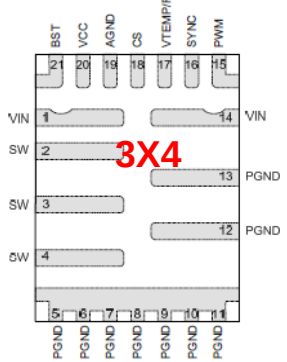
12A

12V

16V

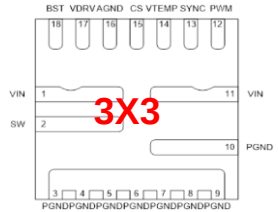
22V

MP86902B



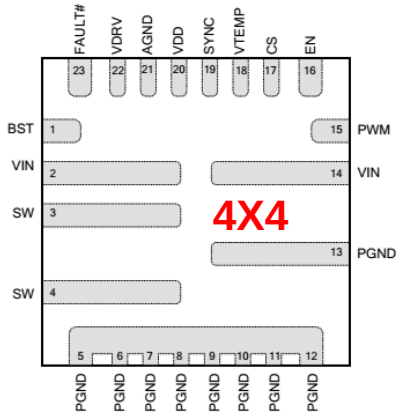
3-12V / 35A

MP86902A



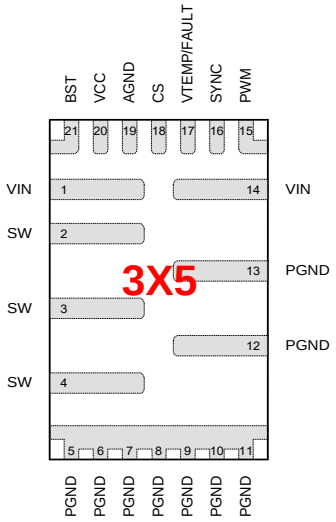
3-12V / 15A

MP86909



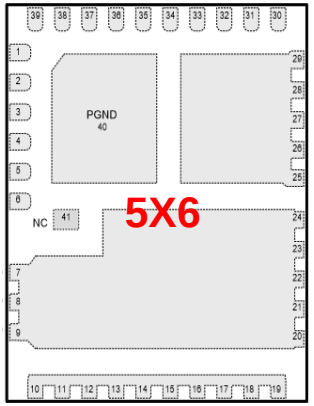
4.5-16V / 50A

MP86941/71 (w/PFO)



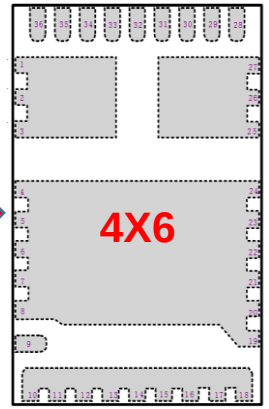
4.5-22V / 30A

MP86979



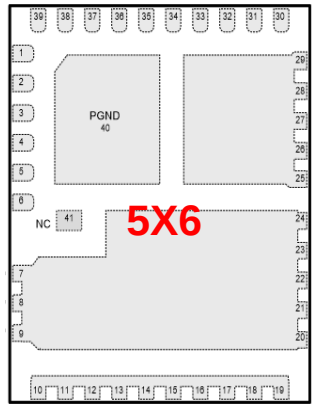
5X6 CF Version of MP86949

MP86949



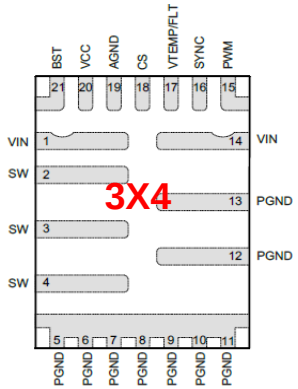
4.5-22V / 45A

MPQ86940



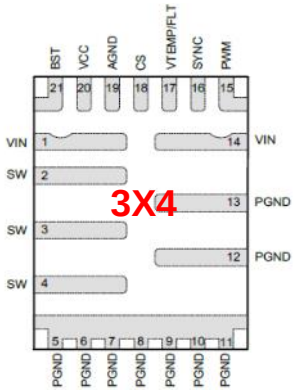
3-22V / 40A

MP86901C



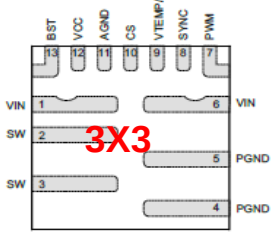
4.5-22V / 30A

MP86901B



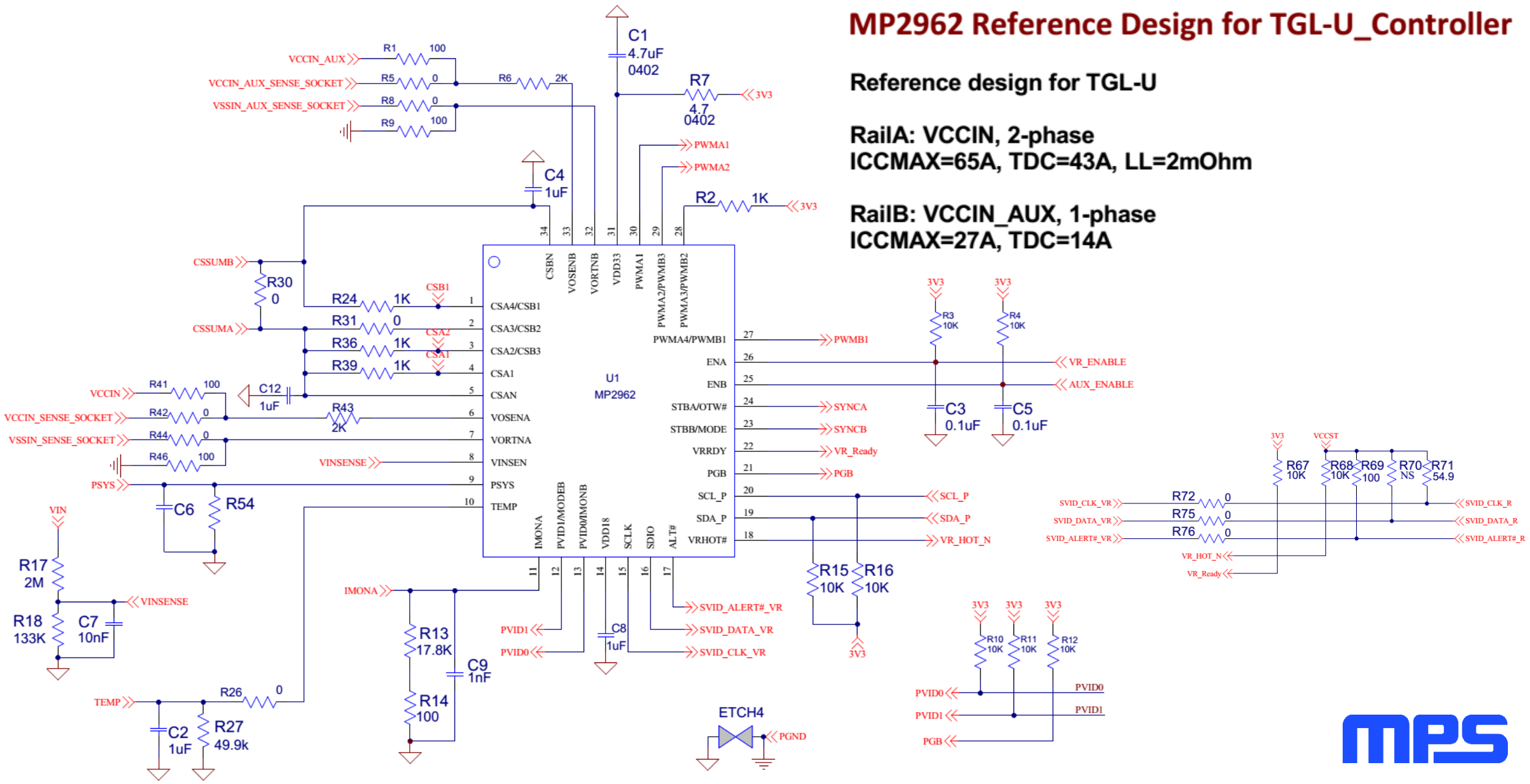
4.5-22V / 20A

MP86901A

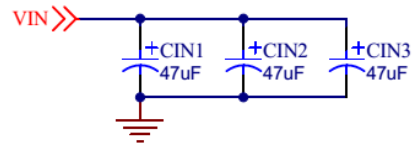


4.5-22V / 12A

Intel TGL-UP3 Design Example (VCCIN, VCCIN_AUX)

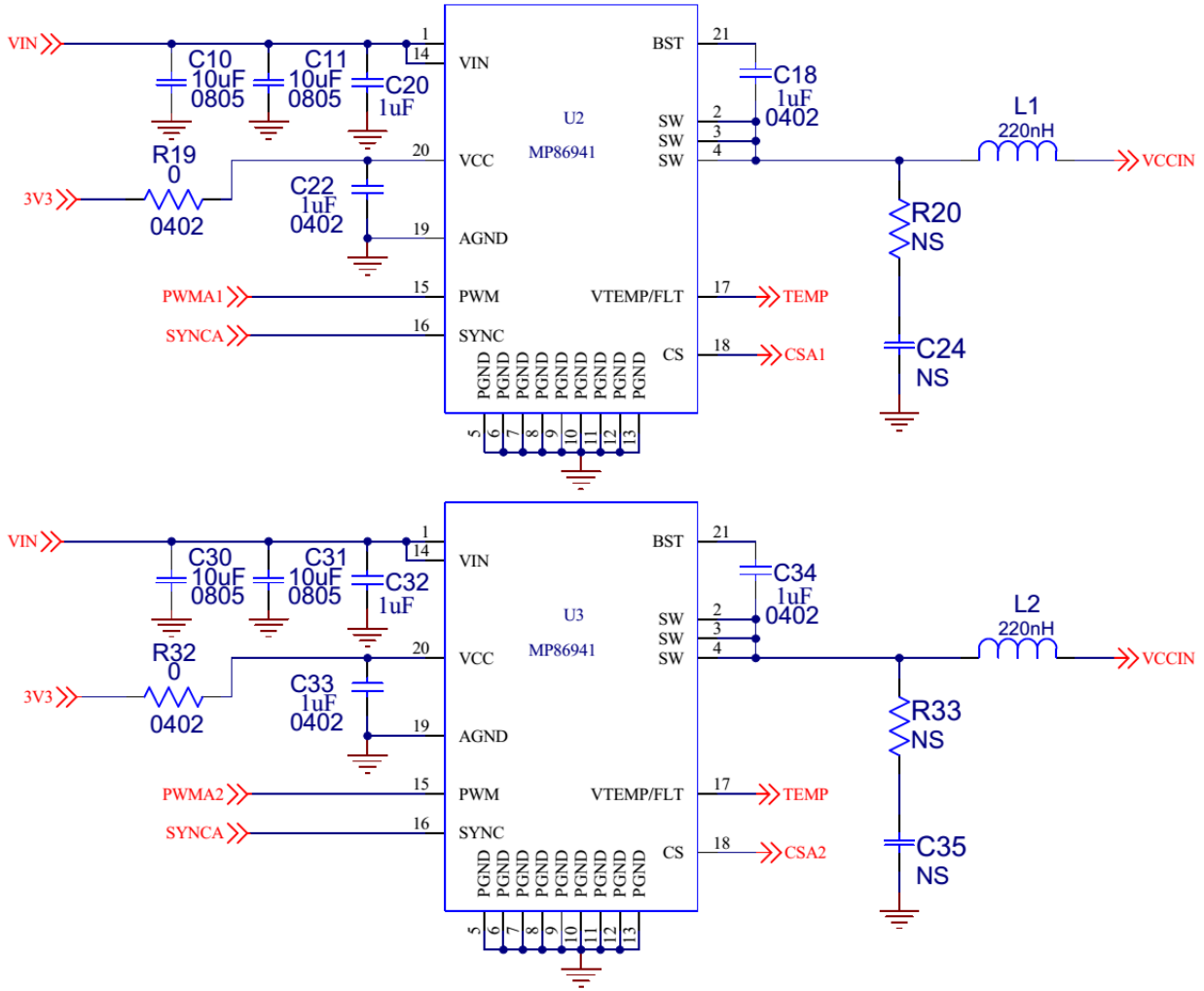


Intel TGL-UP3 Example (VCCIN, VCCIN_AUX)

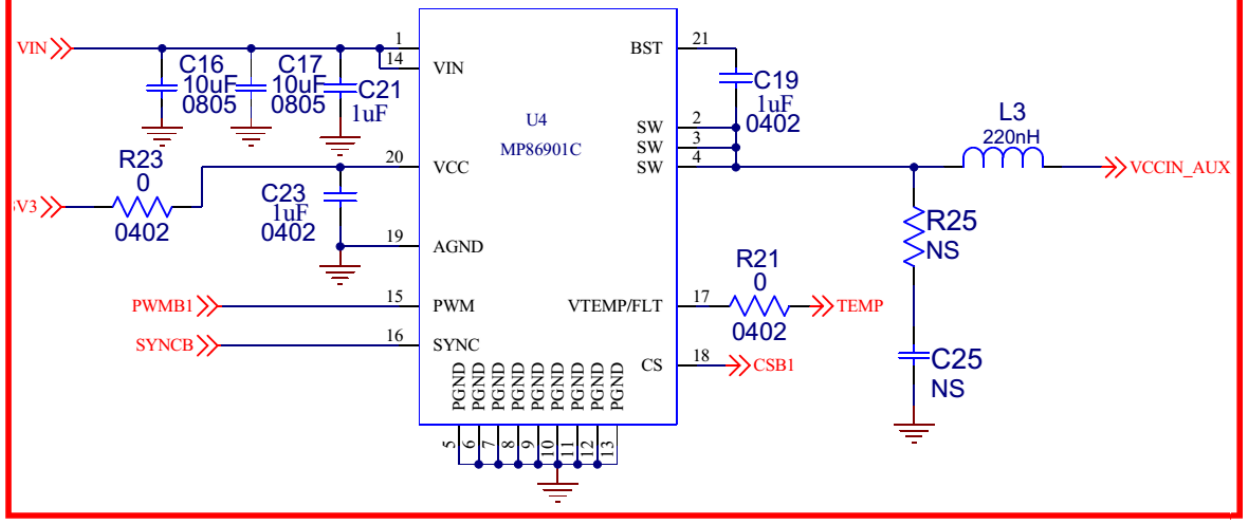


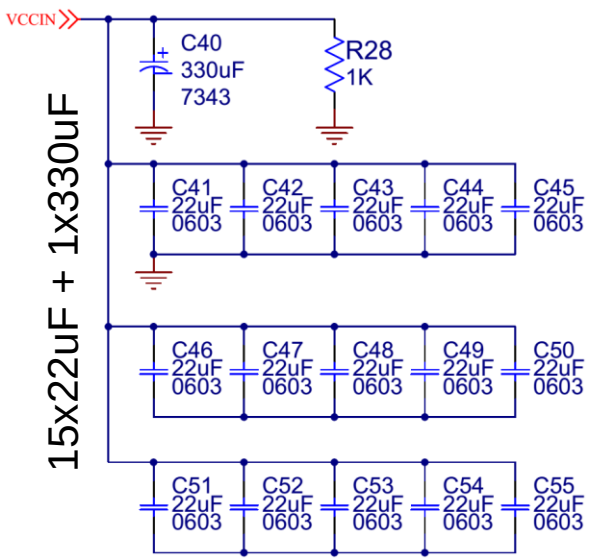
3x47uF Bulk Capacitance at the input

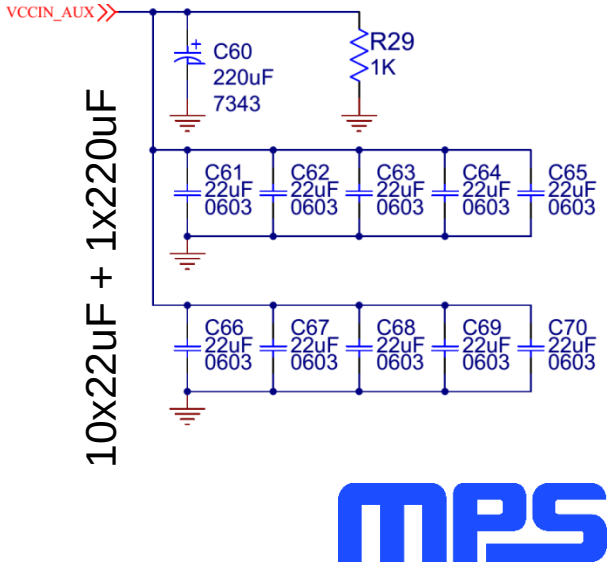
VCCIN Power Stage



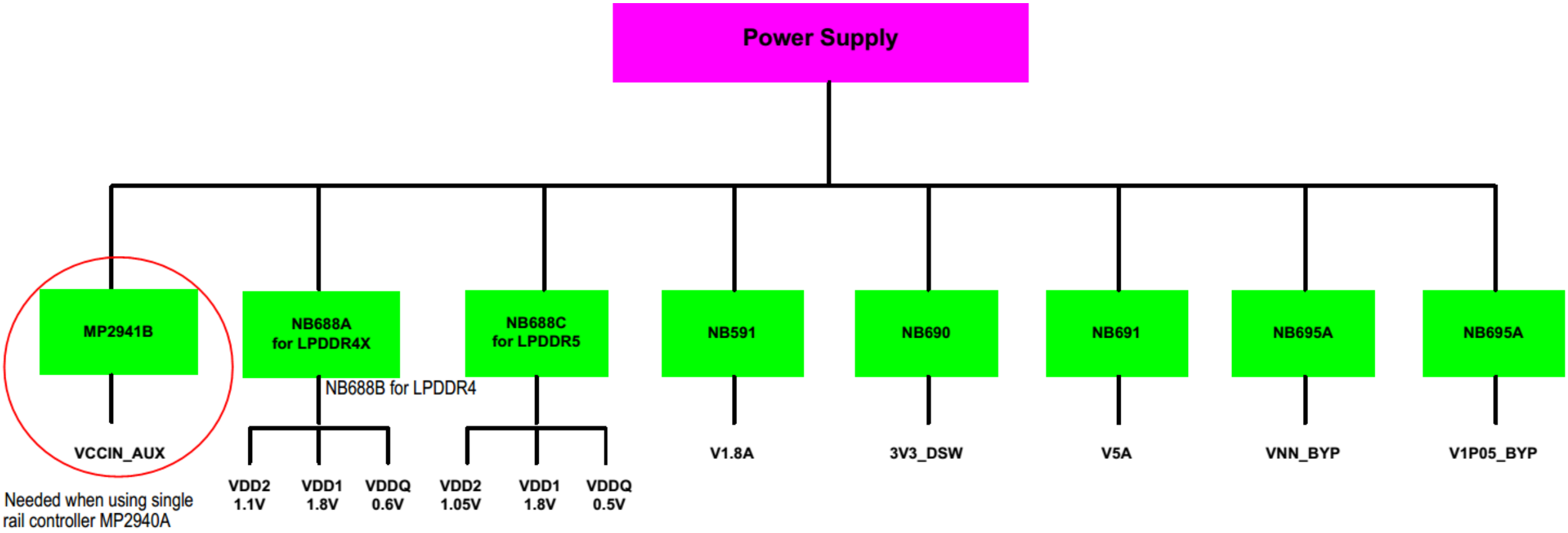
VCCIN_AUX Power Stage







Intel TGL-UP3 Example (Other Rails)



Summary – Q&A

- Complete Power Solution from a single vendor
- Digital Controller eases design process and verfication
- Fast Control Loop allows reduction of output capacitors to fullfill ripple/transient specifications
- High efficiency Monolithic DrMOS devices with low thermal resistance Flip-Chip packages supports space constraints designs
- Accurate DrMOS on-die current sense leads to better overall system performance and much less engineering effort (no inductor DCR sensing and temperature compensation required)
- Design Support (initial controller configuration, layout guides, schematic/layout review)
  Reduces risk and saves development time