Driving Power MOSFETs

Pete Millett

Senior Technical Marketing Engineer

September 2020

Pete Millett – Senior Technical Marketing Engineer

2014–Present

- MPS Senior Technical Marketing Engineer for motor driver ICs
- Responsible for new product definitions as well as application engineering

2005–2013

- Systems Engineer and Systems Manager at Texas Instruments
- Product definition and systems engineering for motor driver ICs (DRV8XXX)

1982–2005

- Board-level hardware design engineer at various computer and consumer electronics companies

Driving power MOSFETs

MOSFET Basics

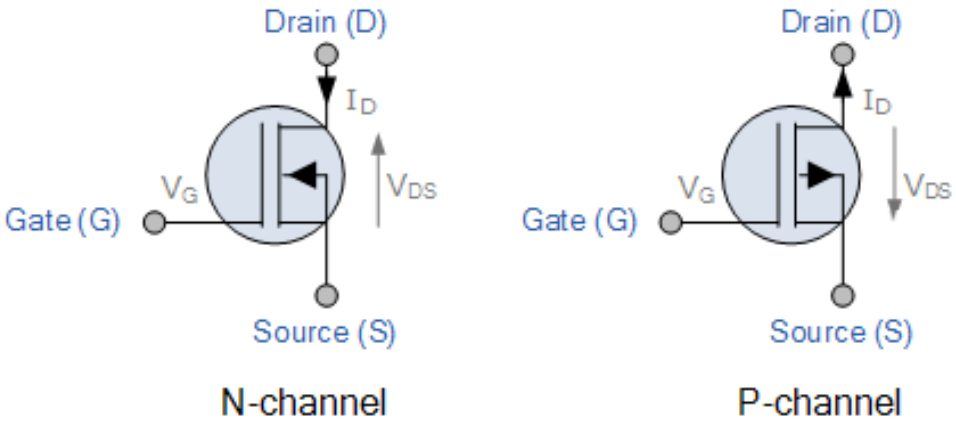
Driving Loads: H-Bridges and Half-H-Bridges

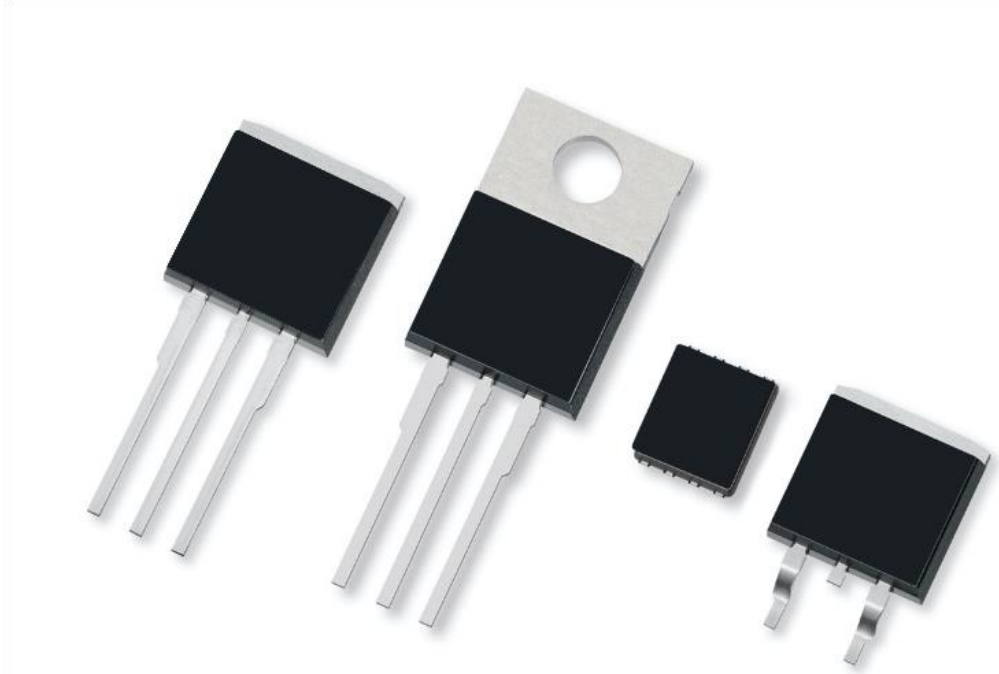
Driving the Gate

Effects of MOSFET Switching Speed

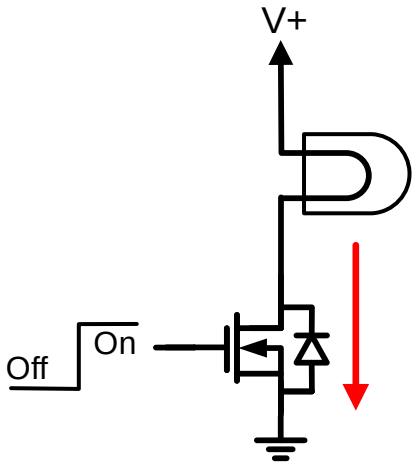
Conclusion

Power MOSFETs

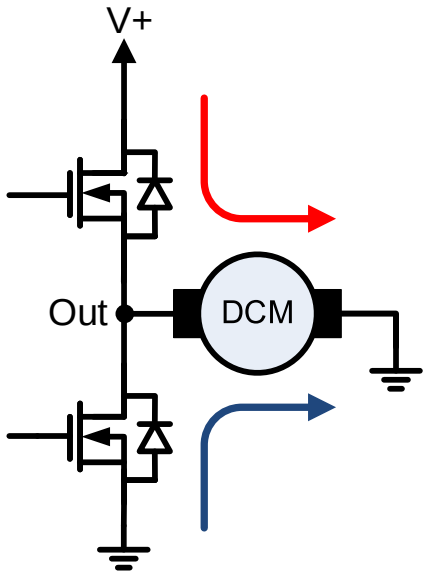




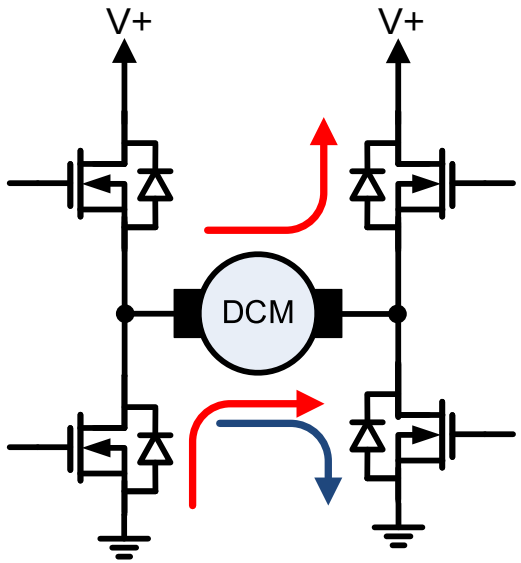
Power Drive Circuits



Low side



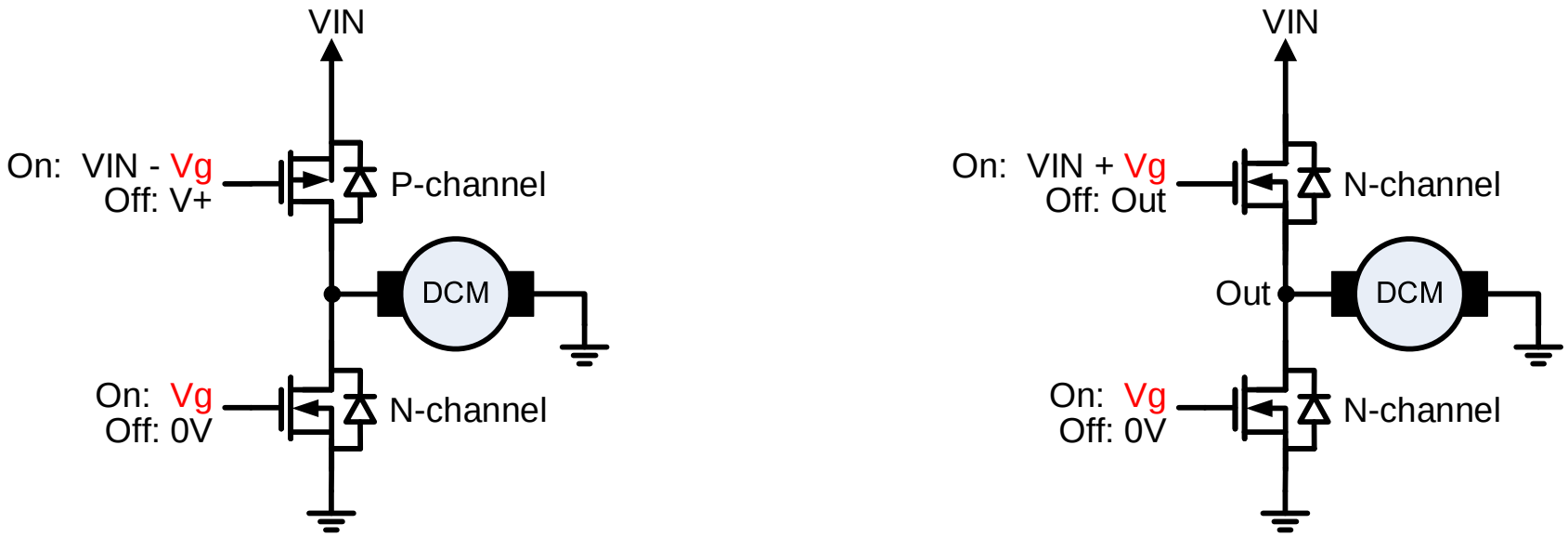
Half Bridge



H-Bridge

Red: PWM On
Blue: PWM Off

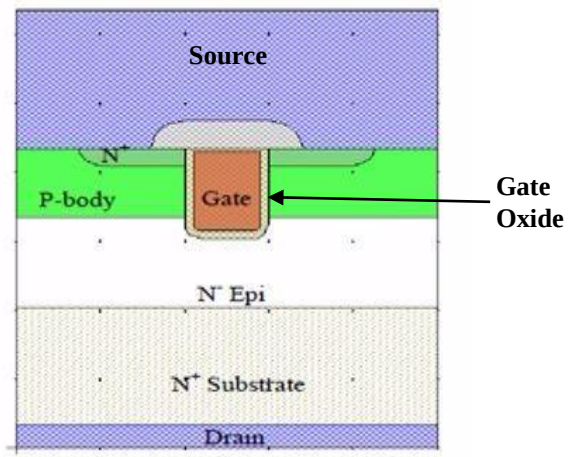
Half Bridges: N and P

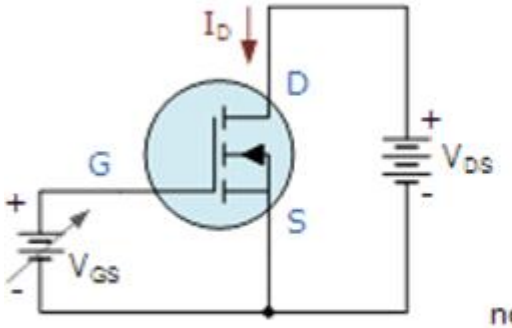


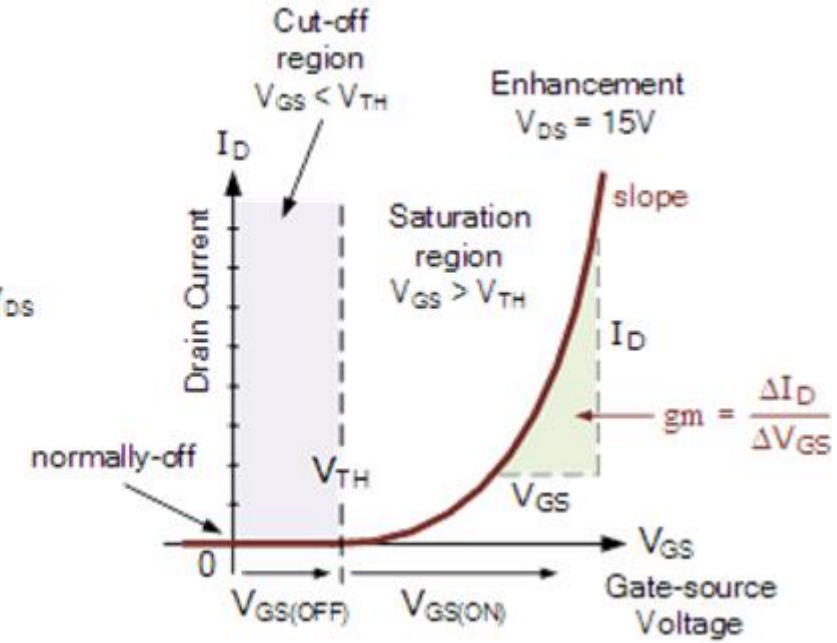
VIN – Load Supply Voltage

VG – Gate Drive Voltage

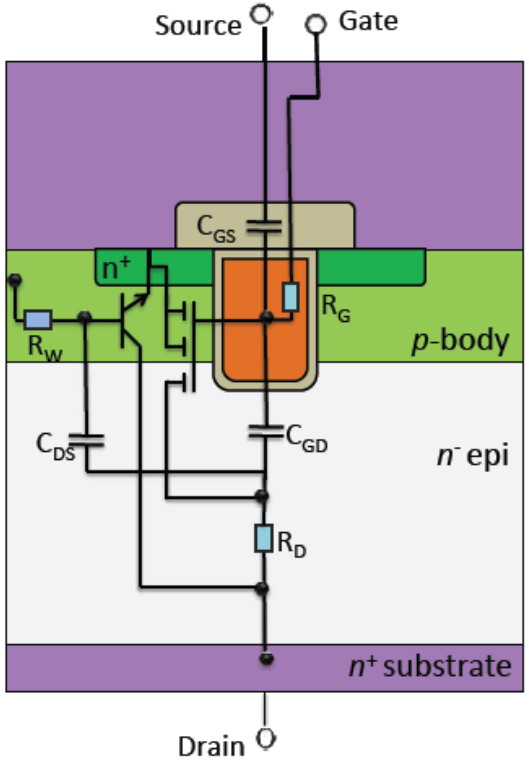
MOSFET Structure

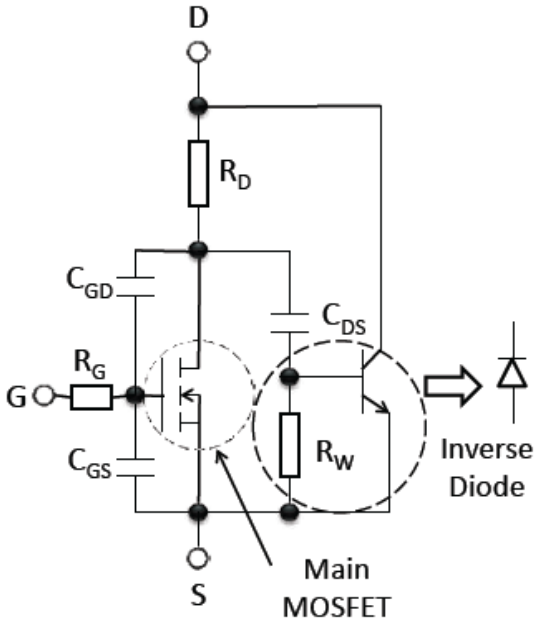






Simplified Model of an N-channel Power MOSFET





Datasheet Specs and Total Gate Charge

$$1 \text{ Coulomb} = 6.28 \times 10^{18} \text{ Electrons}$$

that is:

6,280,000,000,000,000,000

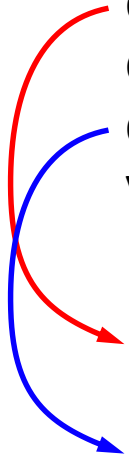
ELECTRONS

Q = CV (Charge = Capacitance x Voltage)

I = Q/t (Current = Charge / Time)

IPP015N04N

VDS	max	40.0 V
RDS (on) (@10V)		max 1.5 mΩ
ID (@25°C)	max	120.0 A
Ptot	max	250.0 W
Ciss		15000.0 pF
Coss		4000.0 pF
QG (typ @10V)		188.0 nC
VGS(th)	min / max	2.0 V / 4.0 V



C_{ISS} – Input capacitance (gate-to-source + gate-to-drain)

Q_G – Total gate charge

Driving the Gate

IPP015N04N

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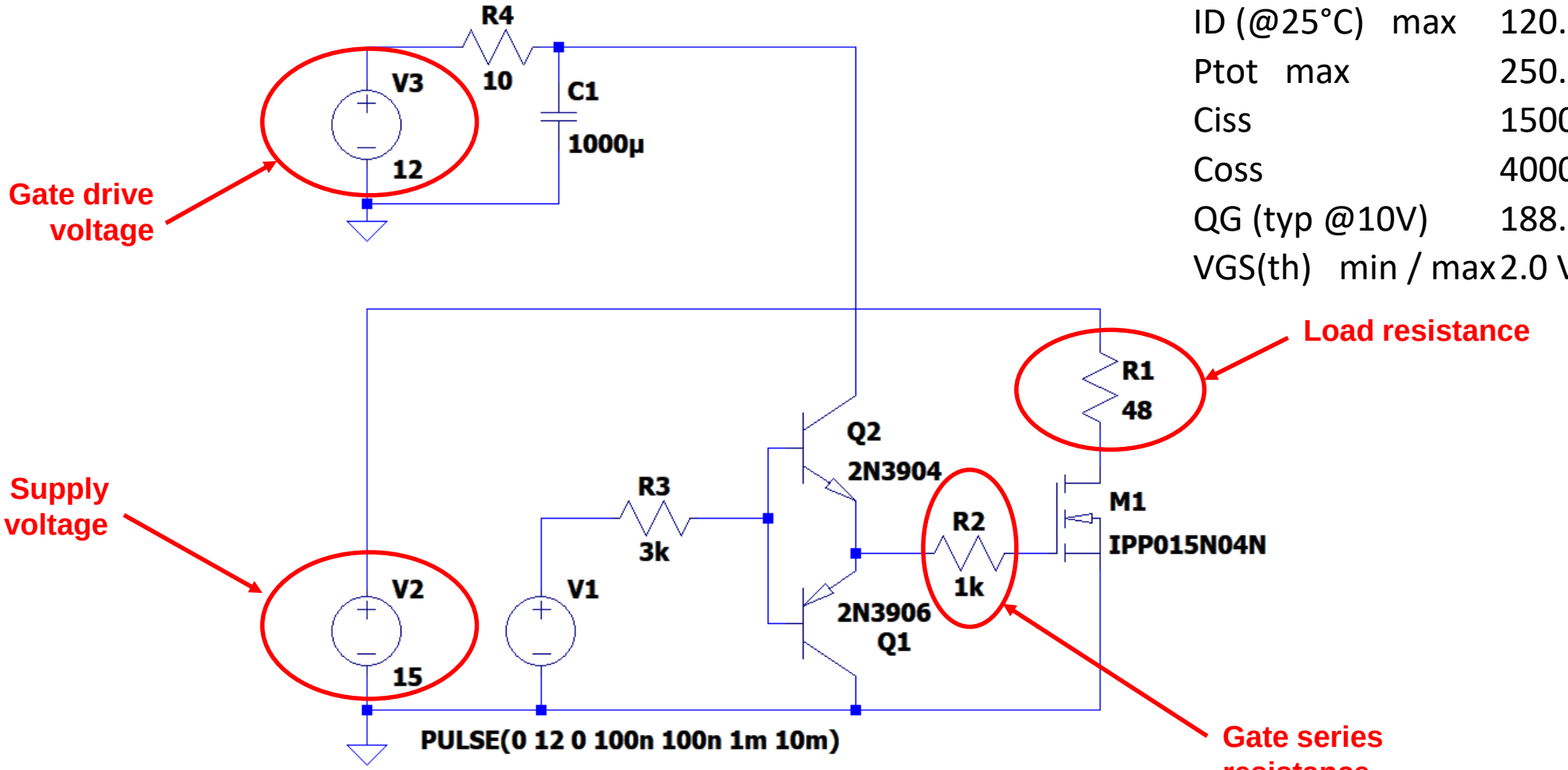
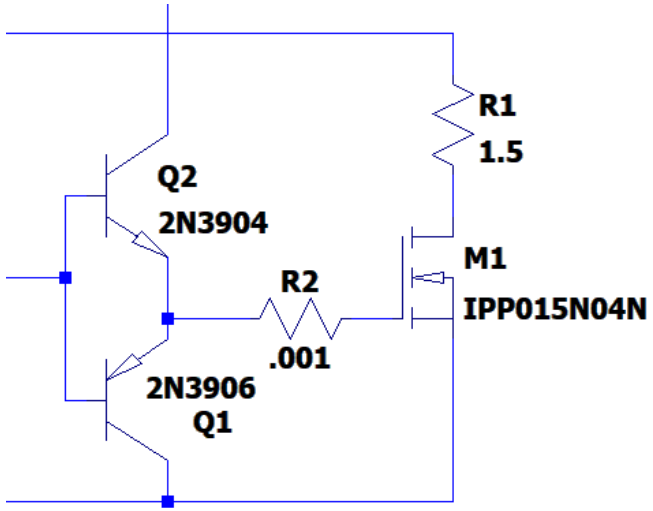
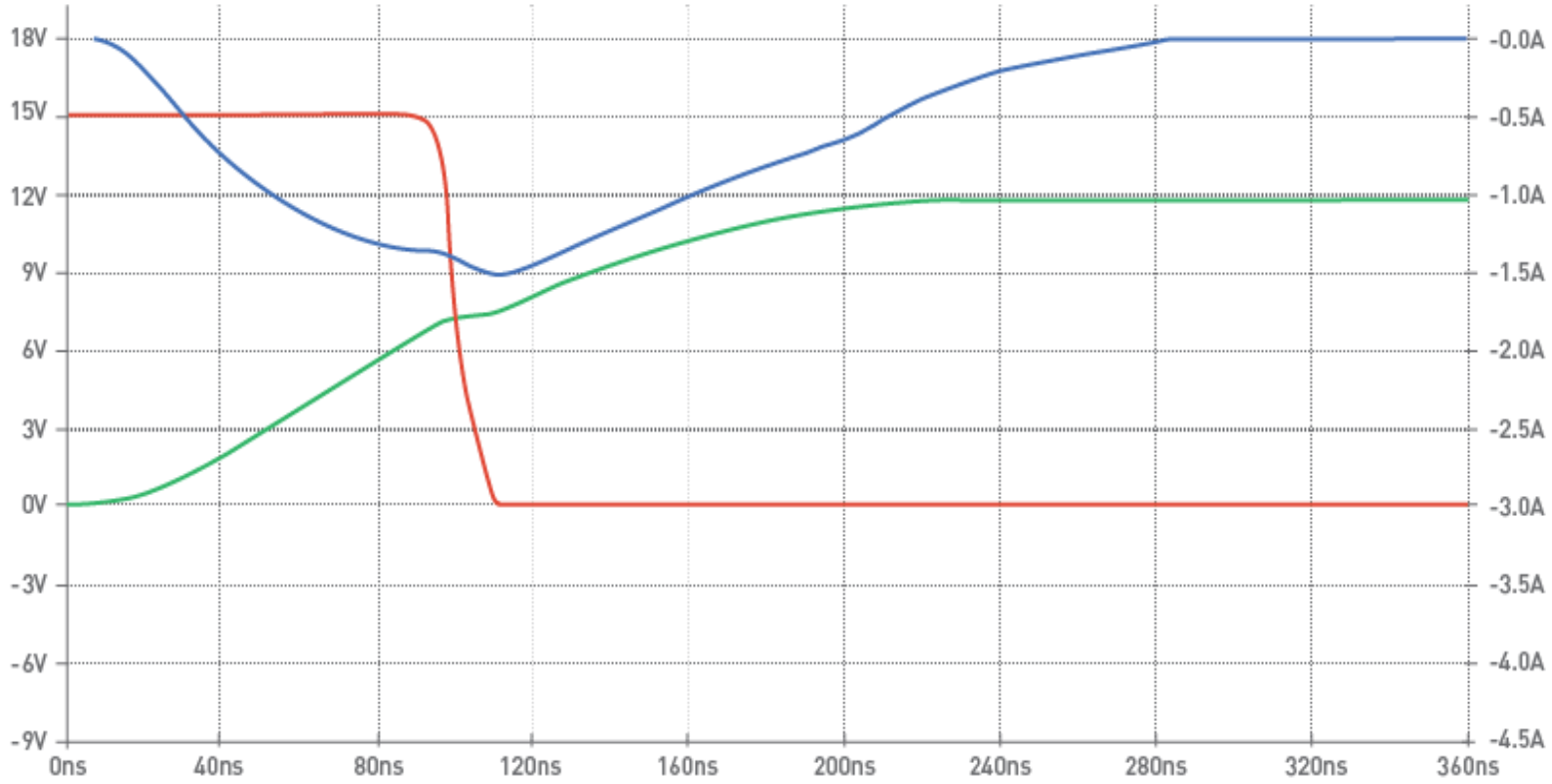


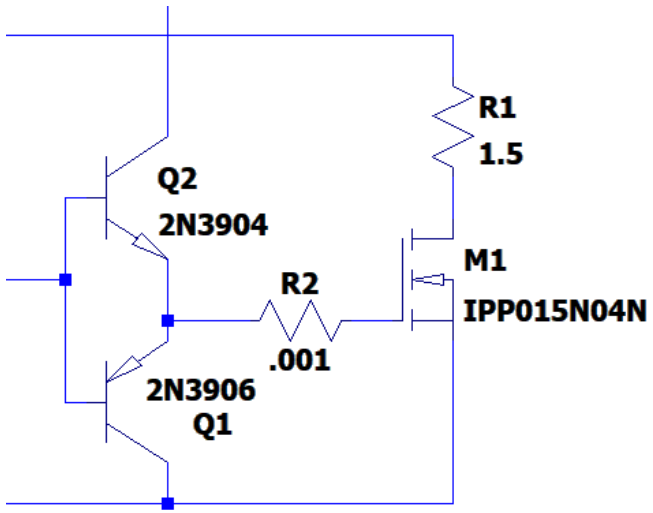
Low Resistance Gate Drive

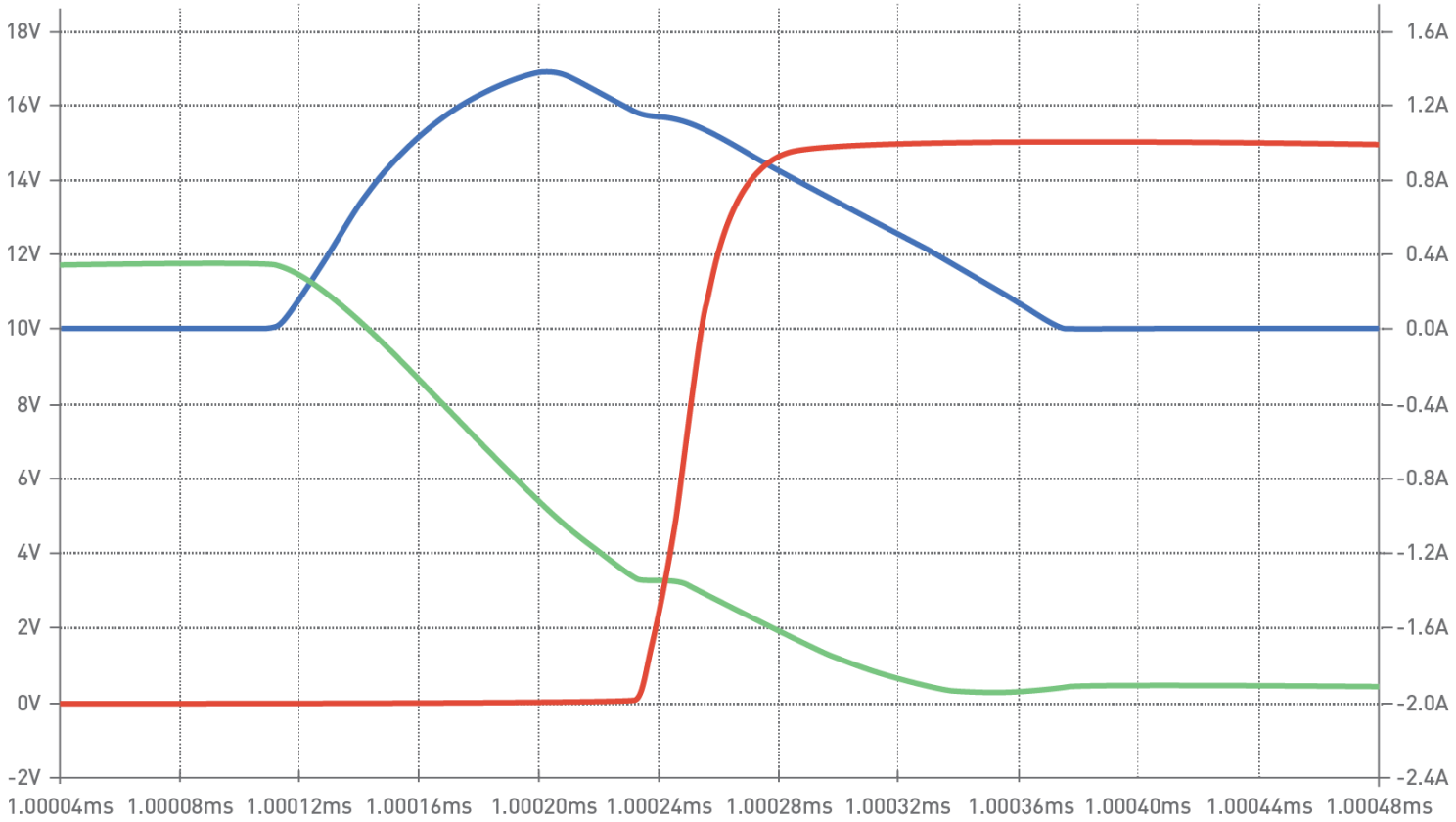




Red: Drain Voltage
Green: Gate Voltage
Blue: Gate Current

Low Resistance Gate Drive





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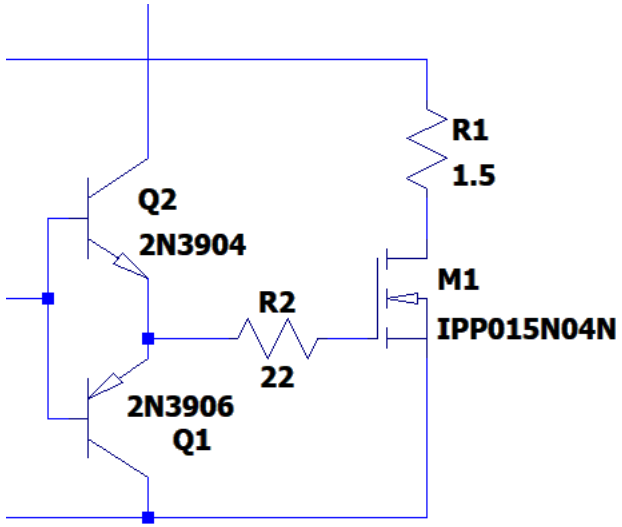
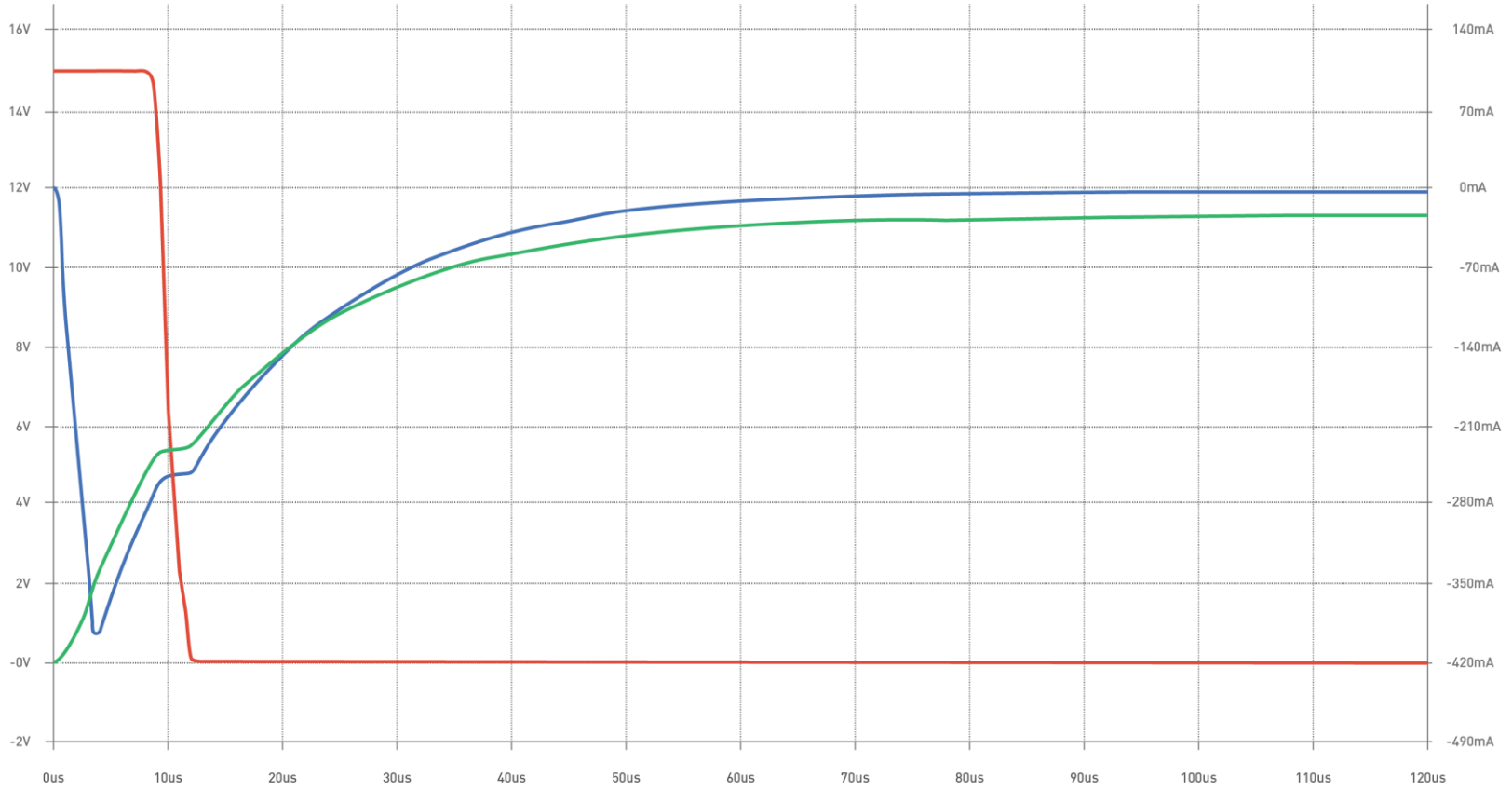
Adding Series Resistance





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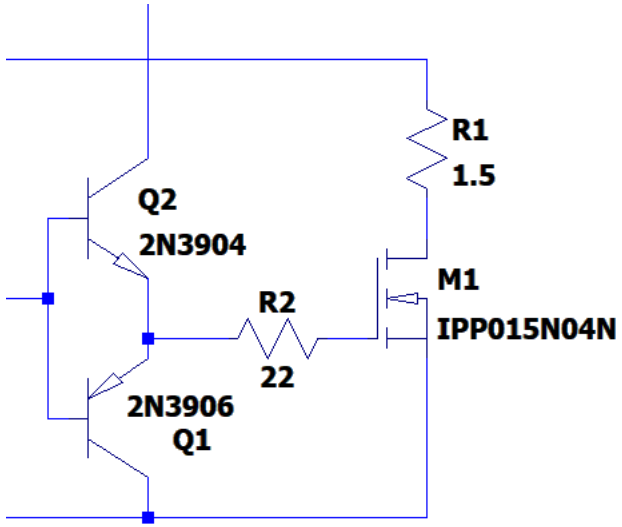

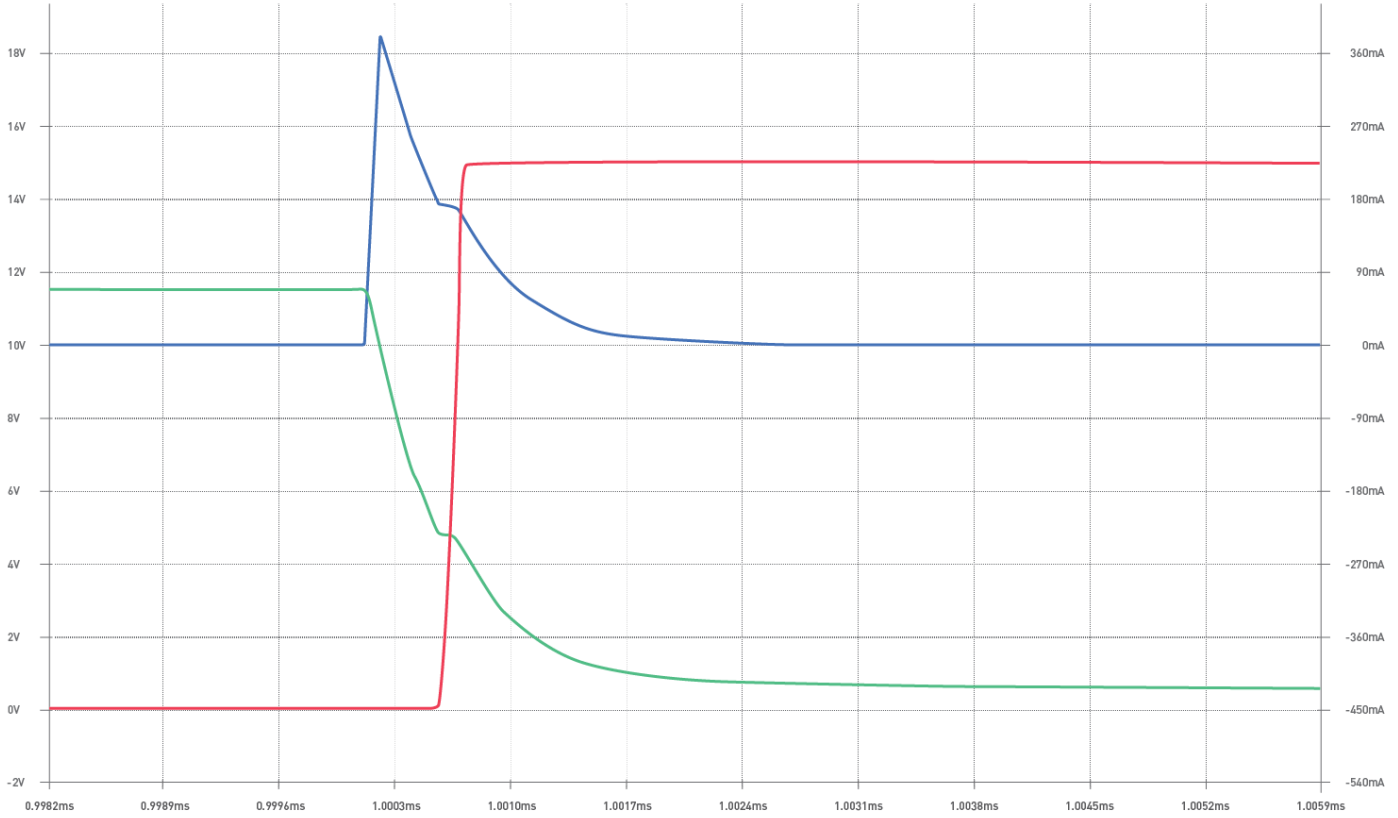

Red: Drain Voltage
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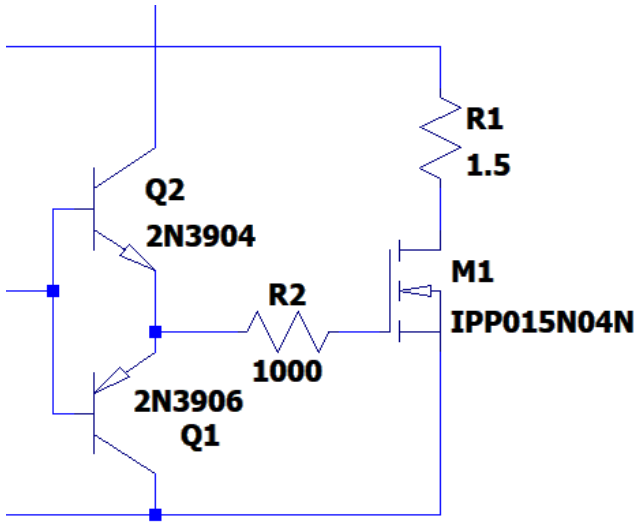
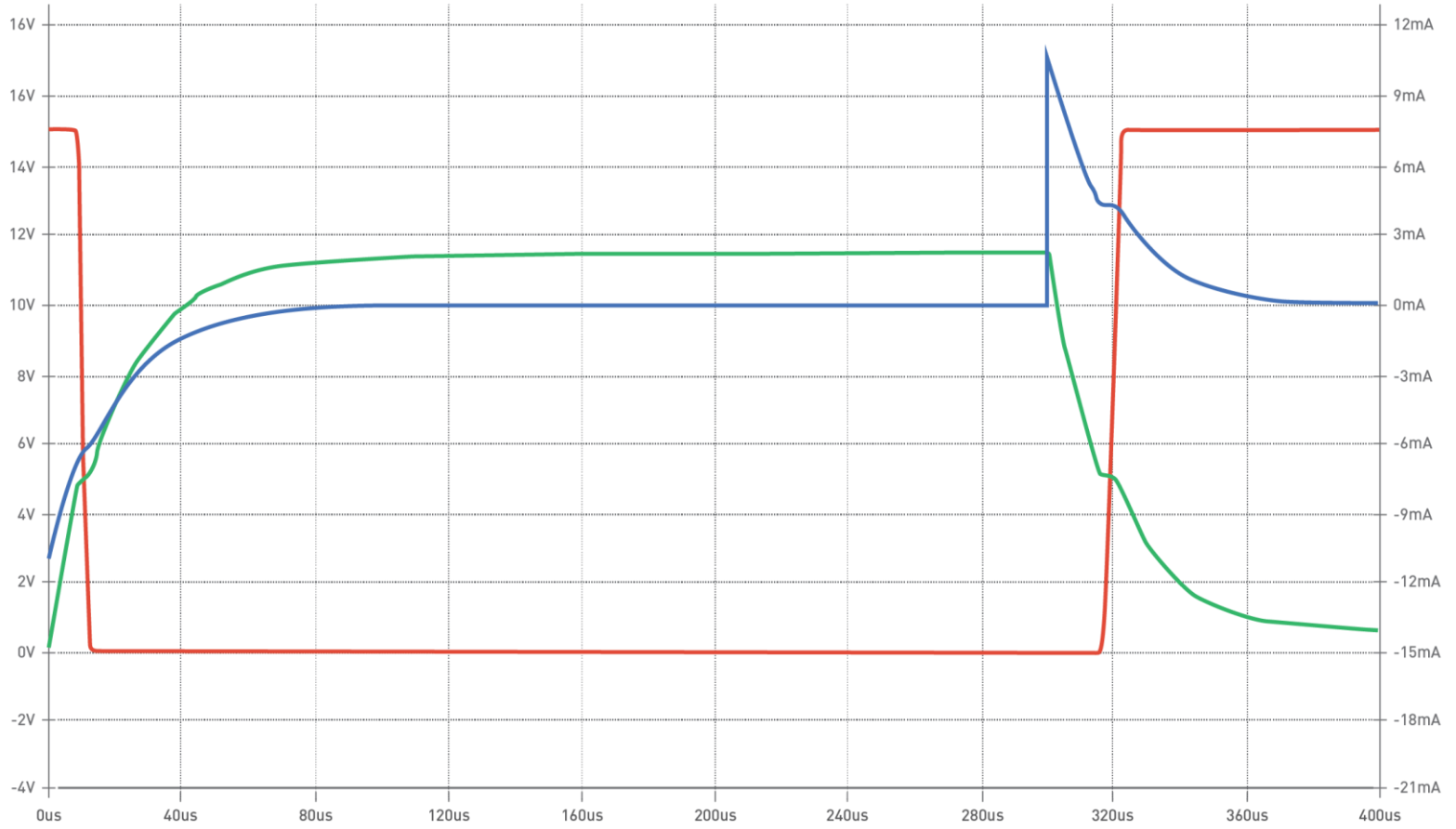
Blue: Gate Current

Too Much Series Resistance?





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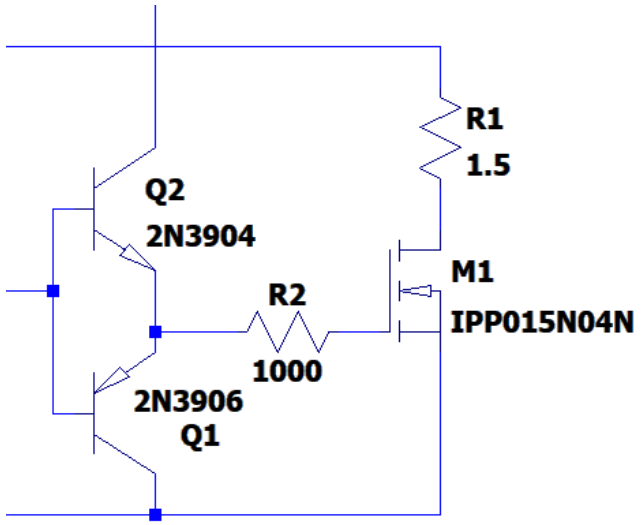
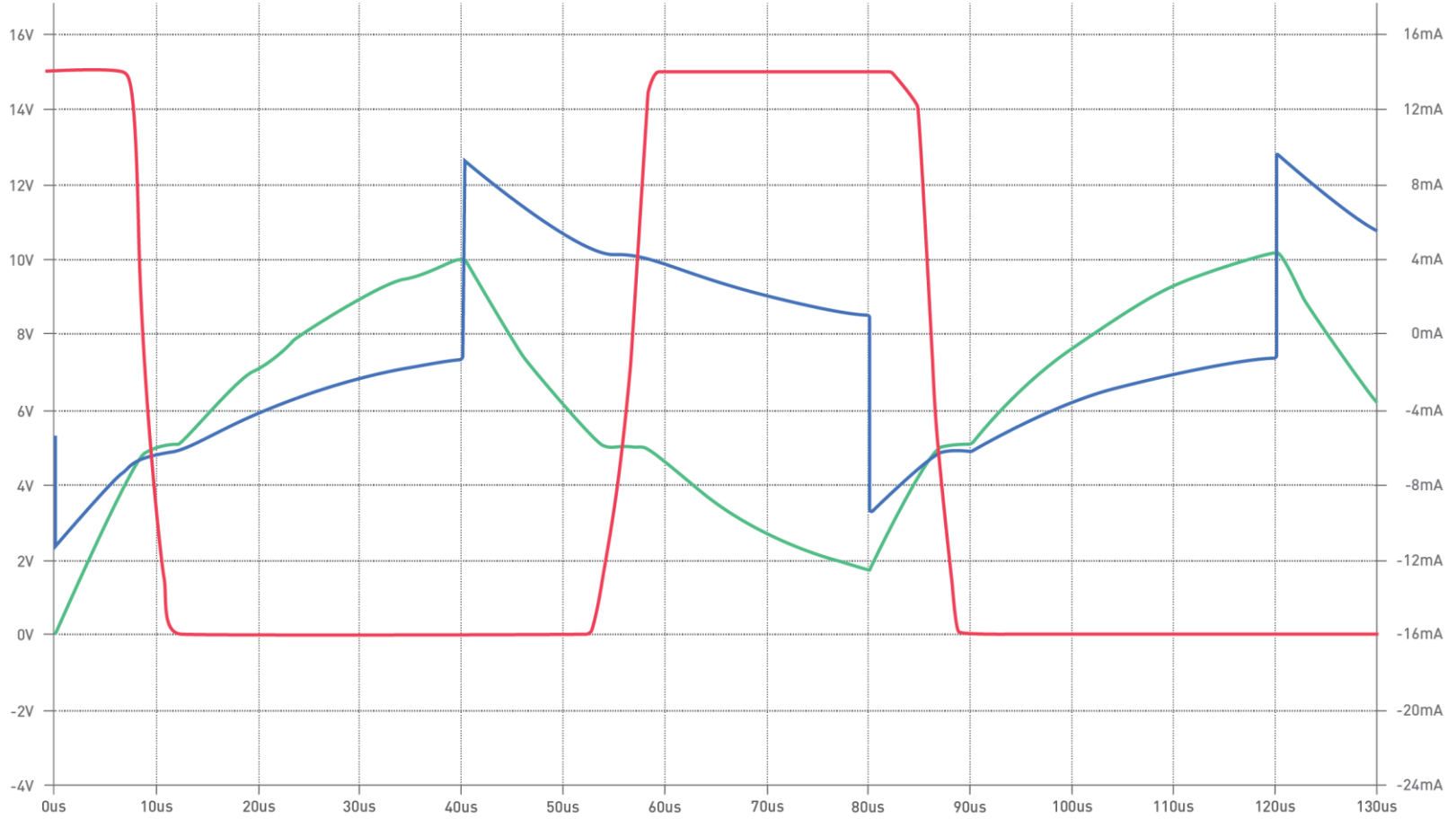
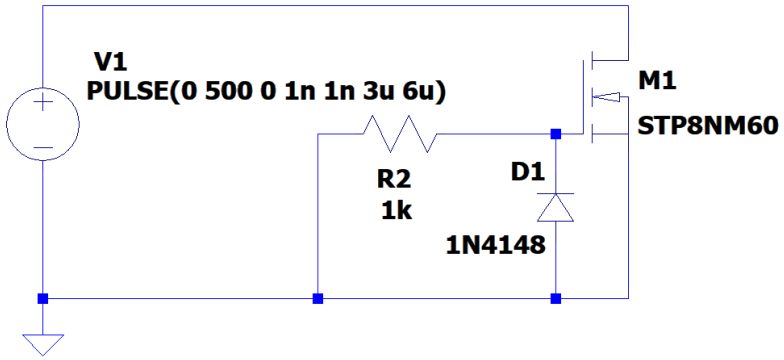
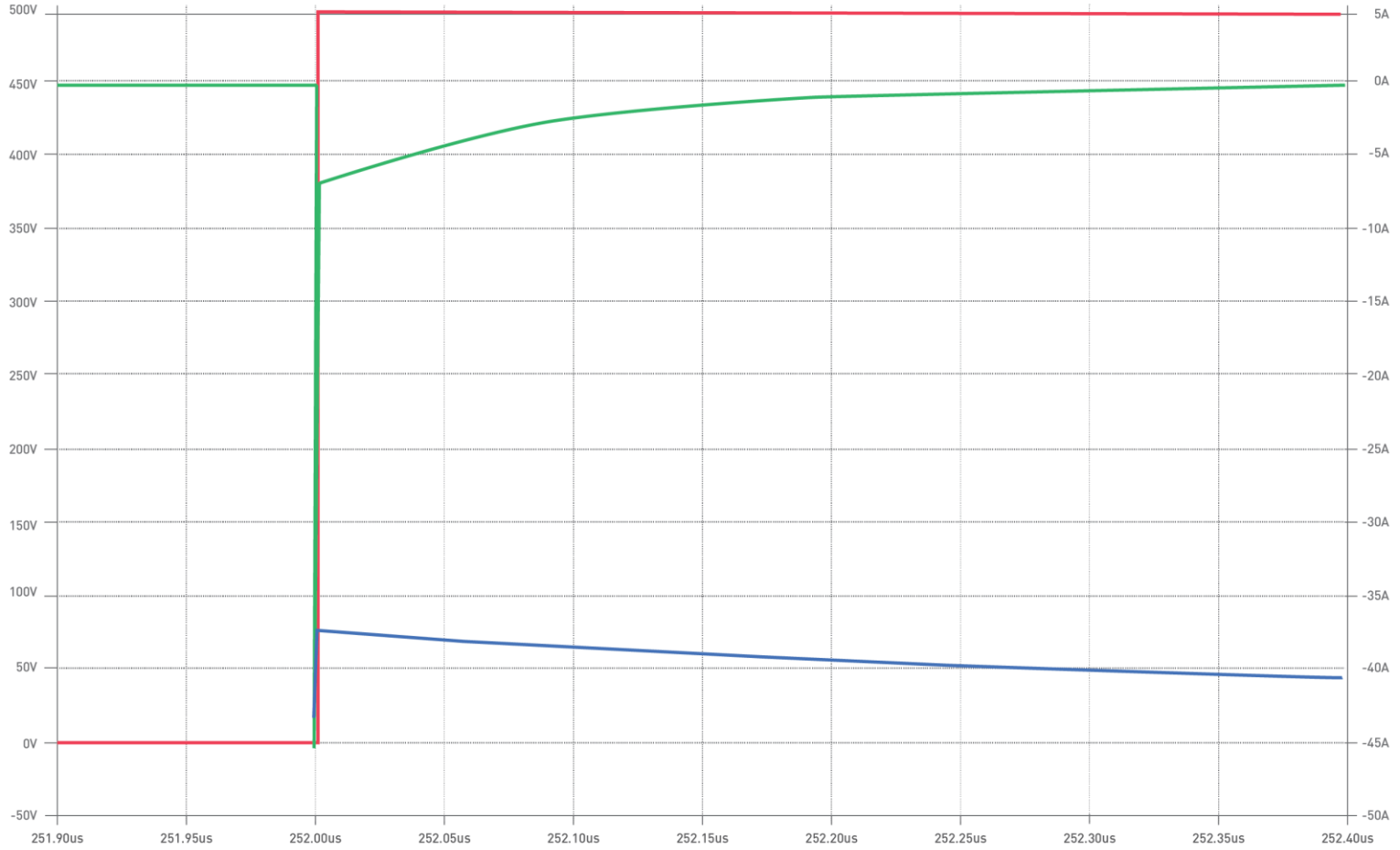




Red: Drain Voltage
Green: Gate Voltage
Blue: Gate Current

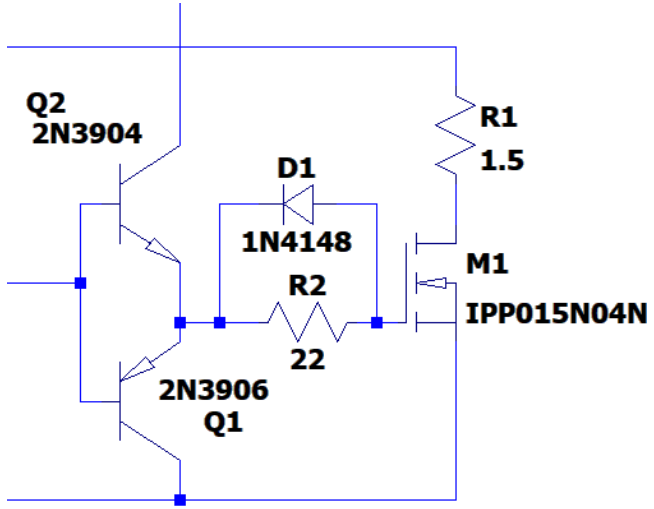
False Turn-On

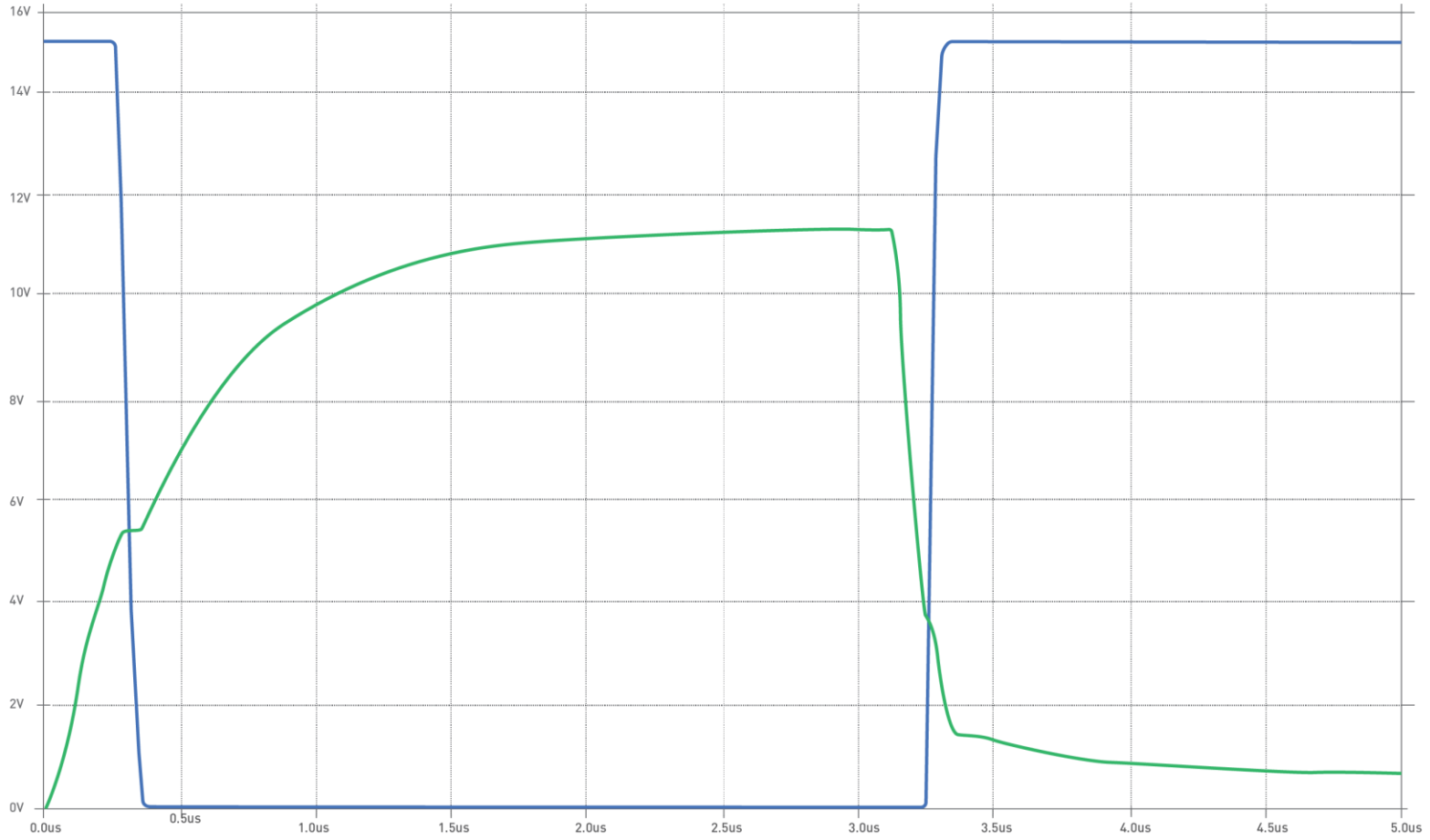




Red: Drain Voltage
Blue: Gate Voltage
Green: Drain Current

Asymmetric Gate Drive

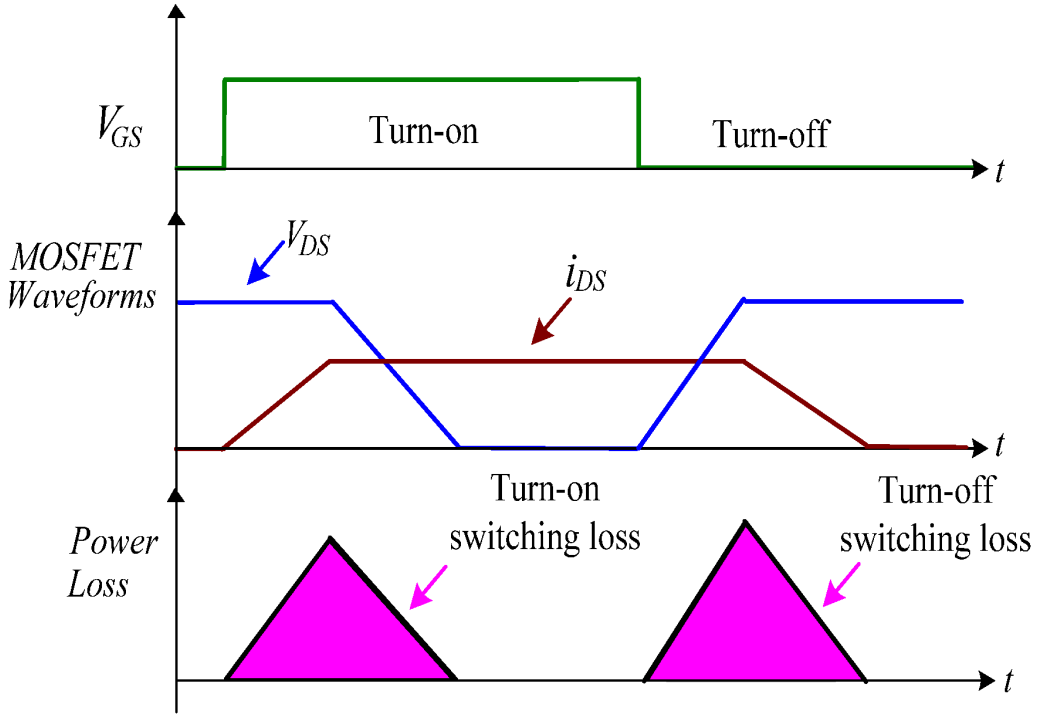




Blue: Drain Voltage

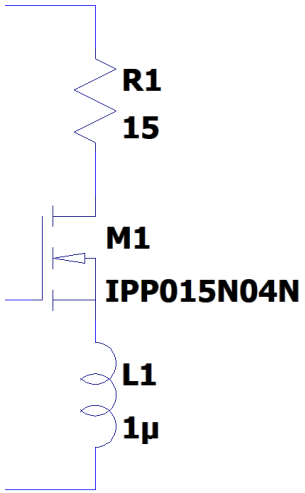
Green: Gate Voltage

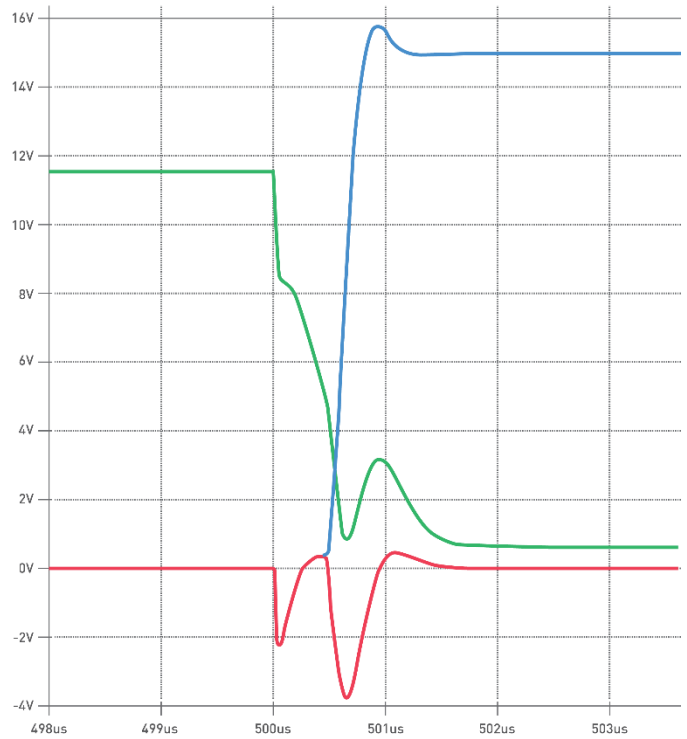
MOSFET Switching Speed



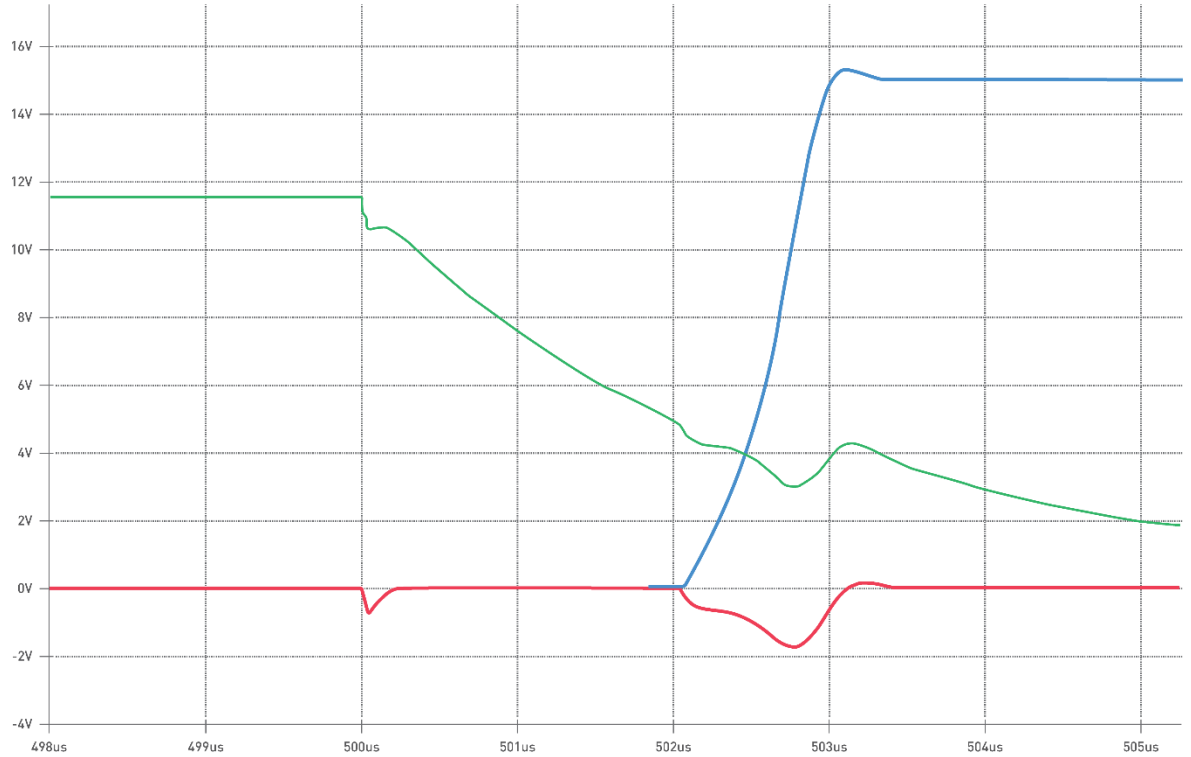
(a)

Why Slow the Gate Down?





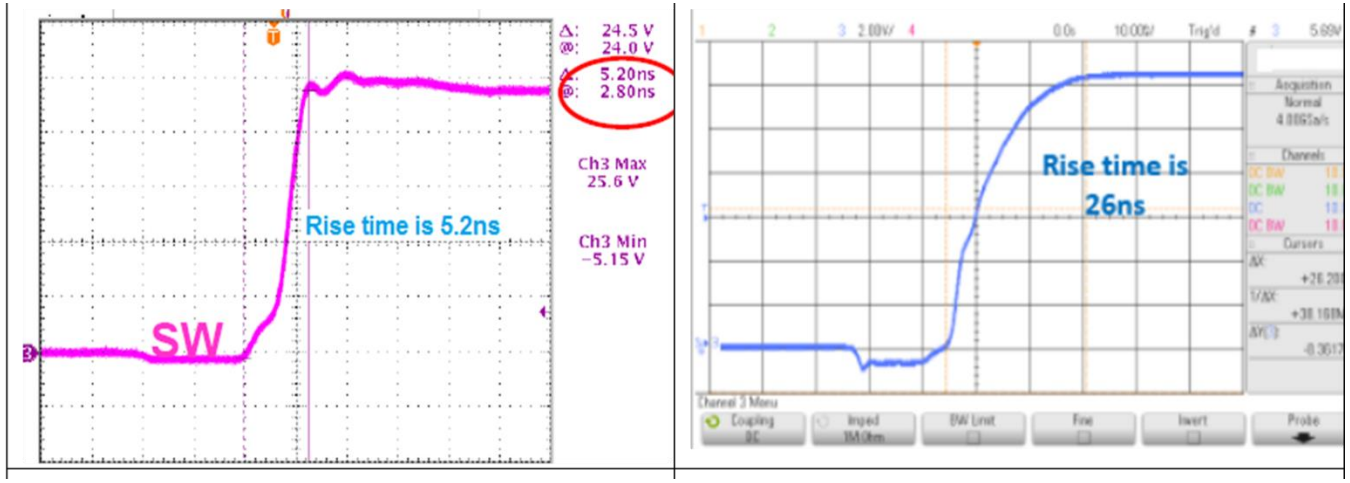
Fast

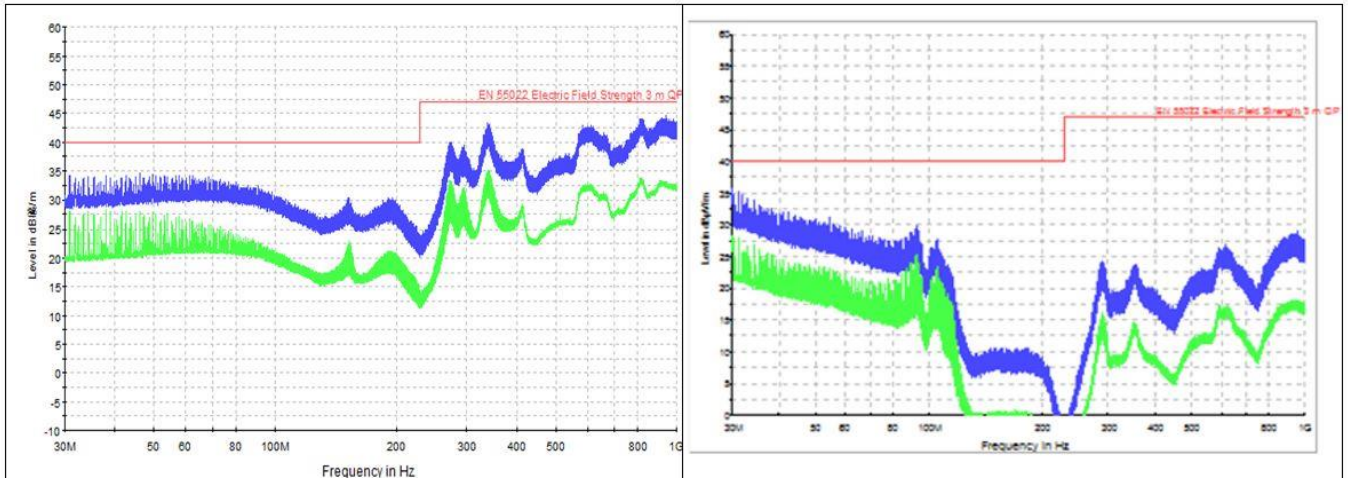


Slow

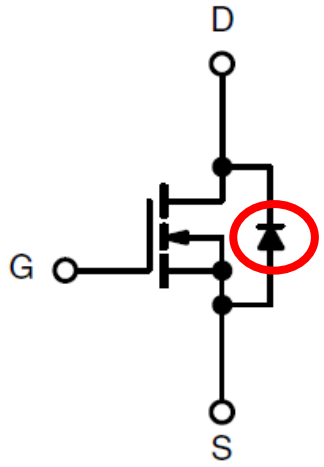
Green: Gate Voltage
Blue: Drain Voltage
Red: Source Voltage

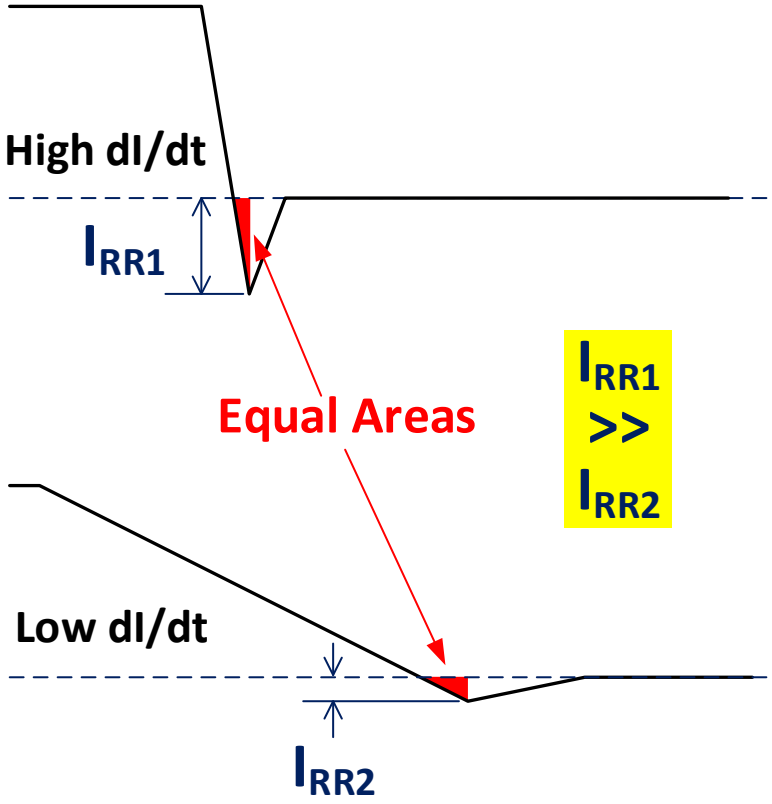
EMI Concerns

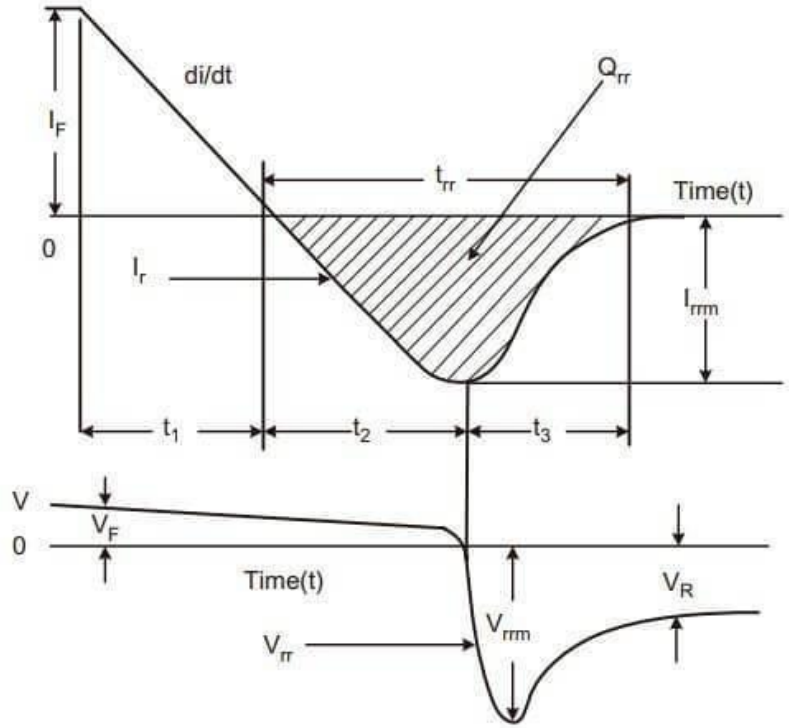




Body Diode Reverse Recovery







Summary

- Key takeaways:
  - Understand how MOSFETs work to implement a successful power circuit
  - Optimize the gate drive to control slew rate, transients, and EMI
  - Carefully design the PCB with consideration of parasitic inductances and impedances

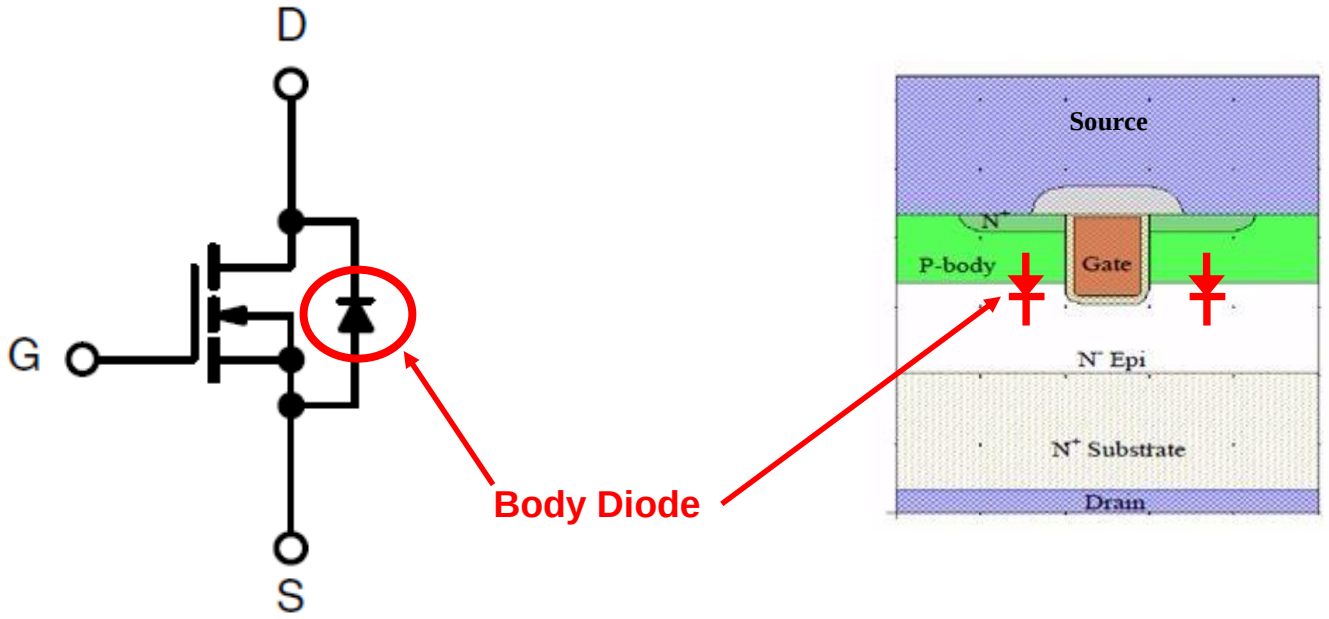
Q&A

Please submit questions through the “Q&A” menu option in the Zoom app

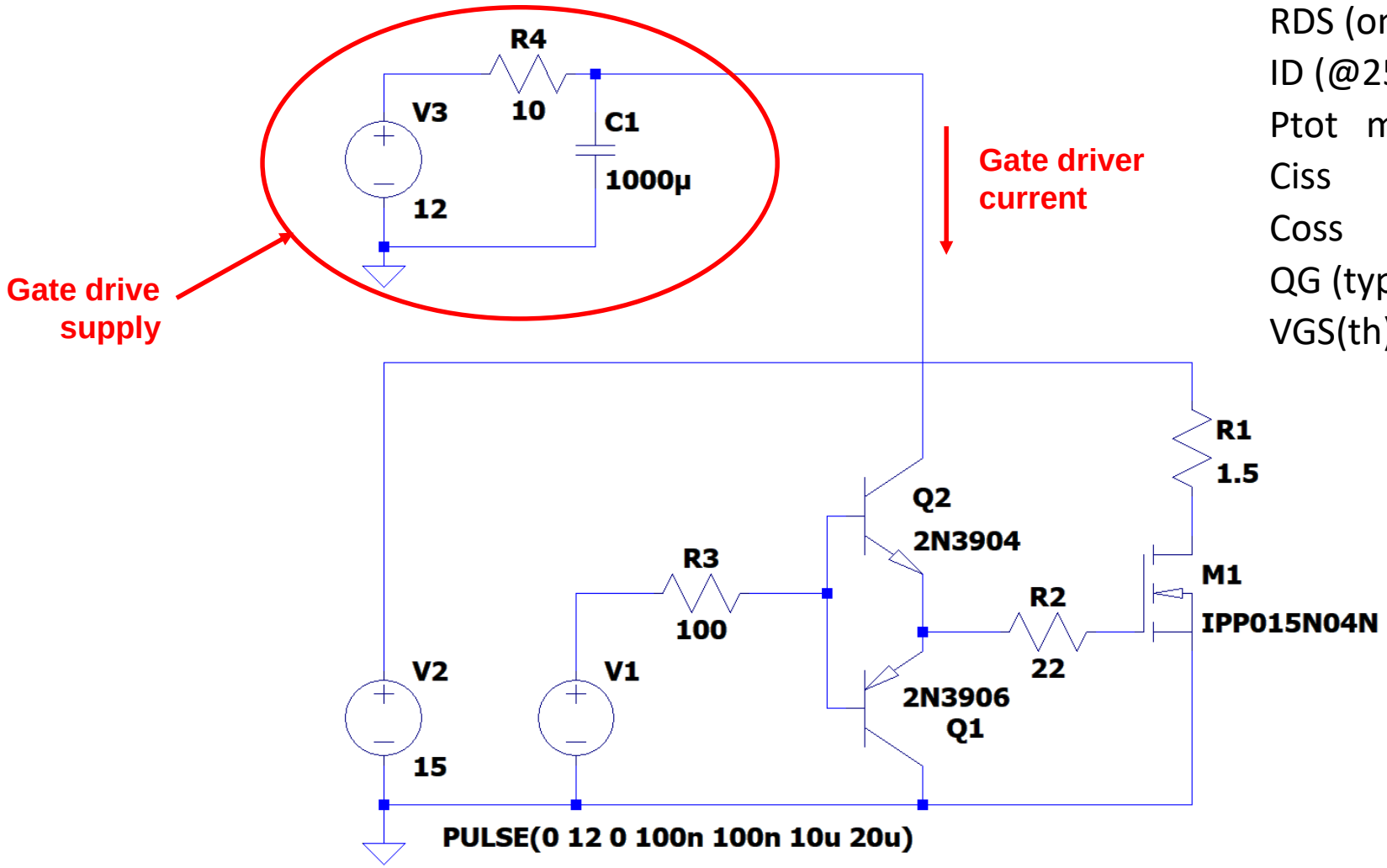
This webinar and others will be available for on-demand streaming at:

MonolithicPower.com/webinars

The Body Diode



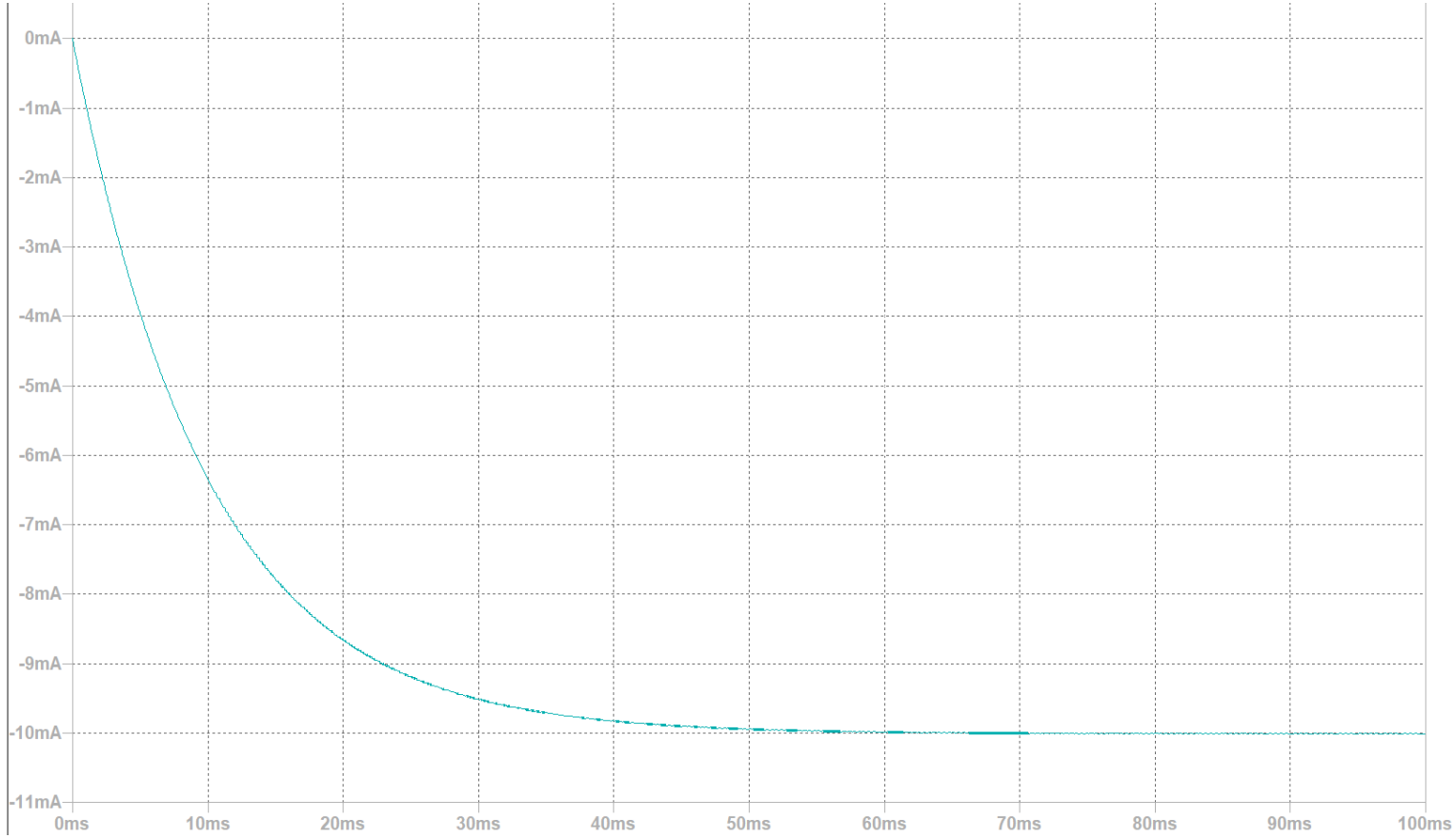
DC Current Needed for Gate Drivers



IPP015N04N

VDS max	40.0 V
RDS (on) (@10V)	max 1.5 mΩ
ID (@25°C) max	120.0 A
Ptot max	250.0 W
Ciss	15000.0 pF
Coss	4000.0 pF
QG (typ @10V)	188.0 nC
VGS(th) min / max	2.0 V / 4.0 V

DC Current Needed for a Gate Driver



MOSFET Ratings and Breakdown

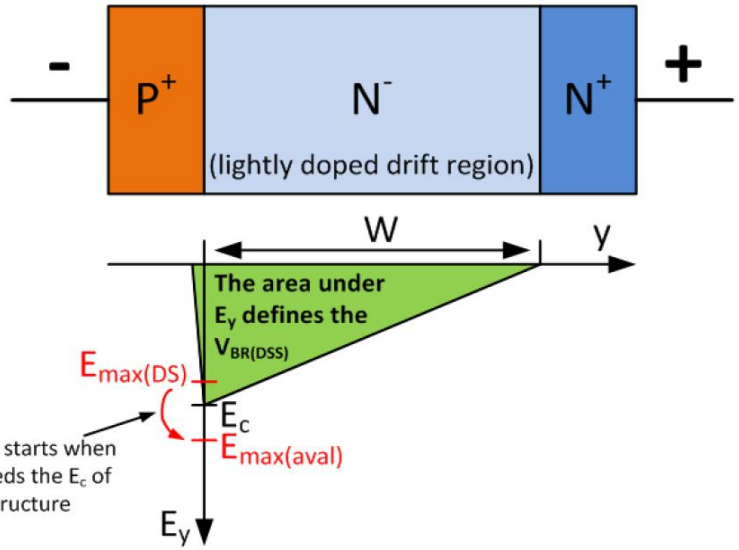
Absolute Maximum Ratings

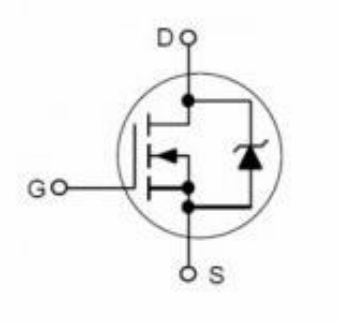
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	60	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	123	
	Continuous Drain Current(1)	24	
I_{DM}	Pulsed Drain Current(2)	256	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	83	
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 39 A, L = 0.1 mH, R_G = 25 Ω	76	mJ

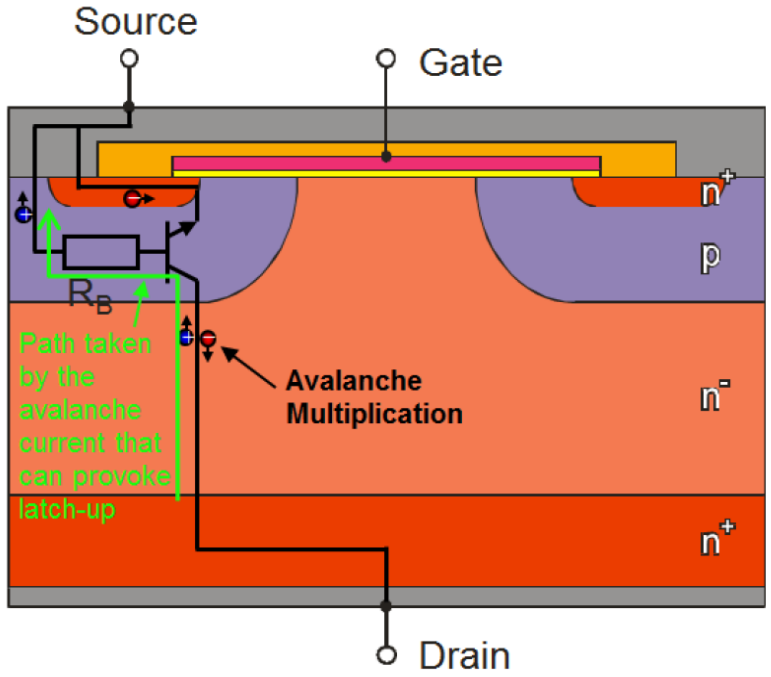
(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-in^2, 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.5°C/W, pulse duration ≤100 μs, duty cycle ≤1%

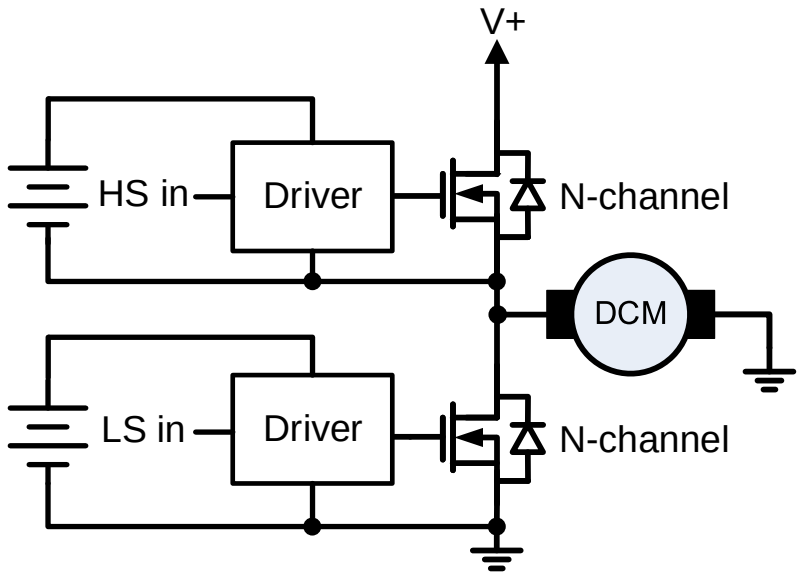
Avalanche


-
P+
N-
(lightly doped drift region)
N+
+
W
y
The area under
Ey defines the
VBR(DSS)
Emax(DS)
Ec
Emax(aval)
Avalanche starts when
Emax exceeds the Ec of
the structure
Ey

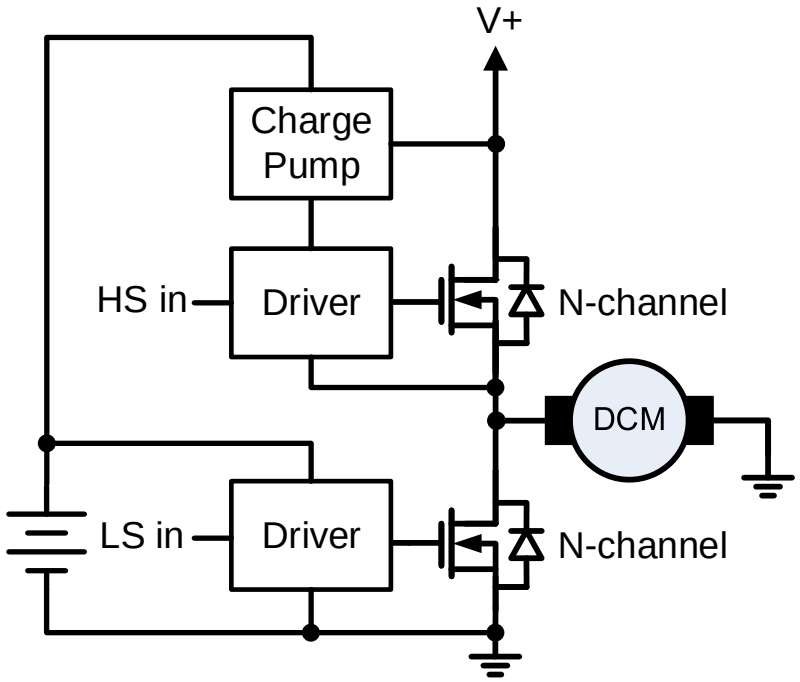

D
G
S


Source
Gate
n+
p
RB
Path taken
by the
avalanche
current that
can provoke
latch-up
Avalanche
Multiplication
n-
n+
Drain

High-Side Gate Drive

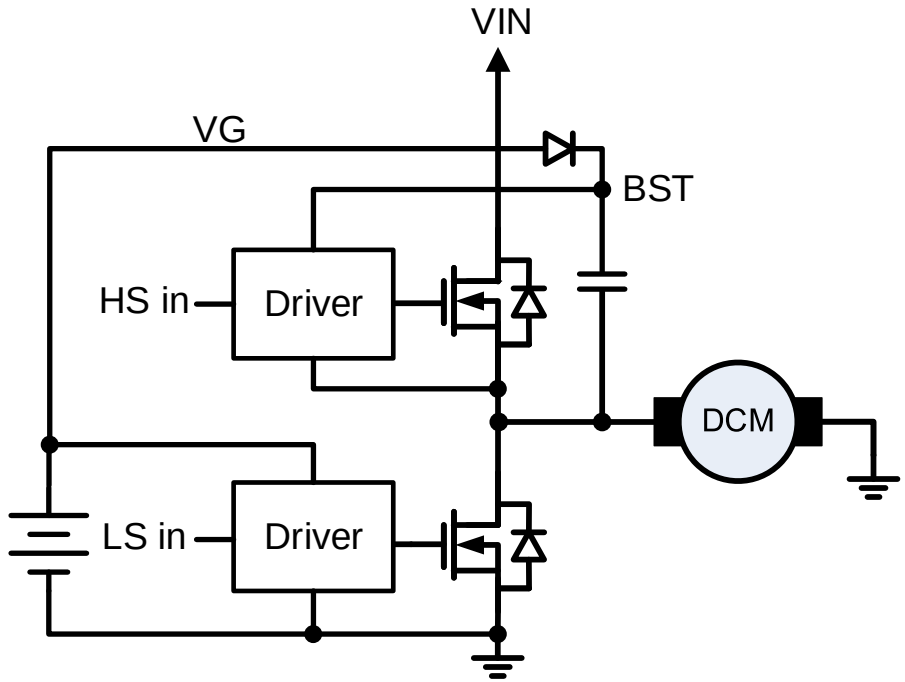


Isolated High-Side Supply

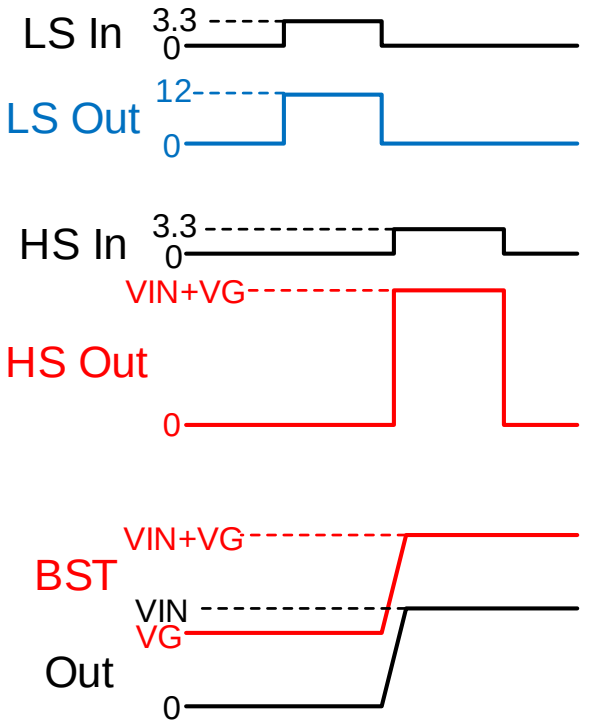


Charge Pump High-Side Supply

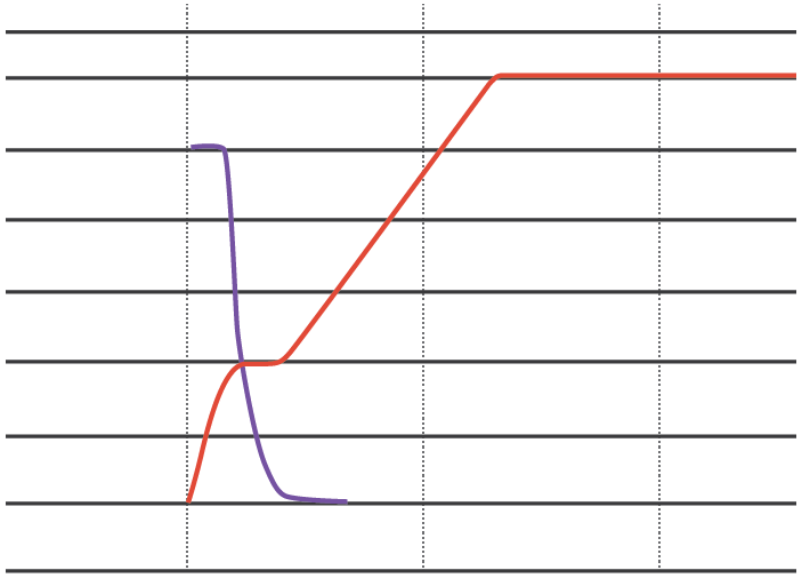
Bootstrap Gate Drive



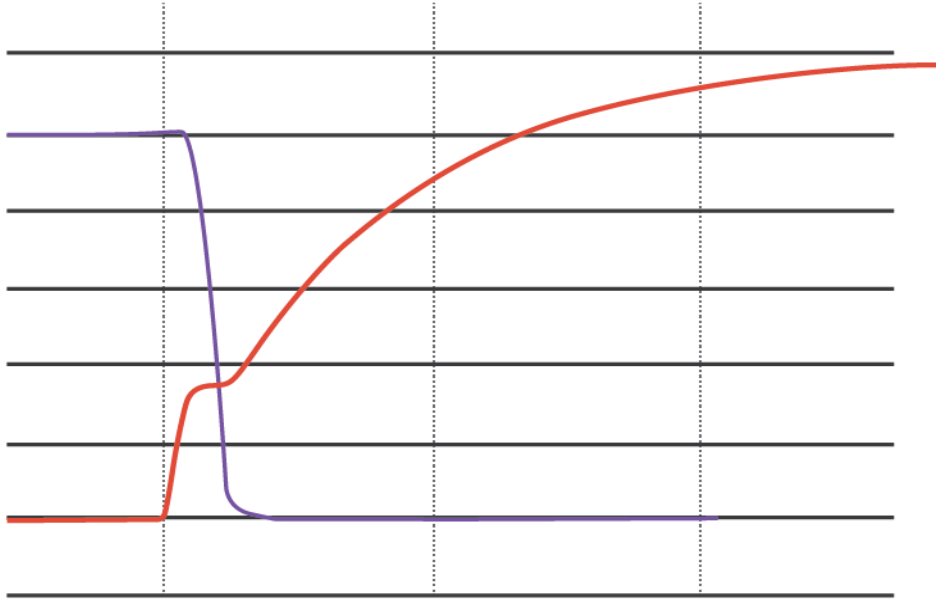
Bootstrap High-Side Supply



Driving the Gate: Constant Current vs. Series Resistance



1 Amp Constant Current Gate Drive
(100nC - Red = gate, purple = drain, 200nS/div)



12V Gate Drive with 12Ω Series Resistance
(100nC - Red = gate, purple = drain, 200nS/div)