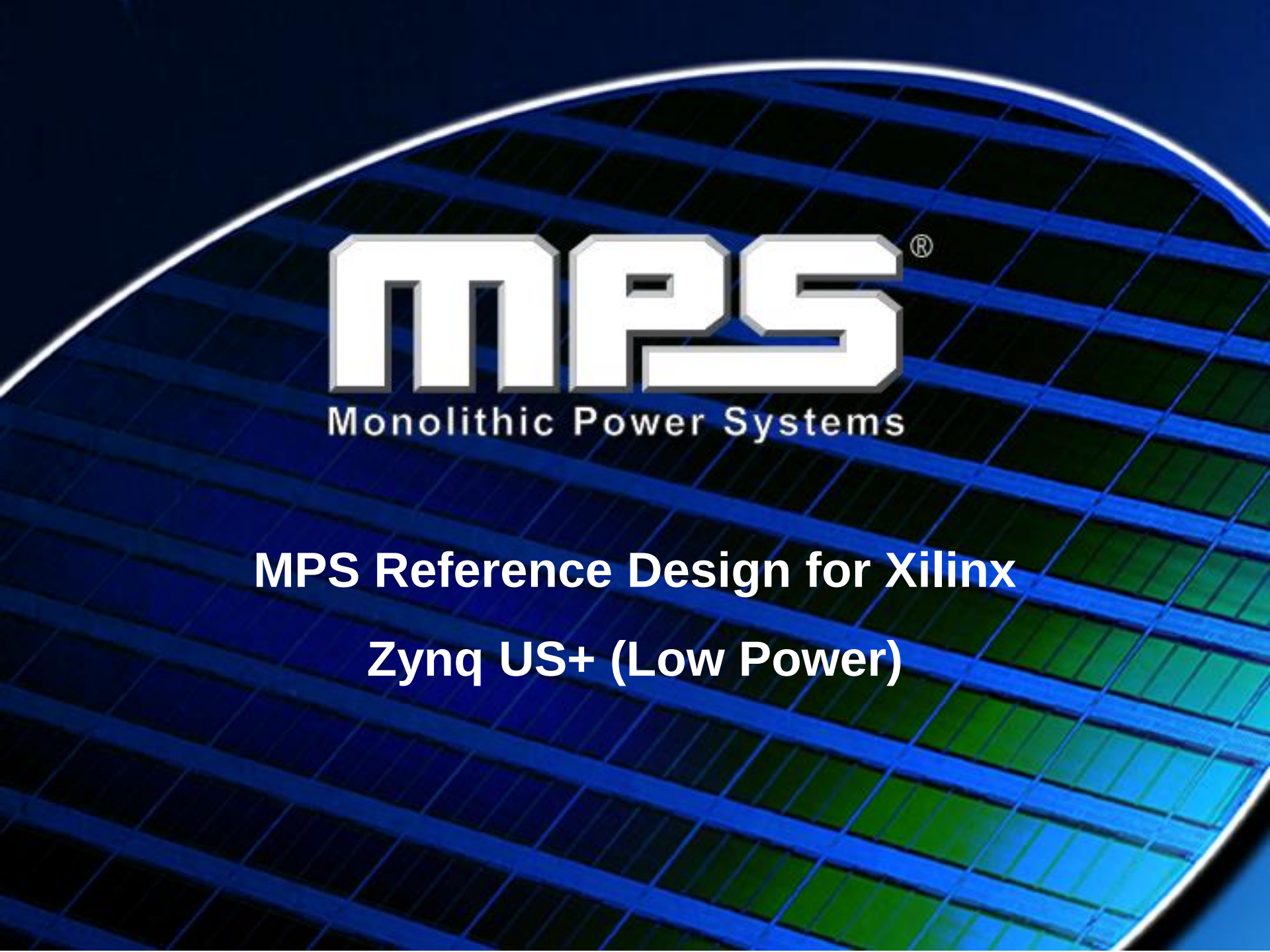
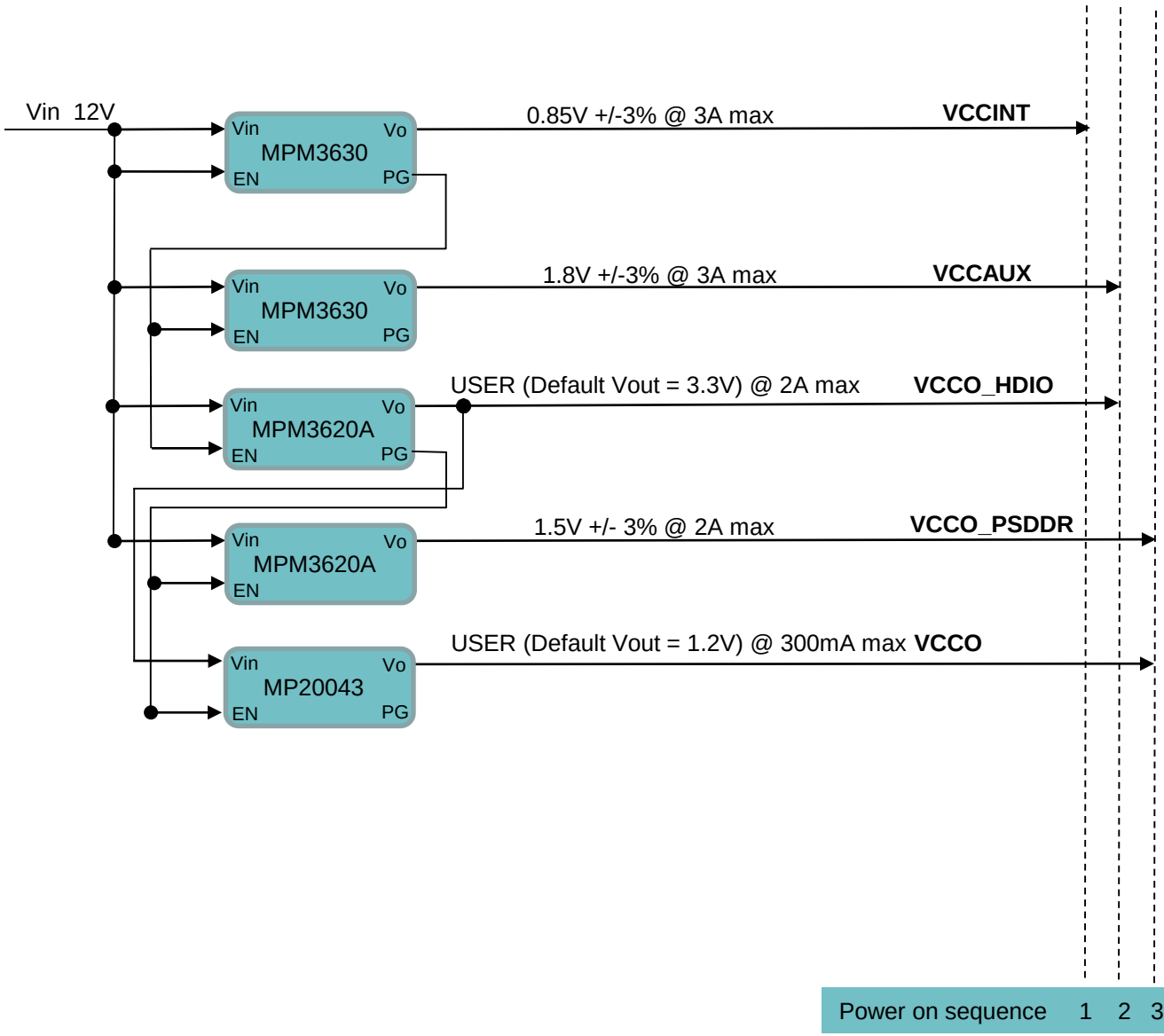


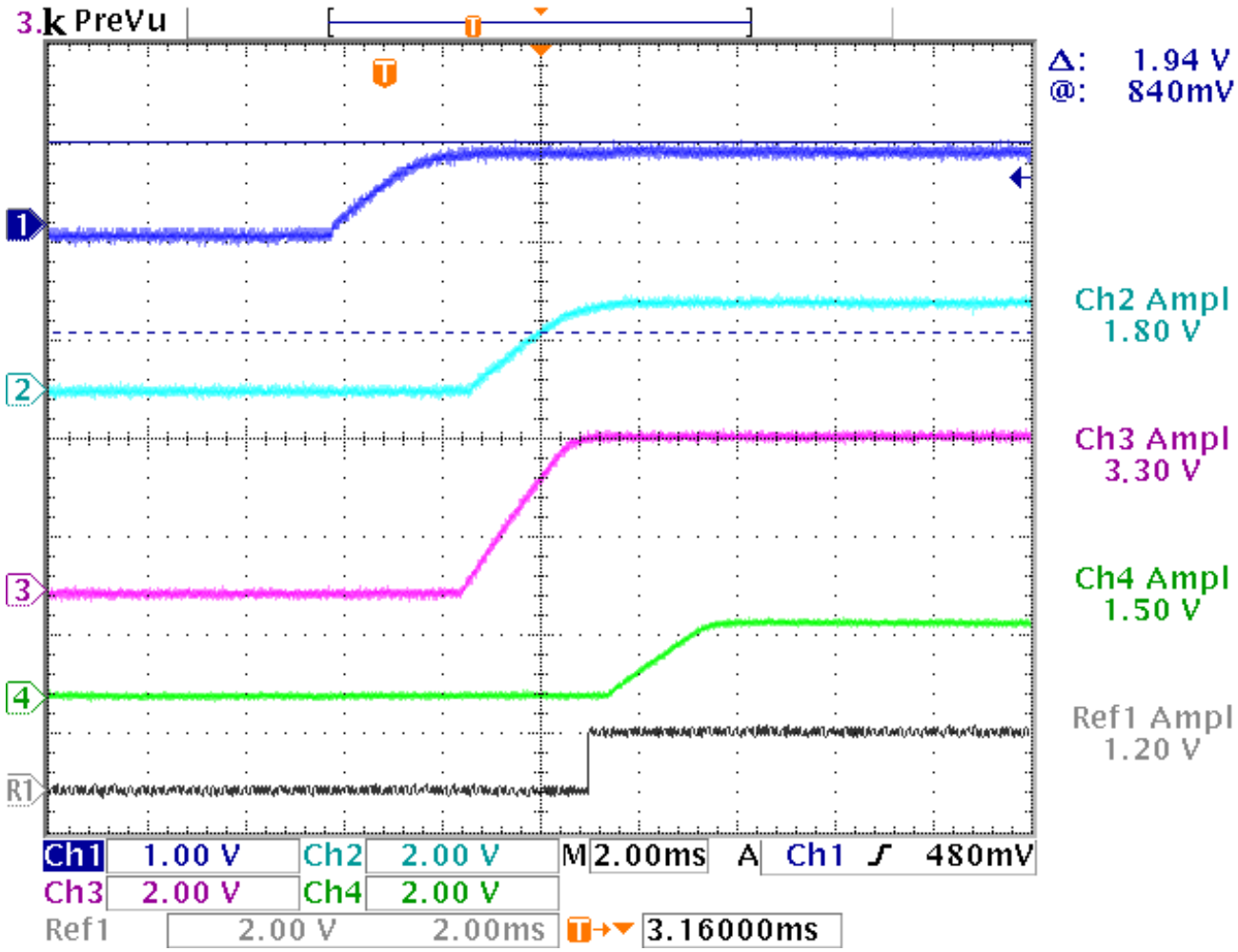
MPS Reference Design for Xilinx Zynq US+ (Low Power)

Block Diagram –
UC1 Always ON (Zynq US+MPSoC)



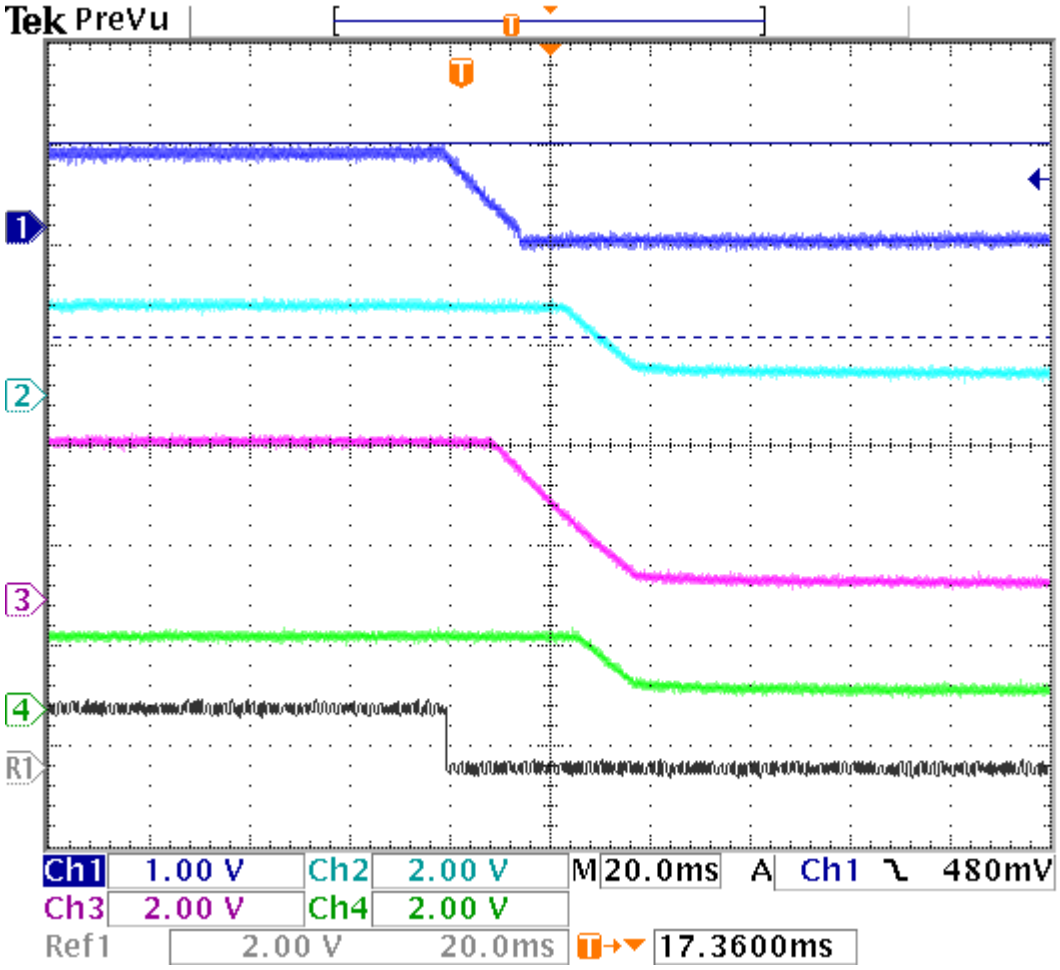
***NOTE: Refer to Design Specs Slide for Options**

Power-up Through Enable Signal



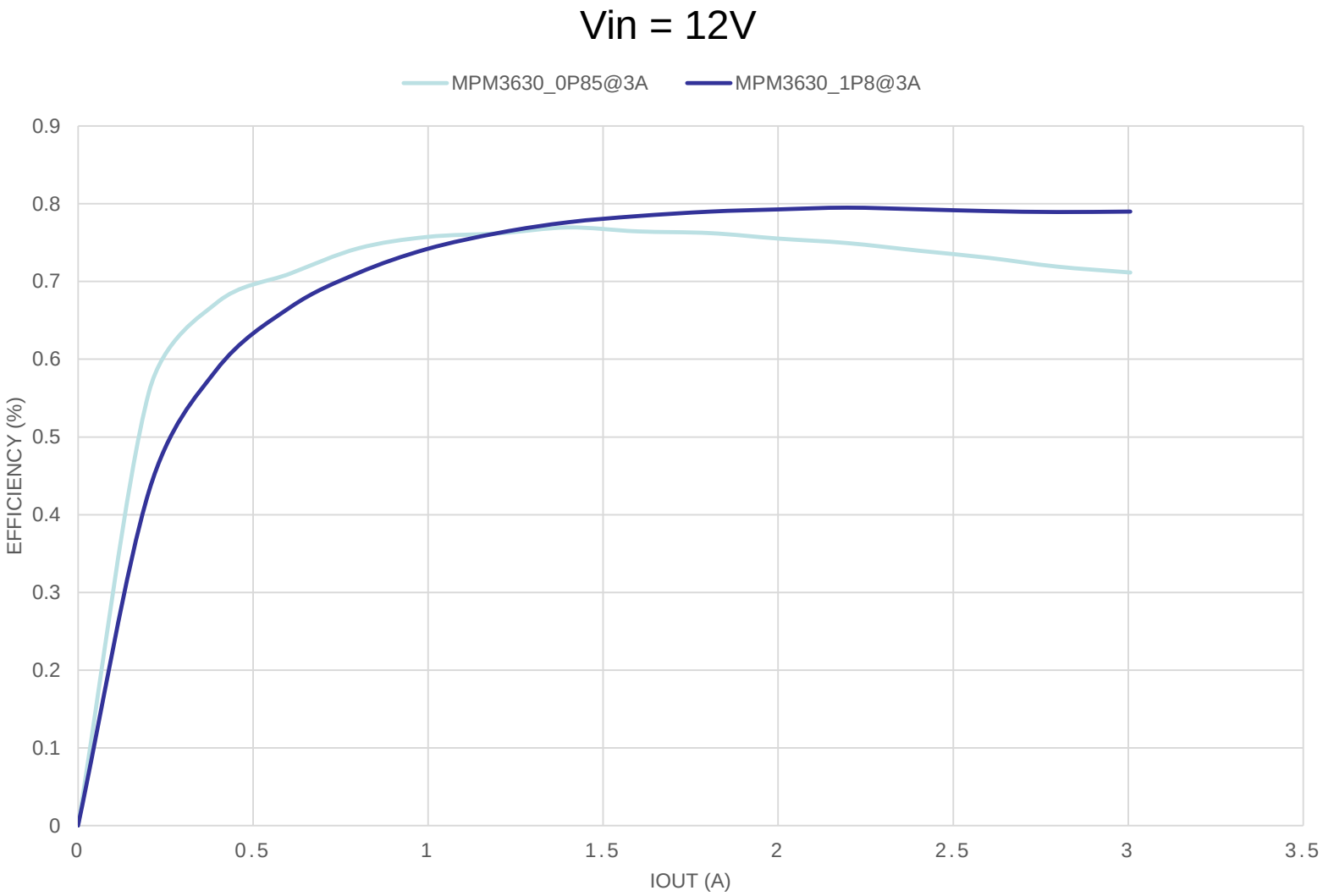
Ch1: MP3630
Ch2: MP3630
Ch3: MP3620A
Ch4: MP3620A
Ref1: MP20043

Power-Down Through Enable Signal

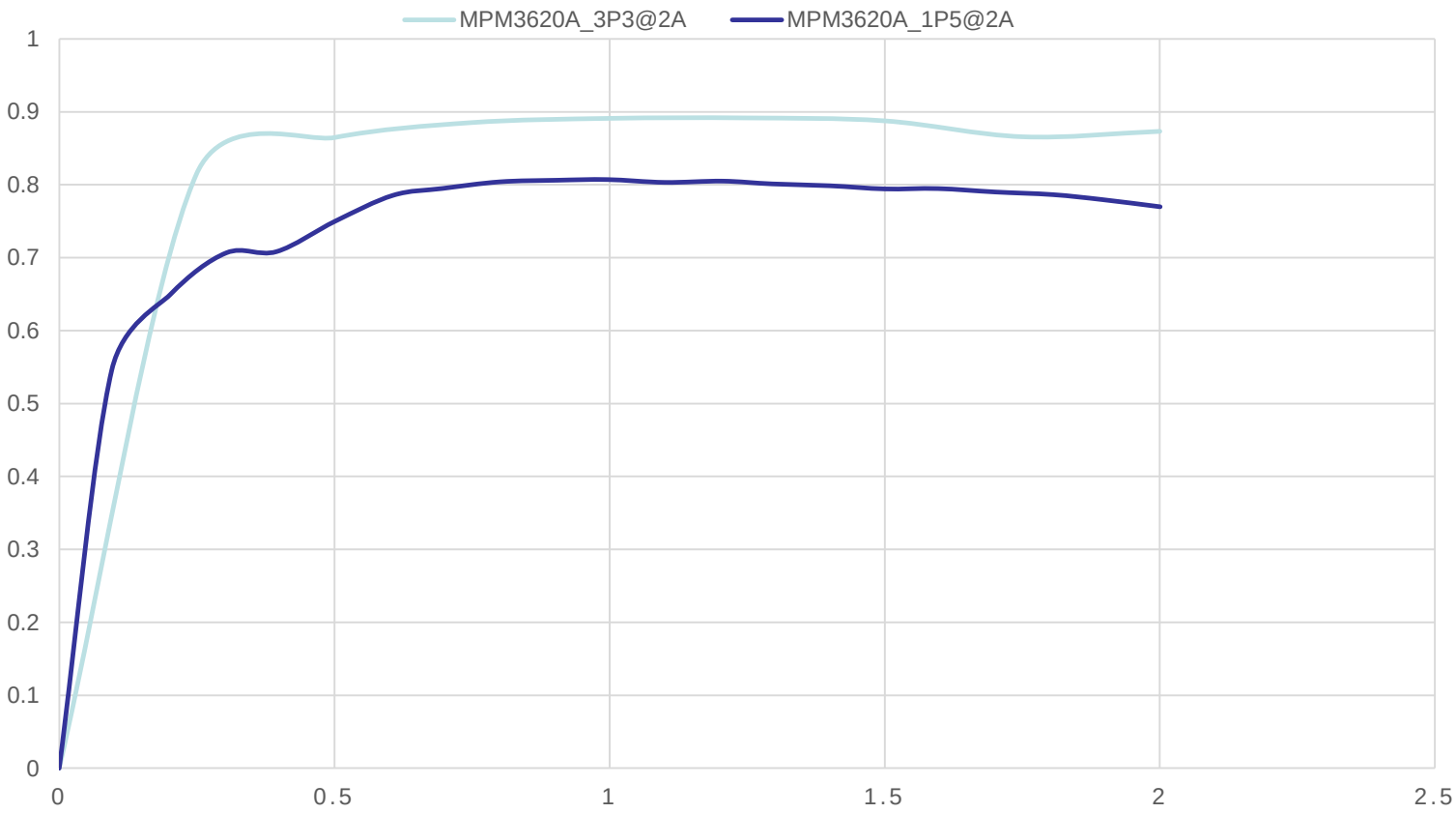


Ch1: MP3630
Ch2: MP3630
Ch3: MP3620A
Ch4: MP3620A
Ref1: MP20043

MPM3630 Efficiency

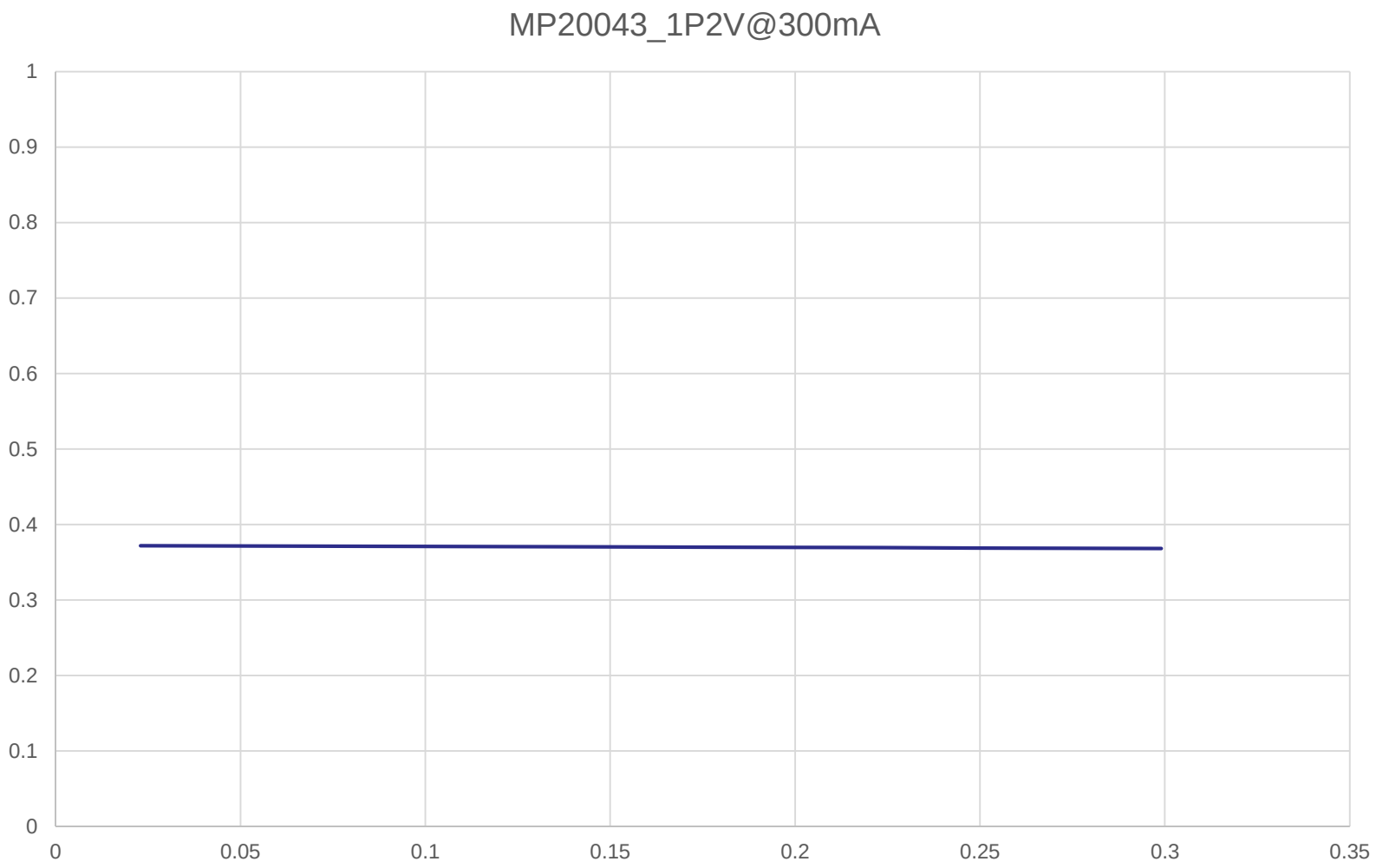


MPM3620A Efficiency



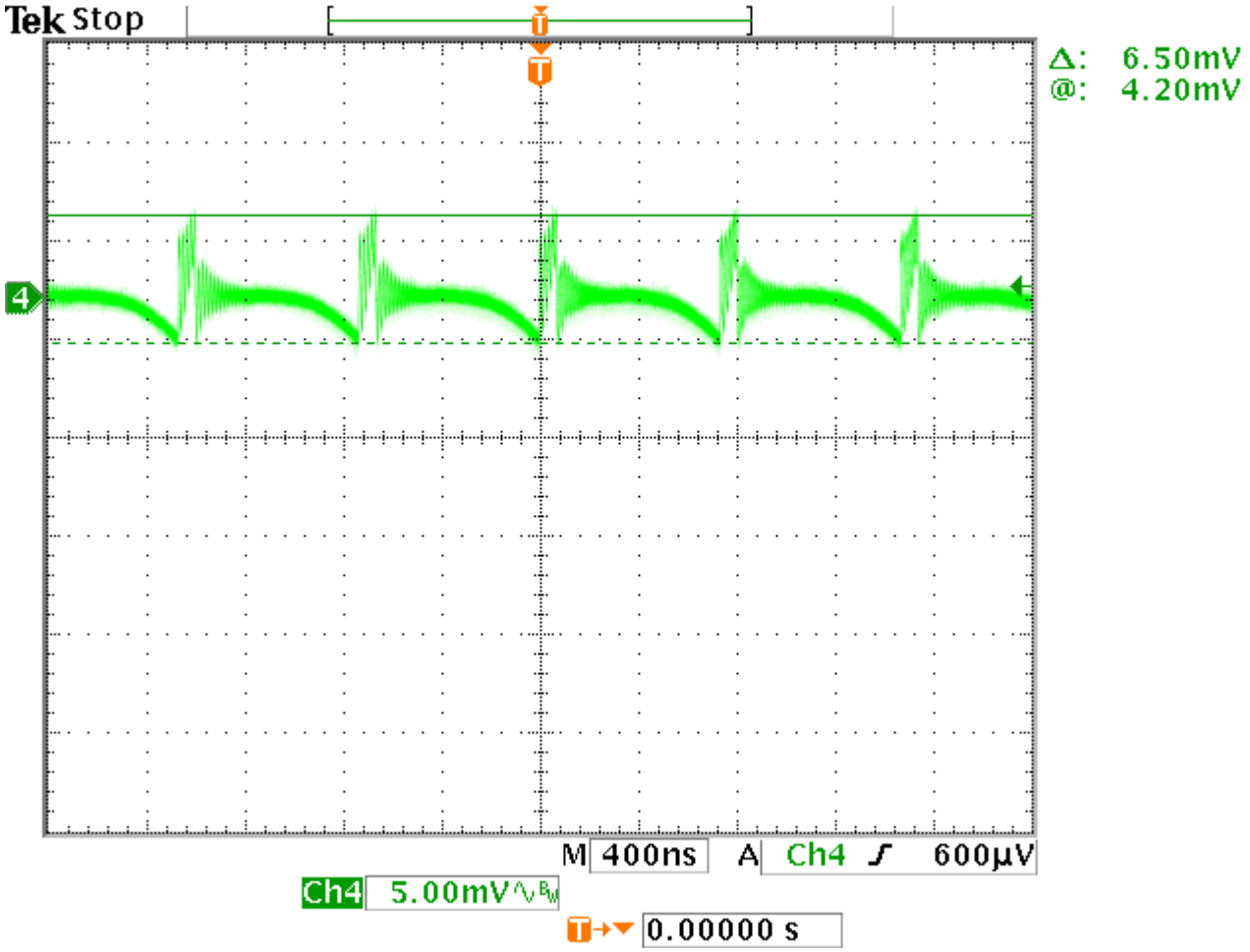
MP20043 Efficiency

Vin = 3.3V



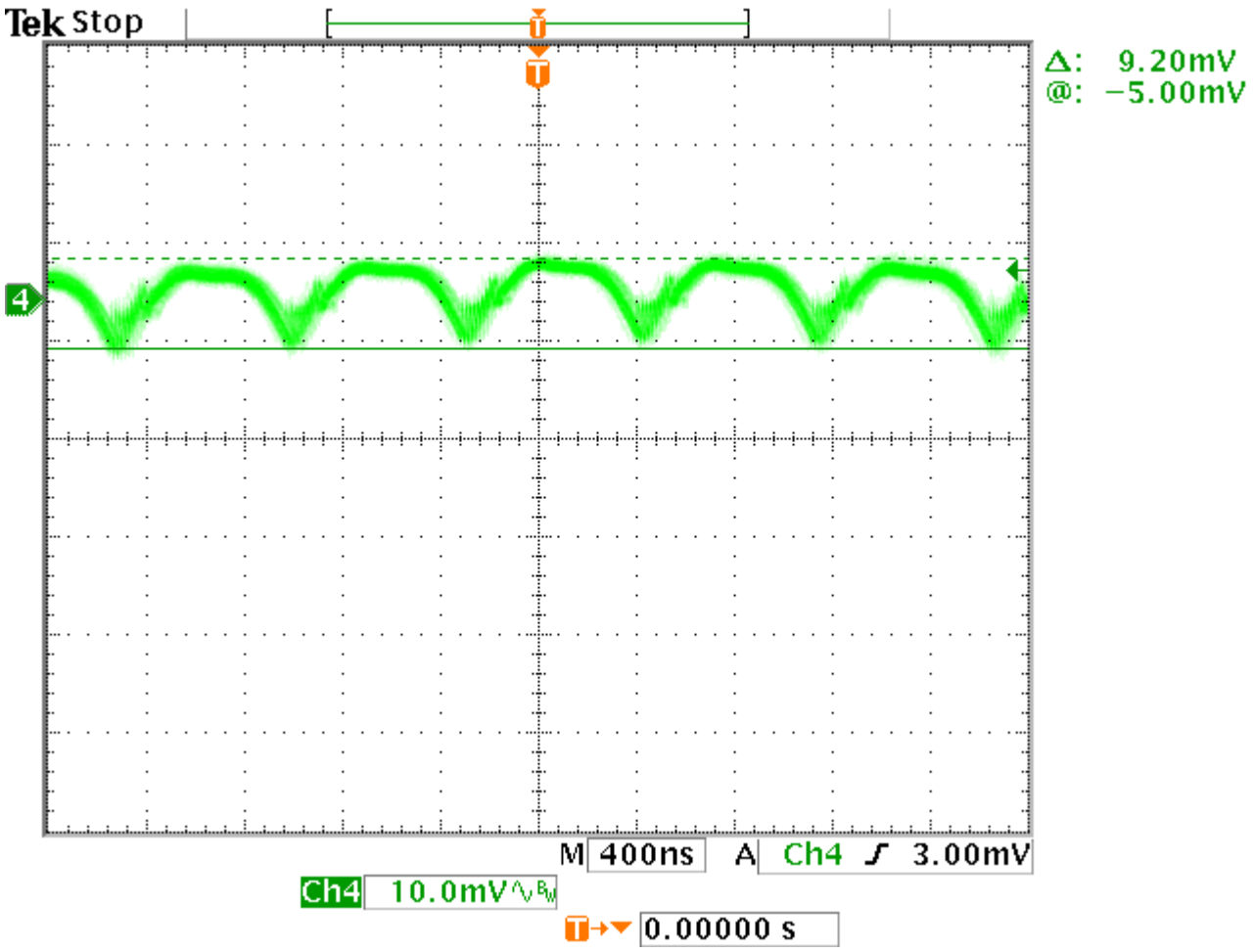
MPM3630 for VCCINT 0.85V Output Ripple

Vin = 12V, Vout = 0.85V, Iout = 3A



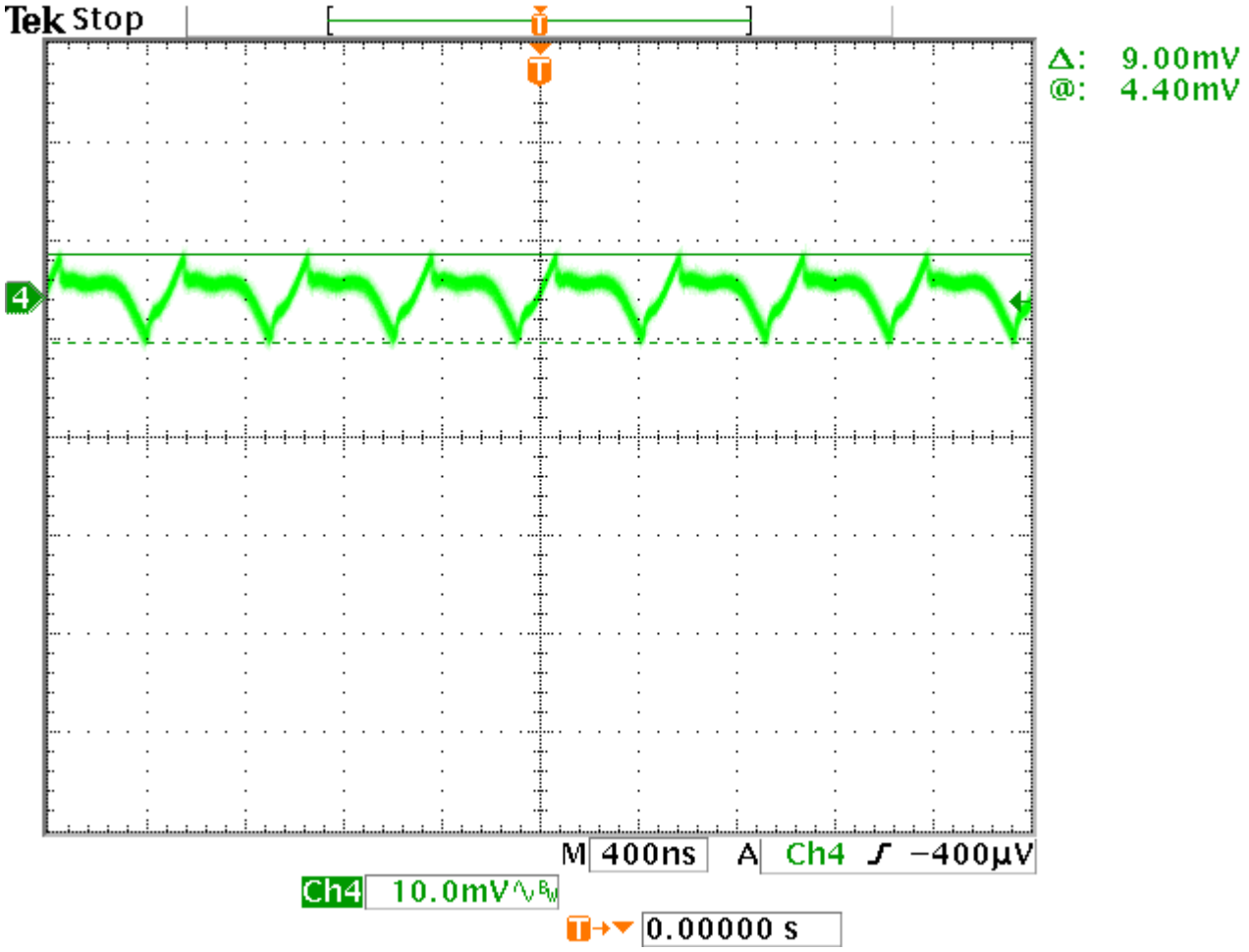
MPM3630 for VCCAUX 1.8V Output Ripple

Vin = 12V, Vout = 1.8V, Iout = 3A



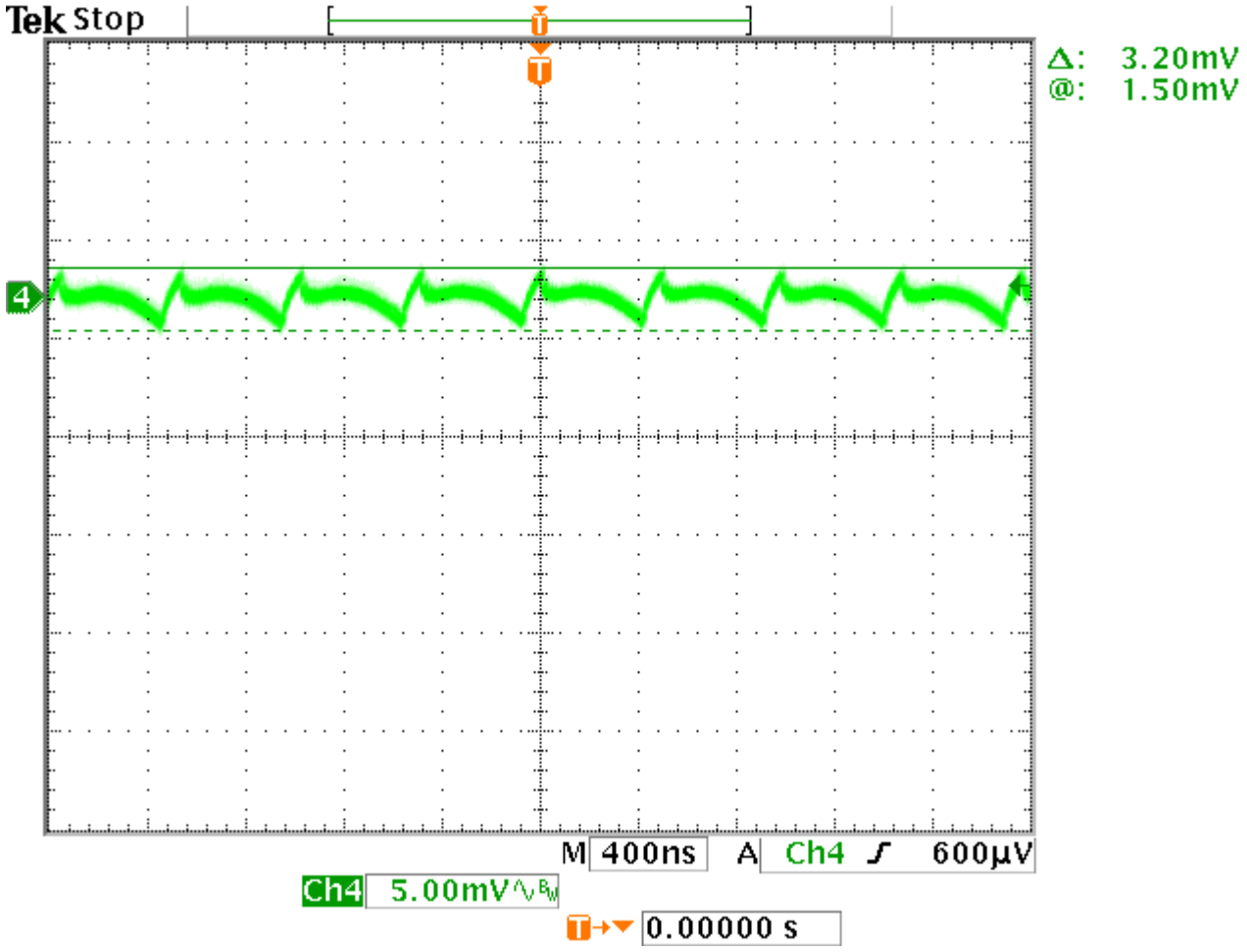
MPM3620A for VCCO_IO 3.3V Output Ripple

Vin = 12V, Vout = 3.3V, Iout = 2A



MPM3620A for VCC_DDR 1.5V Output Ripple

Vin = 12V, Vout = 1.5V, Iout = 2A



MP20043 for 1.2V Output Ripple

Vin = 12V, Vout = 1.2V, Iout = 300mA