Automotive EMI Demystified: Part 2
Pursuing an Ideal Power Supply Layout

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2010 – Present

- MPS Senior FAE since 2010, working with industrial and automotive customers on power supply design.
- Particular specialty focus on layout and EMC topics, including frequently visiting automotive EMC lab for EVB testing / optimization and improving MPS automotive/industrial EVB’s EMC performance

1999 – 2010 FAE at Linear Technology

- Support industrial and automotive customers; Support LTC's EMC clean EV-Board DC1212 (LT3480/LT3685)

1995 – 1998

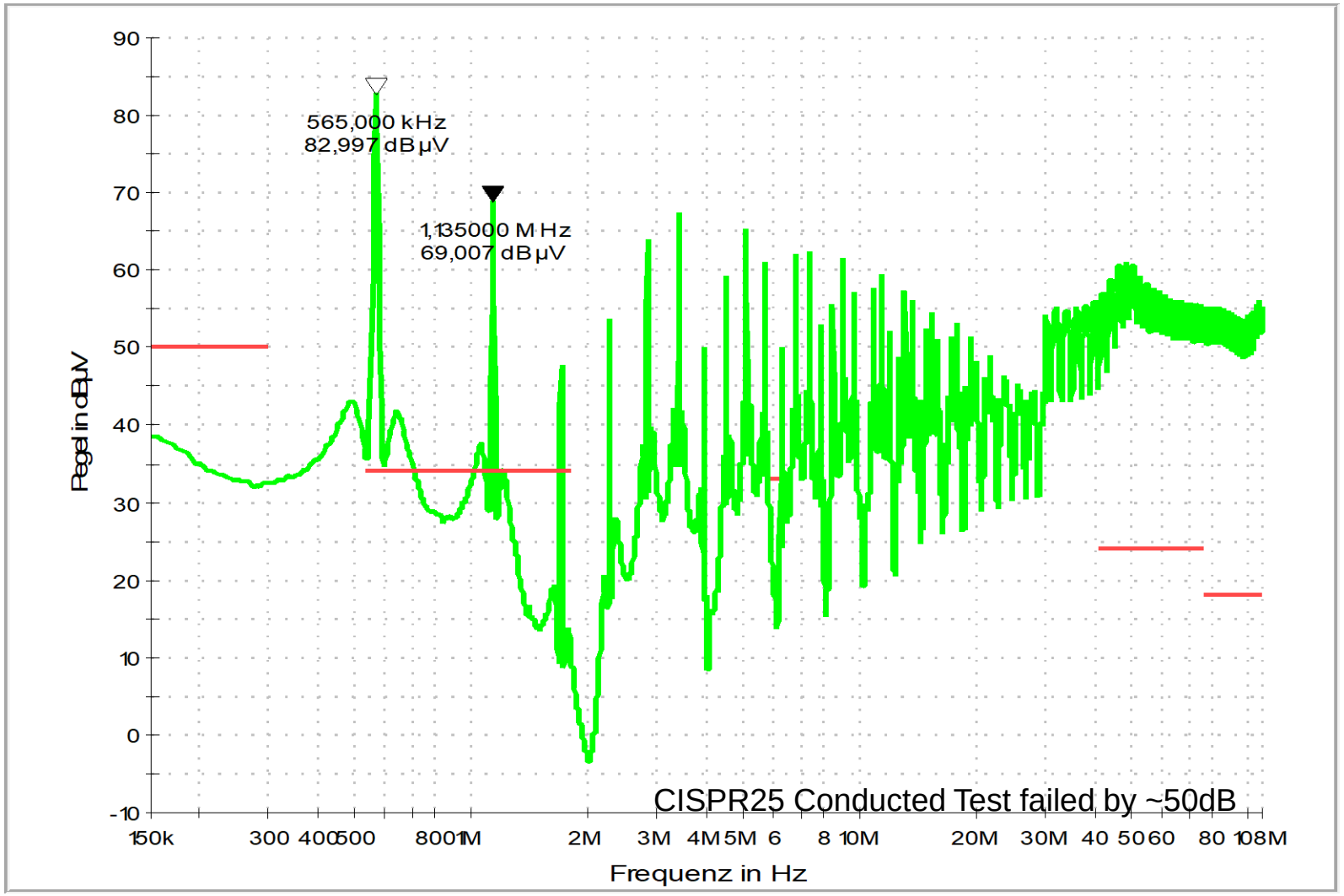
- Hardware design engineer at Nokia Mobile Phones; Worked on early automotive Telematic solution with e-call and emergency battery; EMC support

Agenda

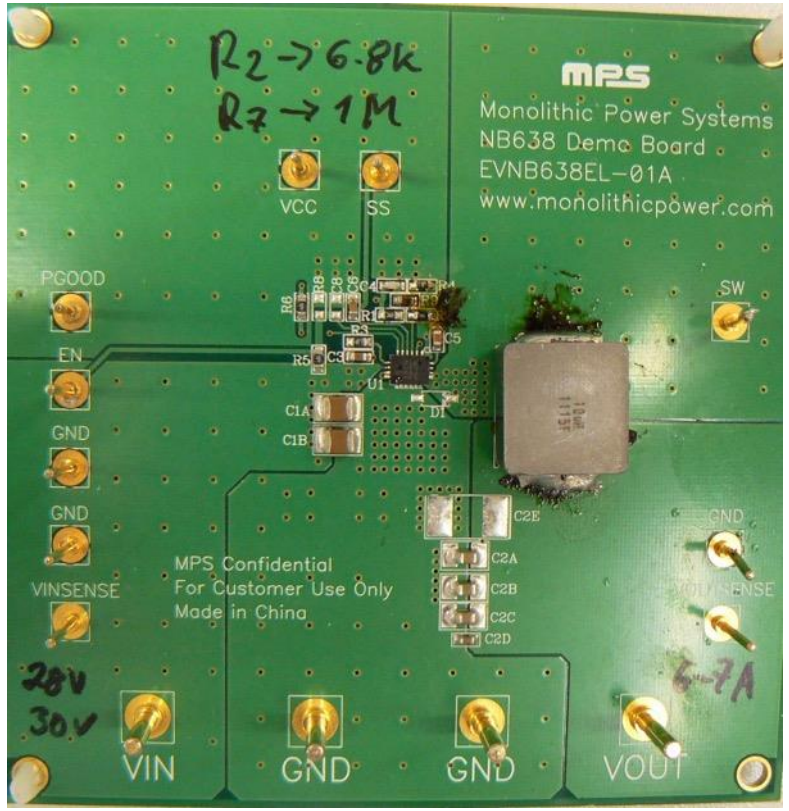
- The Motivation
- Initial PCB Real Estate Planning
- How Best to Utilize Each Layer in the PCB
- Copper Under the Inductor or Not: the Classic Debate
- EMI-Optimized Schematic and Layout Case Study
- Frequently Asked Questions About Layout for EMI
- Open Q&A

Our Motivation: Avoiding This Result

EMC Test Result of a Bad* PCB Without Filter

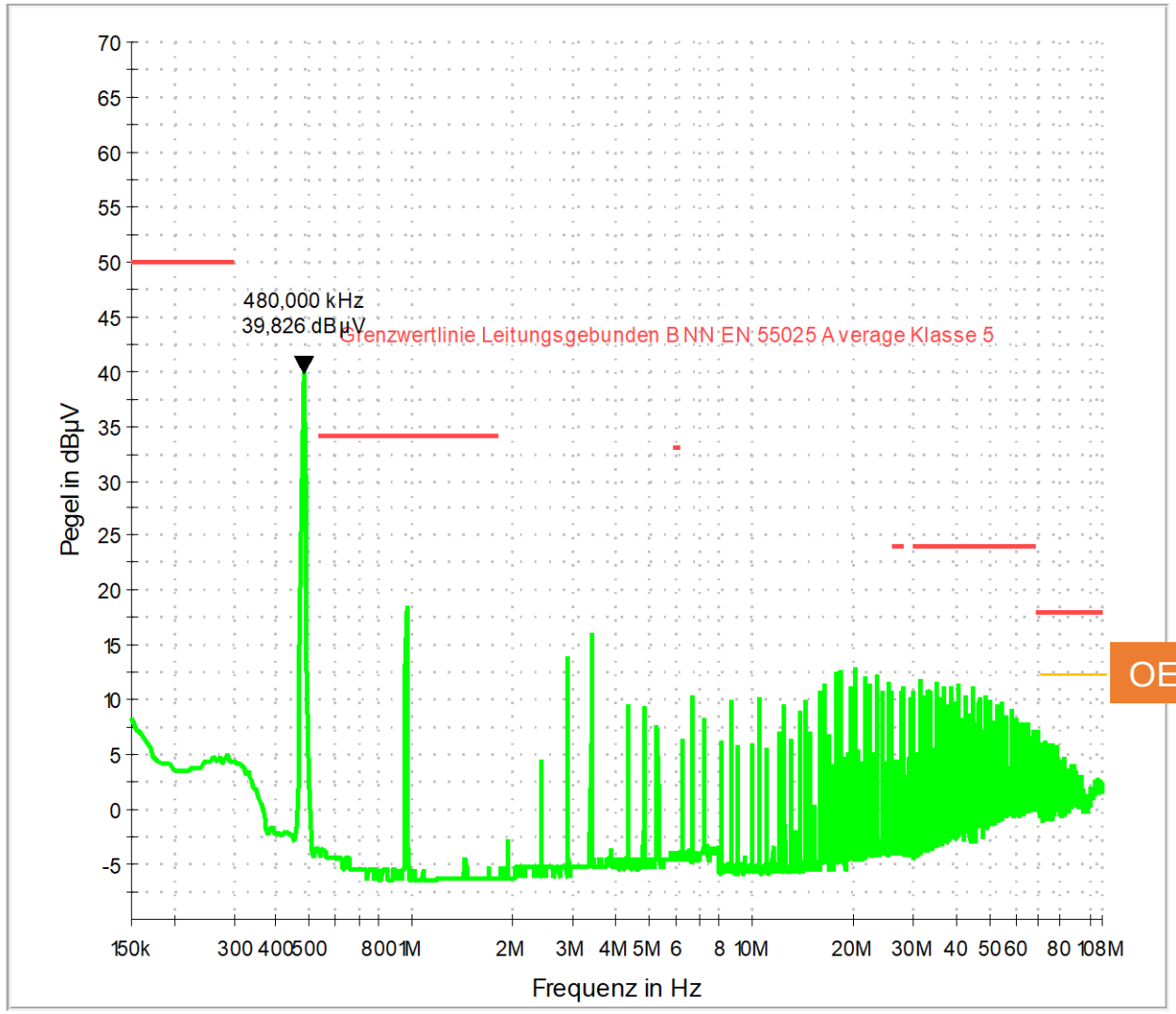


30V / 7A Sync. Buck Board Optimized for Thermal Performance but not EMC

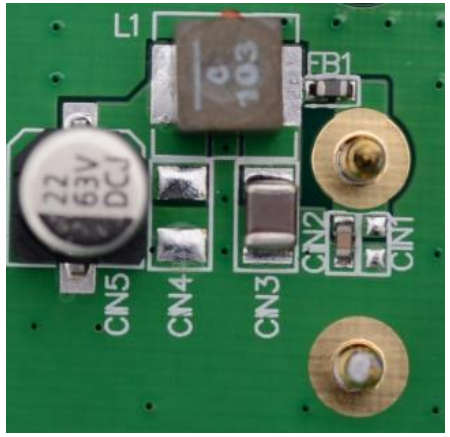


- Large SW area
- No solid GND plane
- Only two Layer
- NO EMC Filter

A Much Better Board with EMC Filter



OEM Limit

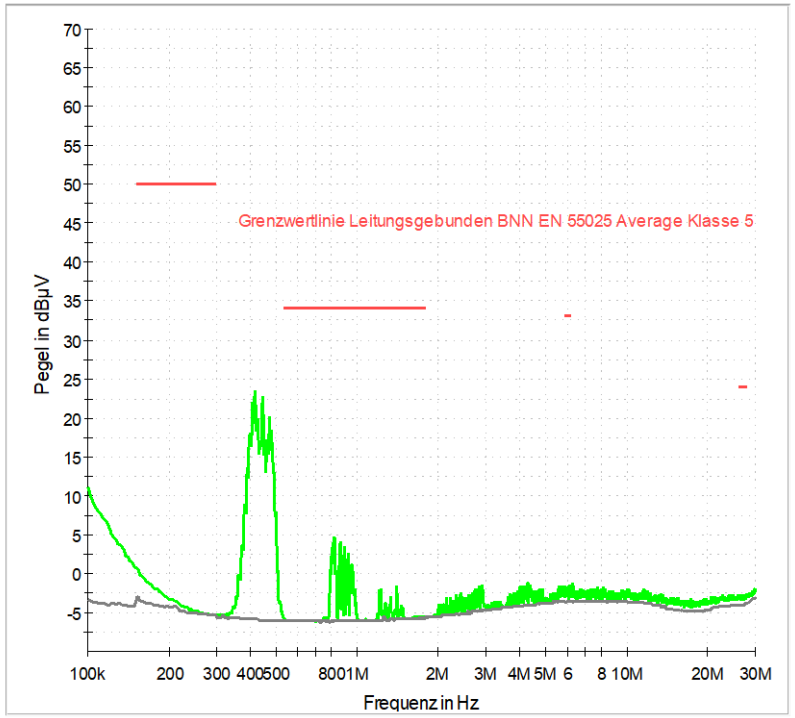


Input EMC Filter on Bottom side of PCB

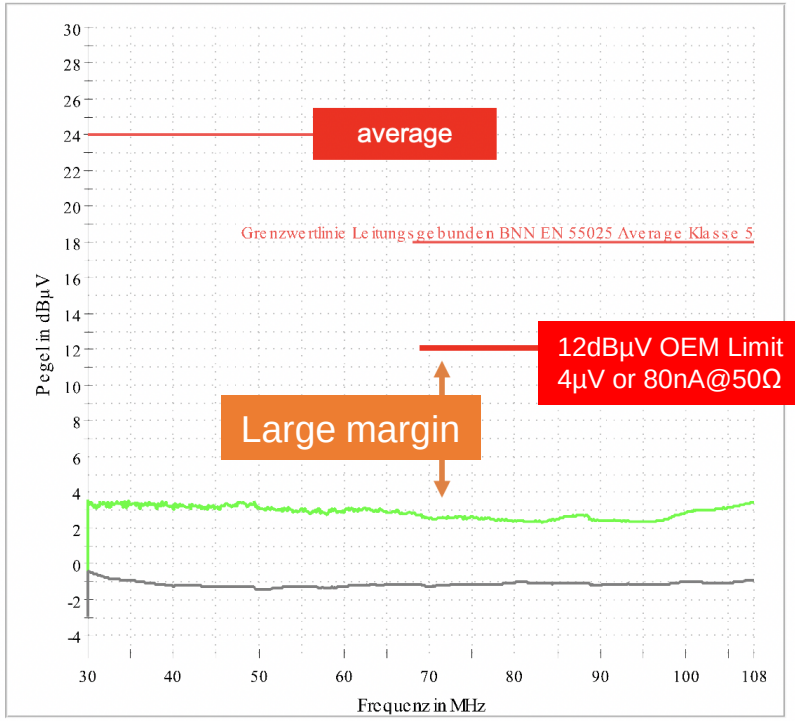
Single stage filter with 10µH 5x5x5 and 10µF 1210

A Much, *Much* Better Board

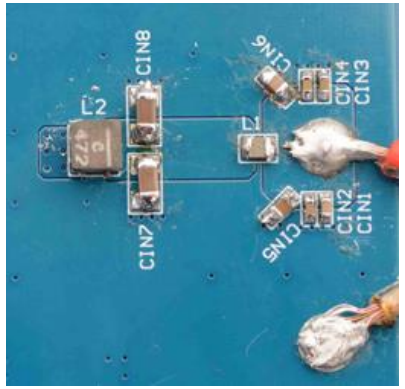
100kHz to 30MHz 9kHz RBW



30MHz to 108MHz 120kHz RBW



EVQ4430-00A 480kHz Spread Spectrum

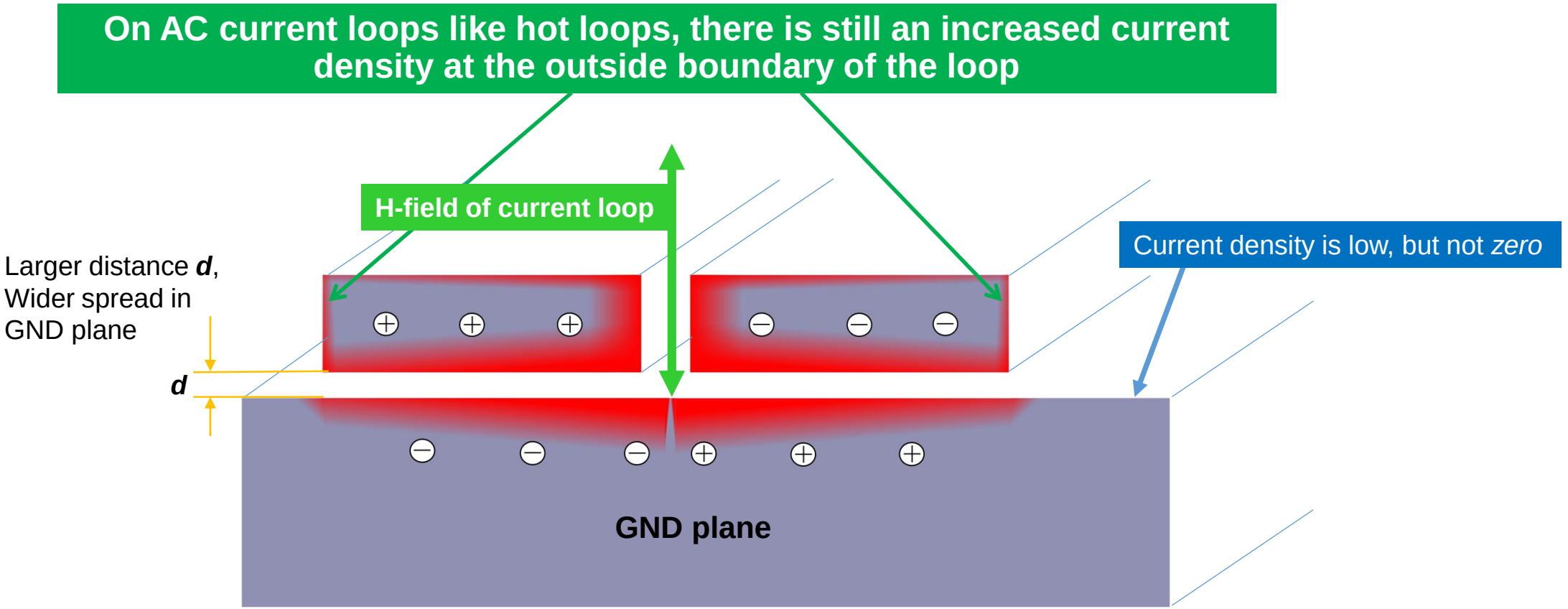


Filter on bottom side

Two stage filter with small components

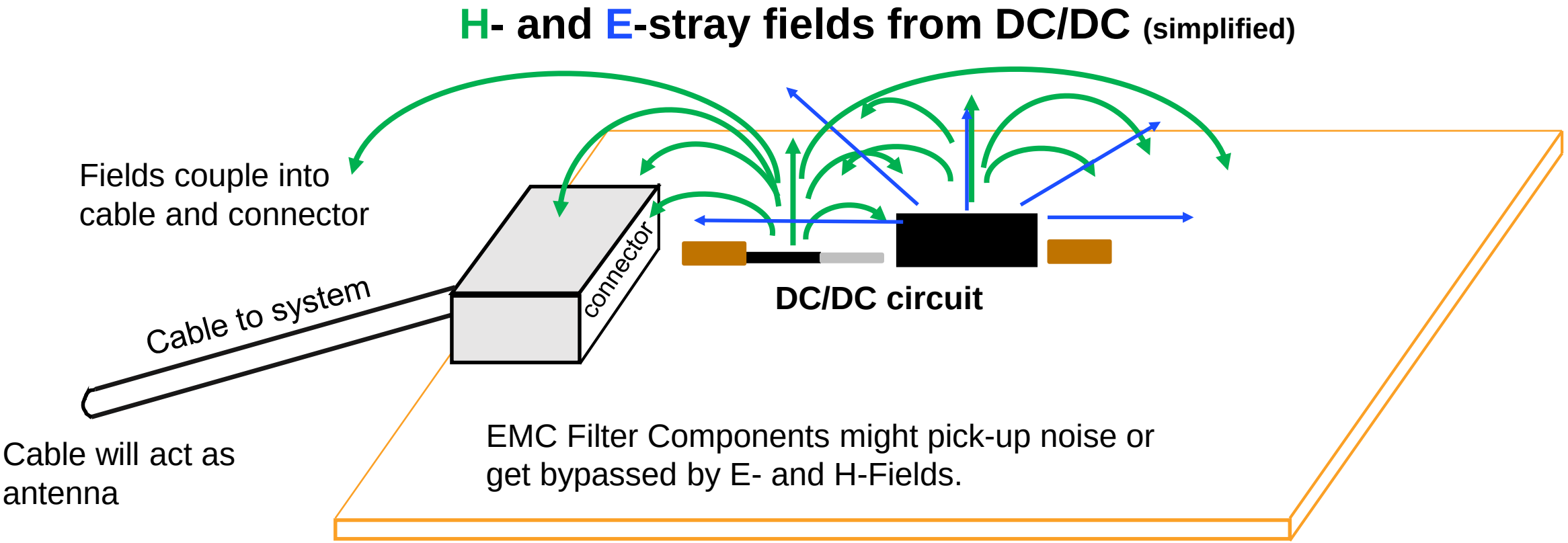
Learn how to get to this level

Reminder From Last Webinar: Magnetic Antennas



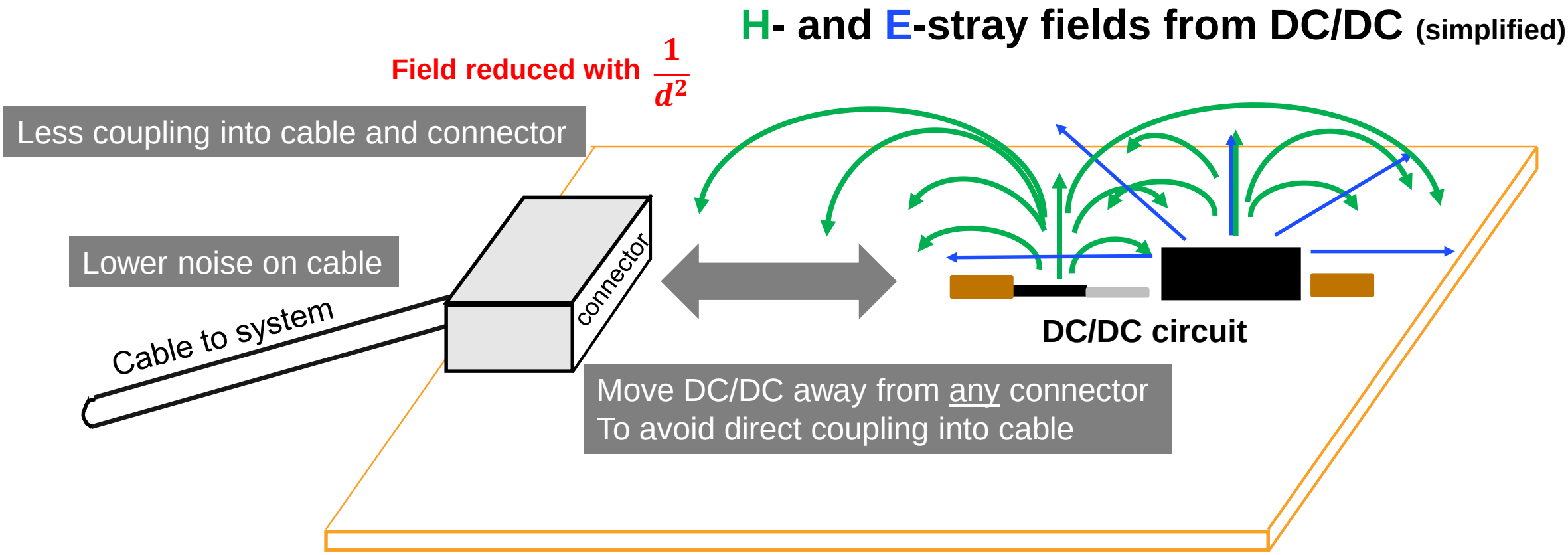
Good EMC Design Starts with Initial PCB Real Estate Plan

Initial PCB Real Estate Plan



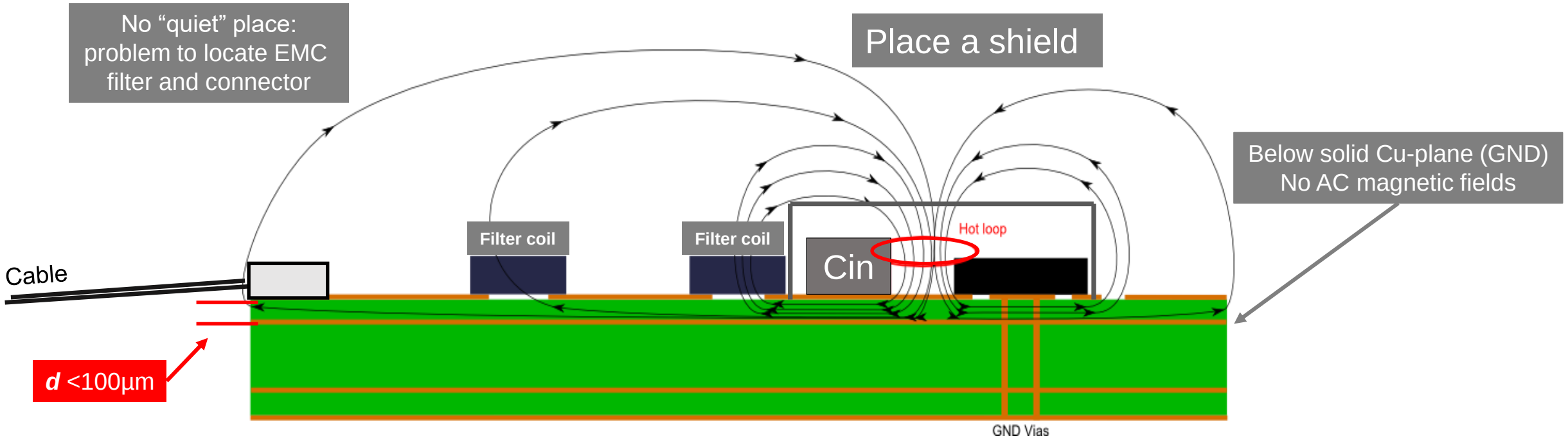
EMC Problem

Initial PCB Real Estate Plan: Where to Place the DC/DC?



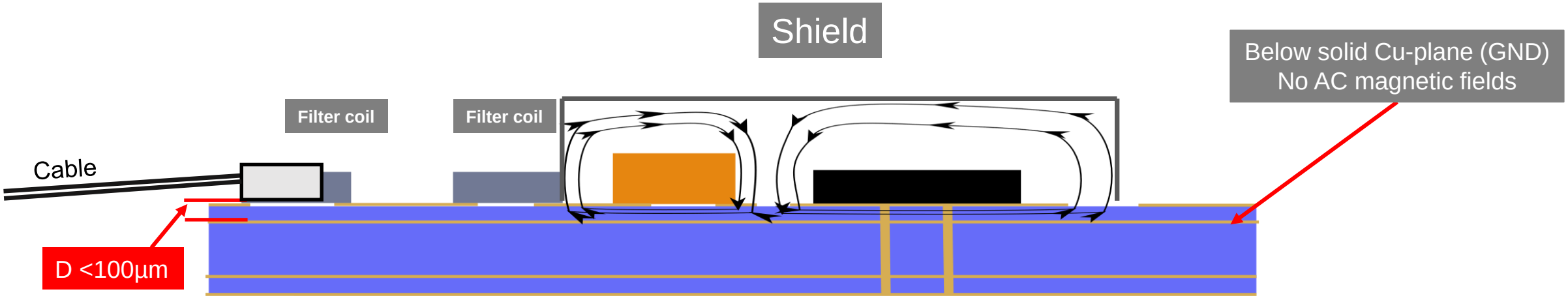
- EMC filter components must be placed close to connector
- In case of two side assembly, EMC filter on opposite side with respect to DC/DC Converter gives best results

Coupling From SW-Node Into Other Circuits: Single Side Assembly

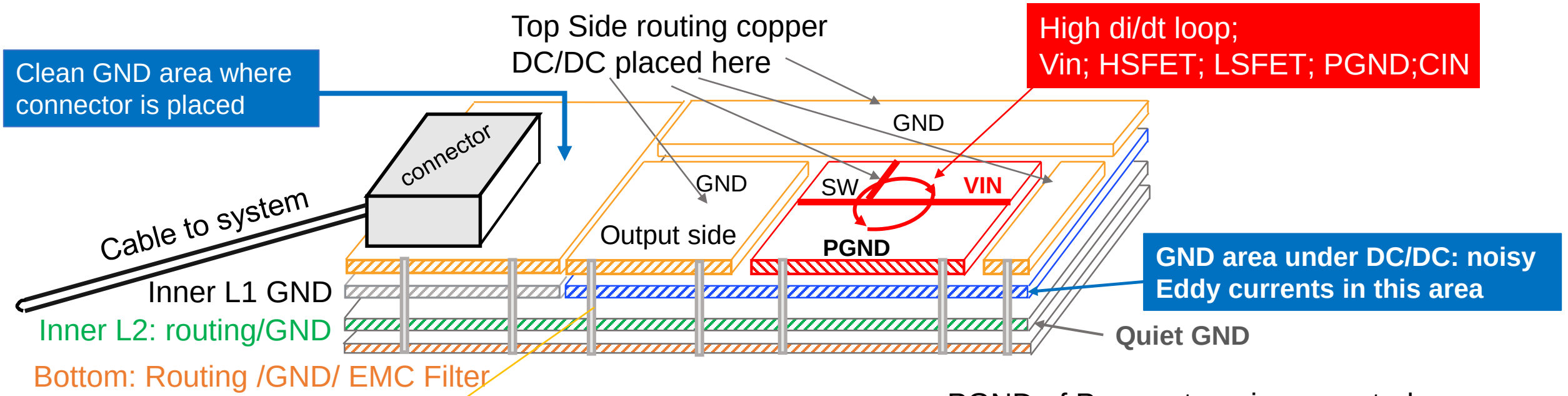


Single Side Assembly : Placing a Shield

A Heat-Sink can
also act as a Shield



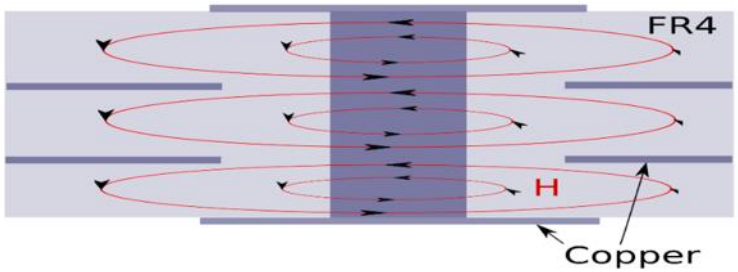
How to Utilize a Multi-Layer PCB for Best EMC Performance?



PGND of Power stage is separated on component side from other GND area.
Vin and PGND of high di/dt
Loop are connected through vias.

Vias act as filter to block noise between noisy parts and clean GND at connector

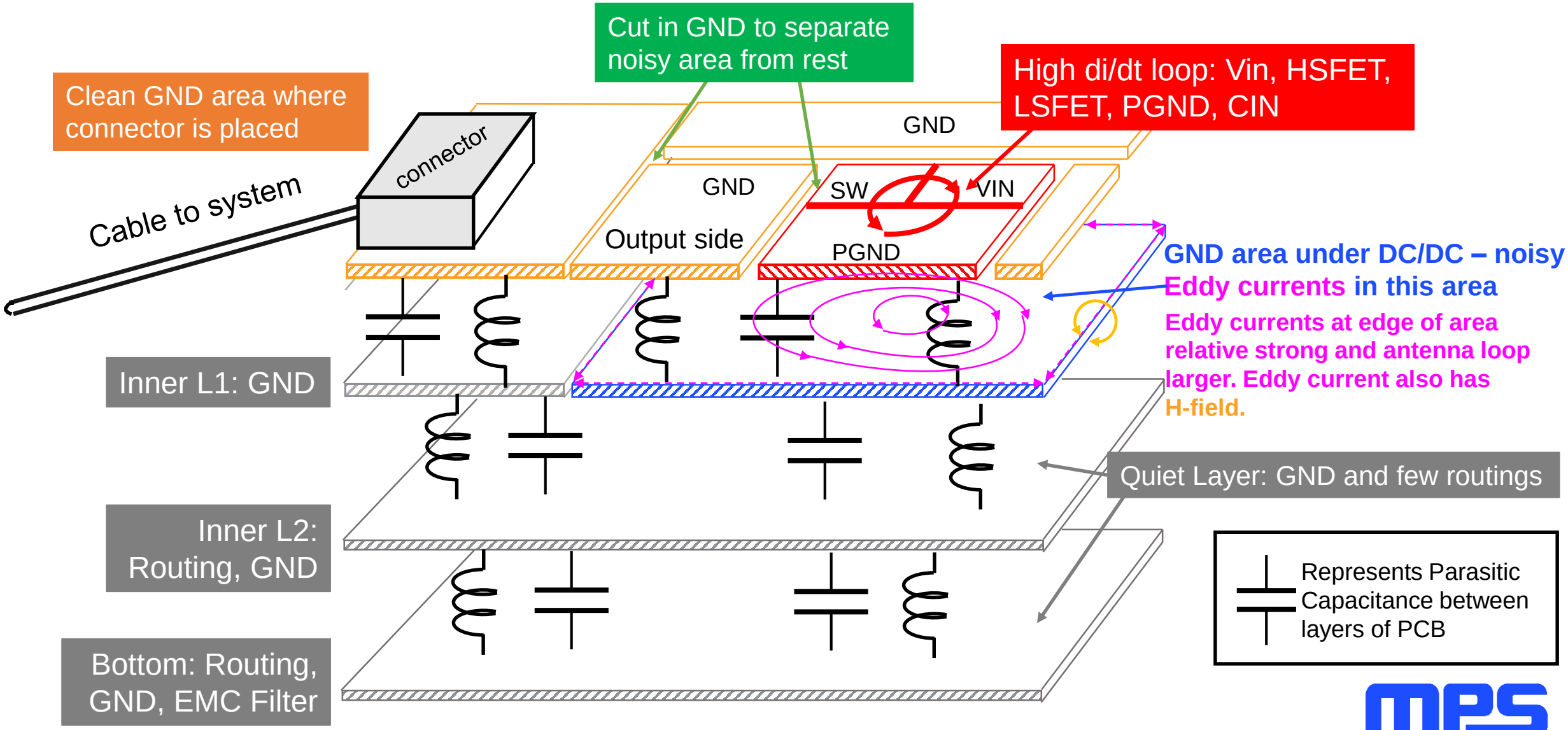
Via in 4 Layer PCB



Complete through via inductance ~1nH

Look at the PCB In 3-Dimensions: Simplified Equivalent Representation

Use parasitic elements of the layout to your advantage. A via is a small inductor 



Place Copper Under Inductor?

Opinion A:
“No! AC magnetic field from coil will create Eddy currents in copper under inductor. This will reduce effective inductance and create additional losses!”

Opinion B:
“Yes! Directly on top side of PCB to avoid magnetic fields disturbing other layers of the PCB!”

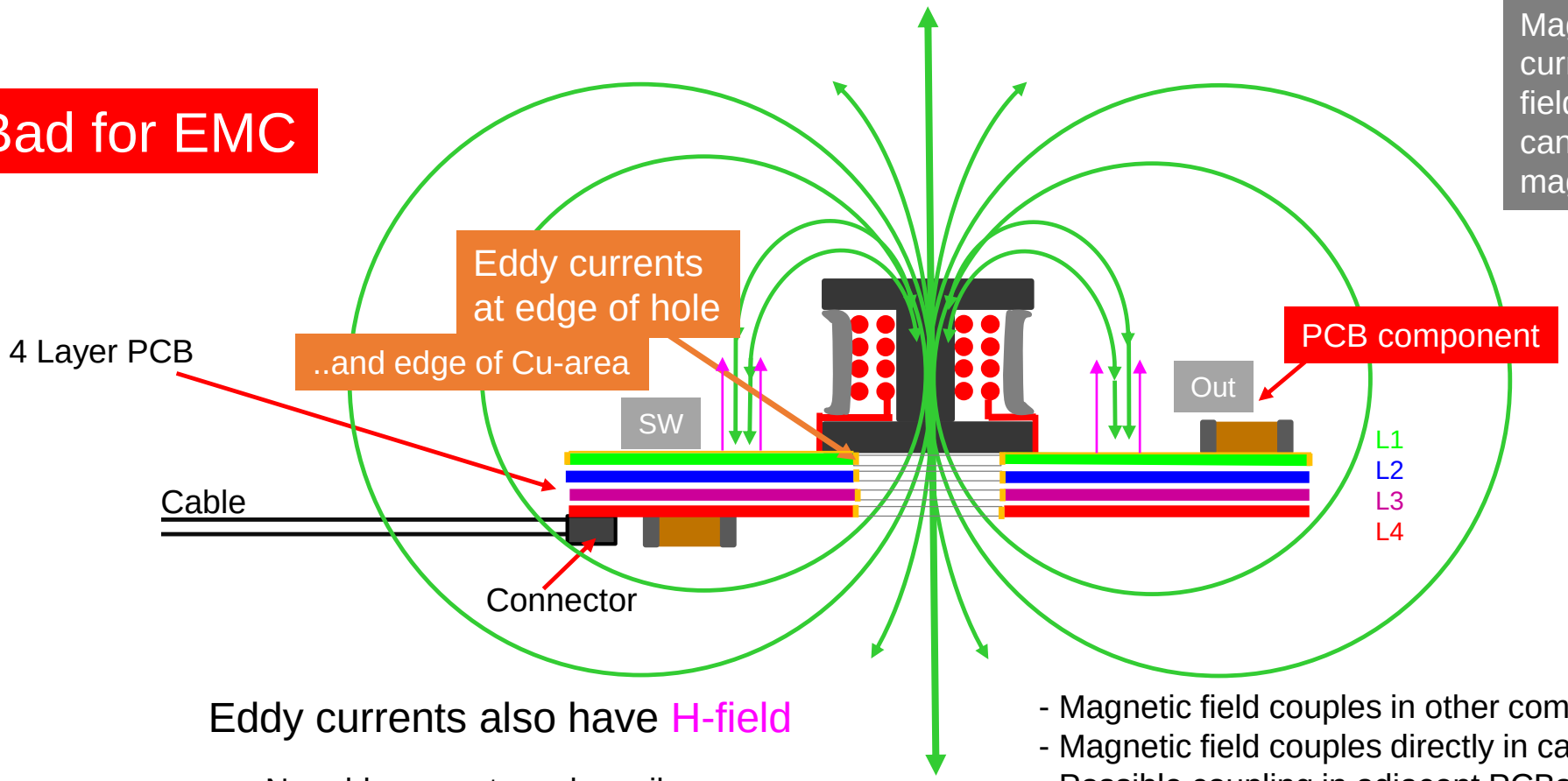
Which opinion is right?

Example 1: No Copper Under Coil in all Layers

Magnetic field lines close around PCB (sketch)

Very Bad for EMC

Magnetic field from Eddy currents on top of copper, field from Eddy currents cancels original AC magnetic field



Eddy currents also have H-field

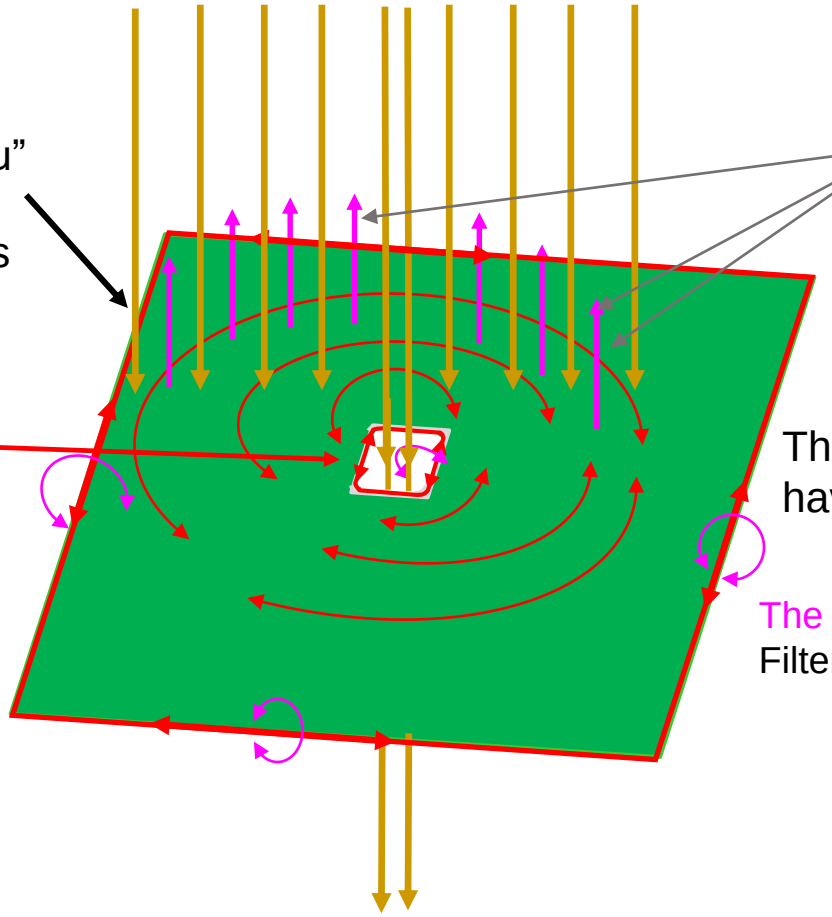
+ No eddy currents under coil
+ No reduction of effective inductance

NO “quiet” position on PCB for EMC filter

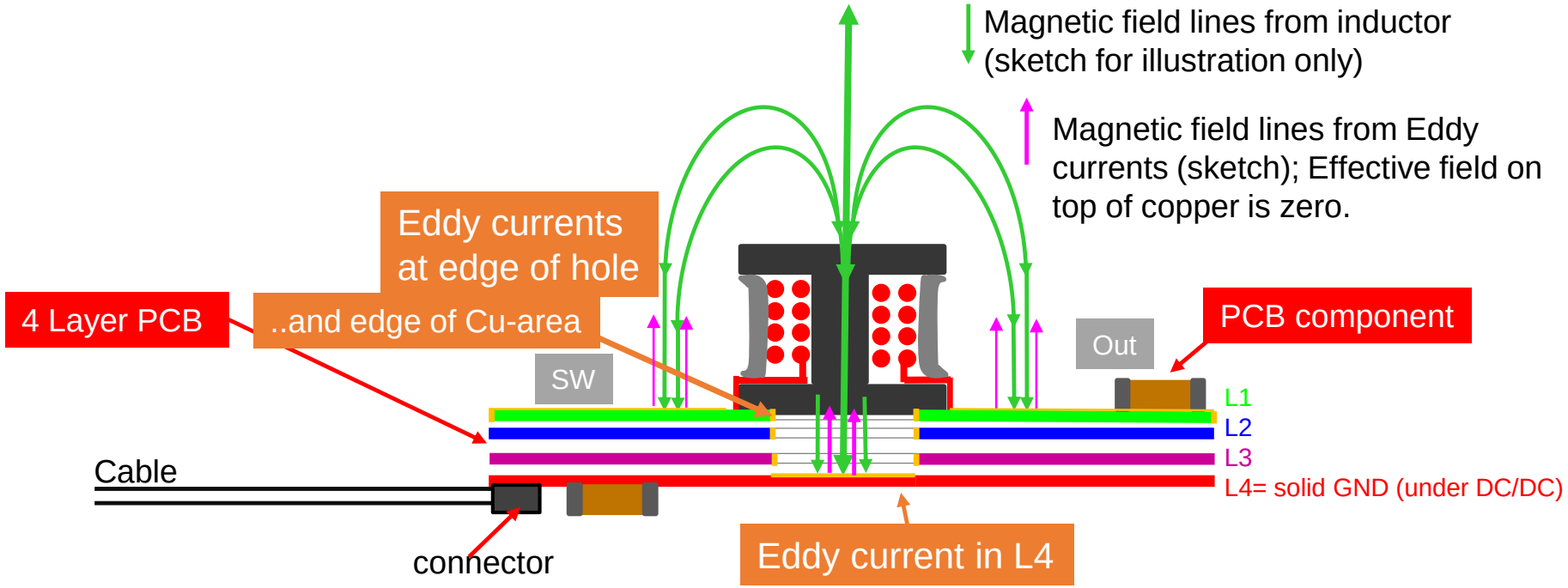
- Magnetic field couples in other components
- Magnetic field couples directly in cable
- Possible coupling in adjacent PCBs
- Eddy currents at edge of hole in all layers

Detailed Look on a PCB with a hole, exposed to AC magnetic field

Simplified sketch for illustration!



Example 2: Copper Under Coil in Layer 4

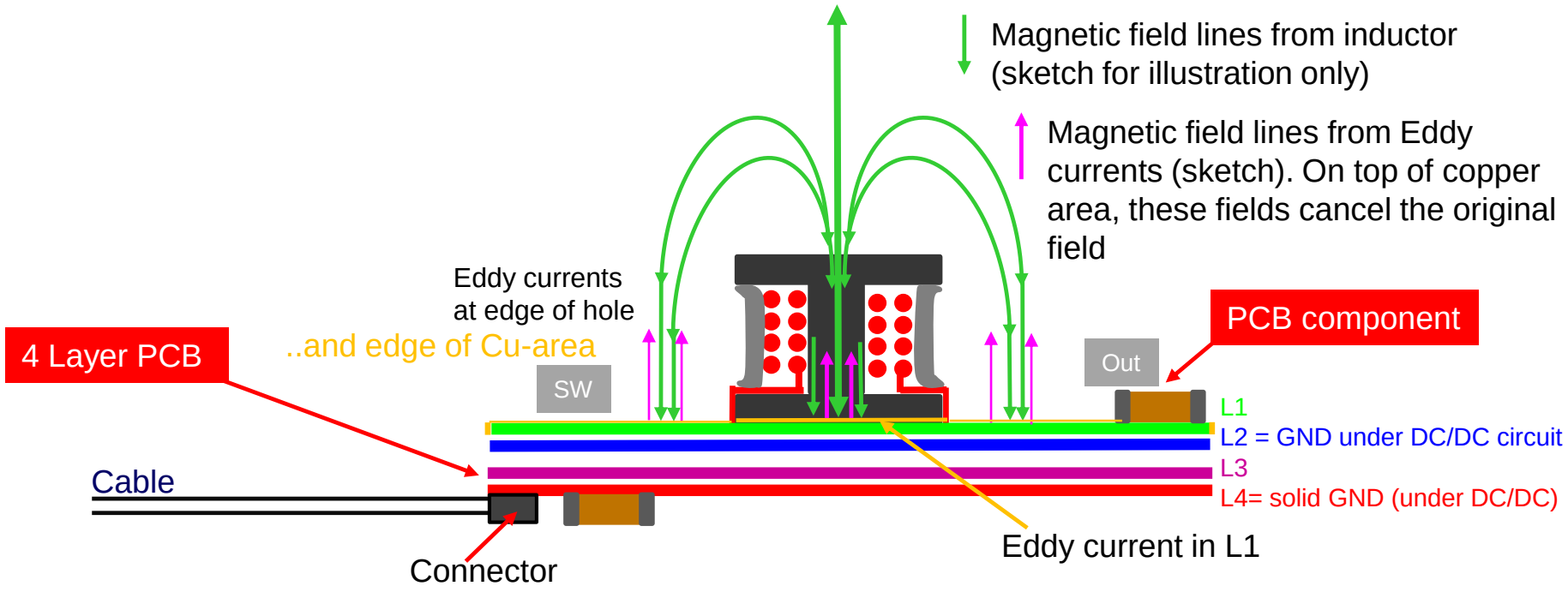


++ much lower magnetic field around PCB
+ less direct coupling into cable

- Losses in Cu due to Eddy currents
- Reduced effective inductance
- Eddy currents at edge of hole in L1-L3

- Bottom side of PCB much cleaner, but not completely clean
- Eddy currents flowing in L4 will create voltage drops across layer-impedance.
- Layer impedance is further increased by any holes or routings
- EMC filter components are referred to a noisy GND and therefore will not be fully effective

Example 3: Copper Under Coil in all Layers



+ No AC magnetic field on bottom side of PCB
+ No magnetic coupling into bottom side components

+ Reduced Magnetic field coupling in cable
+ Reduced coupling in adjacent PCBs
+ AC Magnetic fields only on top side of PCB
+ inner layer should be clean

- Losses in Cu due to Eddy currents
- Increased parasitic capacity of coil
- Reduced effective inductance
- Eddy currents under coil in L1 and at edge of Cu-area

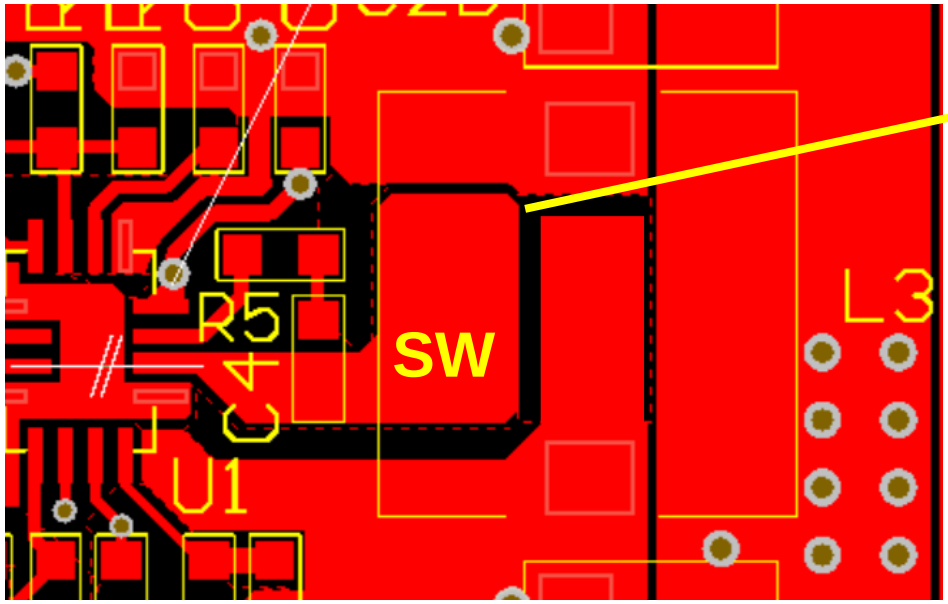
- Bottom side of PCB CLEAN
- EMC filter can be placed effectively here

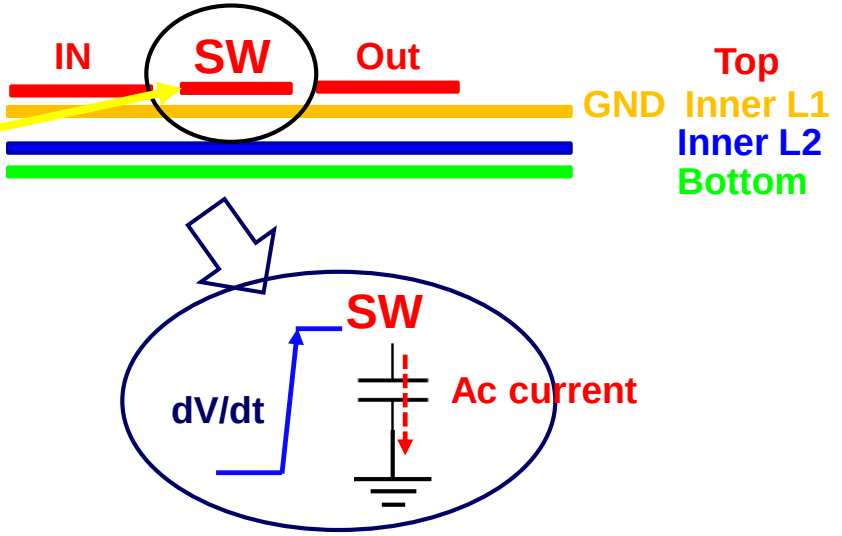
Place GND Copper Under SW-Node?

CON:

If copper is placed in the layer directly under SW-node, parasitic capacitance of SW is increased. An AC current will flow across that parasitic capacitor

Top side Layout Example EVQ4430





PRO:

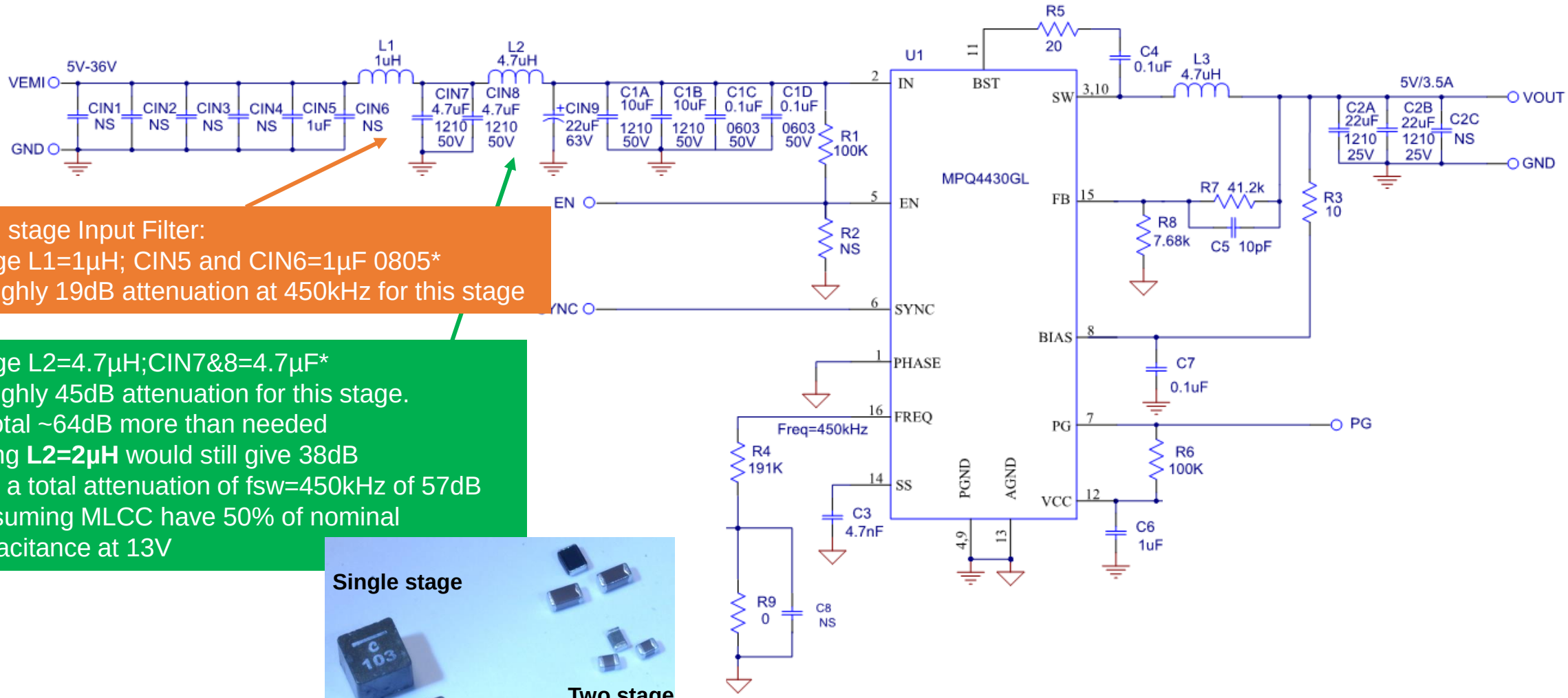
Solid GND under DC/DC will allow Eddy currents to mirror image the top side high di/dt current loop

- Parasitic Capacitor from SW to GND:
  C_sw = 17mm^2/0.1mm*4*8.85pF/m = 102pF
- Low-Side-Power FET: Coss ~ 3nF to 7nF
  this is around 30 times higher

Parasitic capacitance is negligibly small

Buck EMC Optimized Schematic

MPQ4430 Family: P2P 1A to 3.5A



Two stage Input Filter:
Stage L1=1µH; CIN5 and CIN6=1µF 0805*
Roughly 19dB attenuation at 450kHz for this stage

Stage L2=4.7µH;CIN7&8=4.7µF*
Roughly 45dB attenuation for this stage.
In total ~64dB more than needed
Using **L2=2µH** would still give 38dB
And a total attenuation of fsw=450kHz of 57dB
*assuming MLCC have 50% of nominal capacitance at 13V

T-EVQ4431-L-00A Top Side

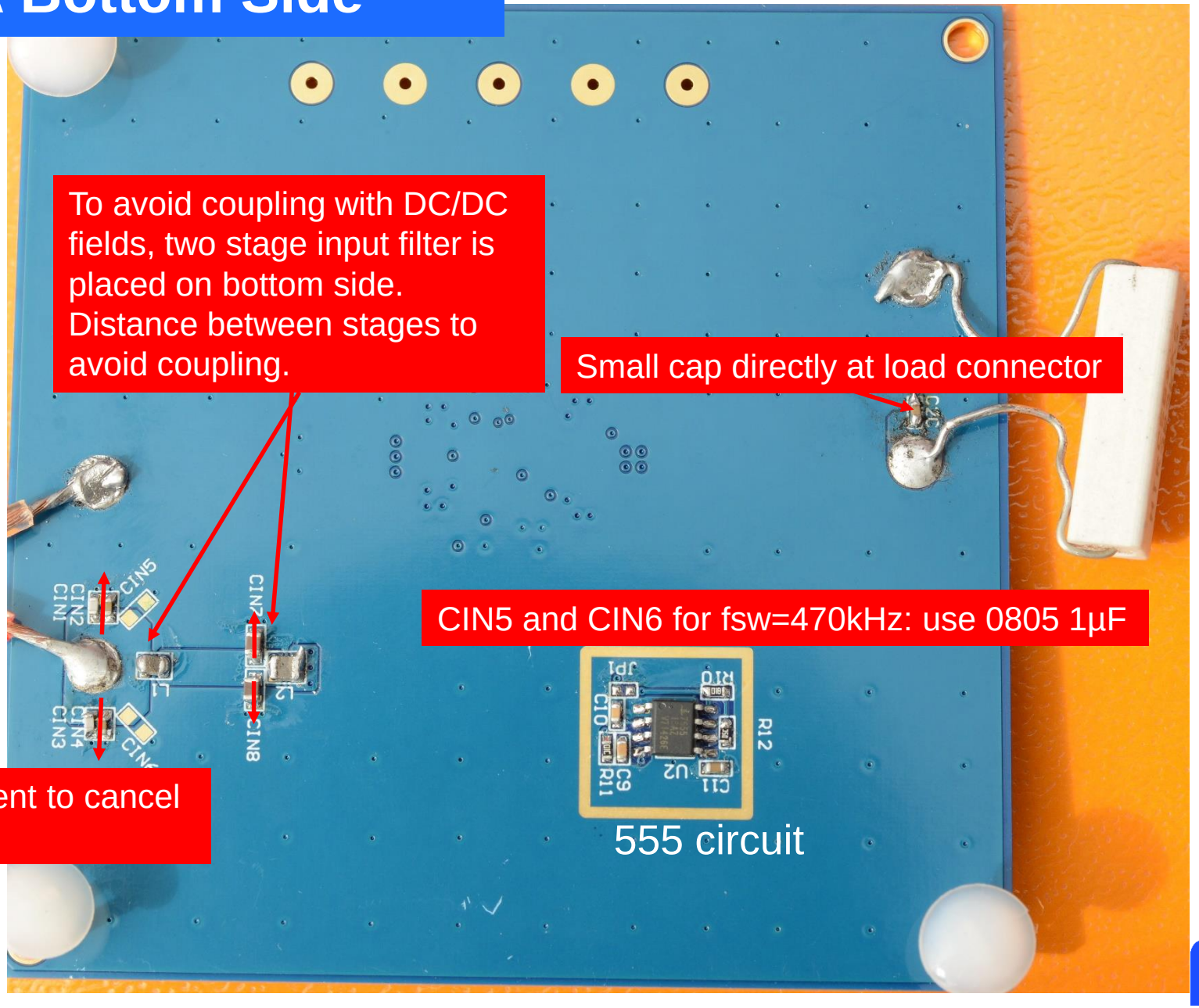
Cuts in Top GND to separate noisy PGND from clean GND

Two Cout are placed on both sides of coil

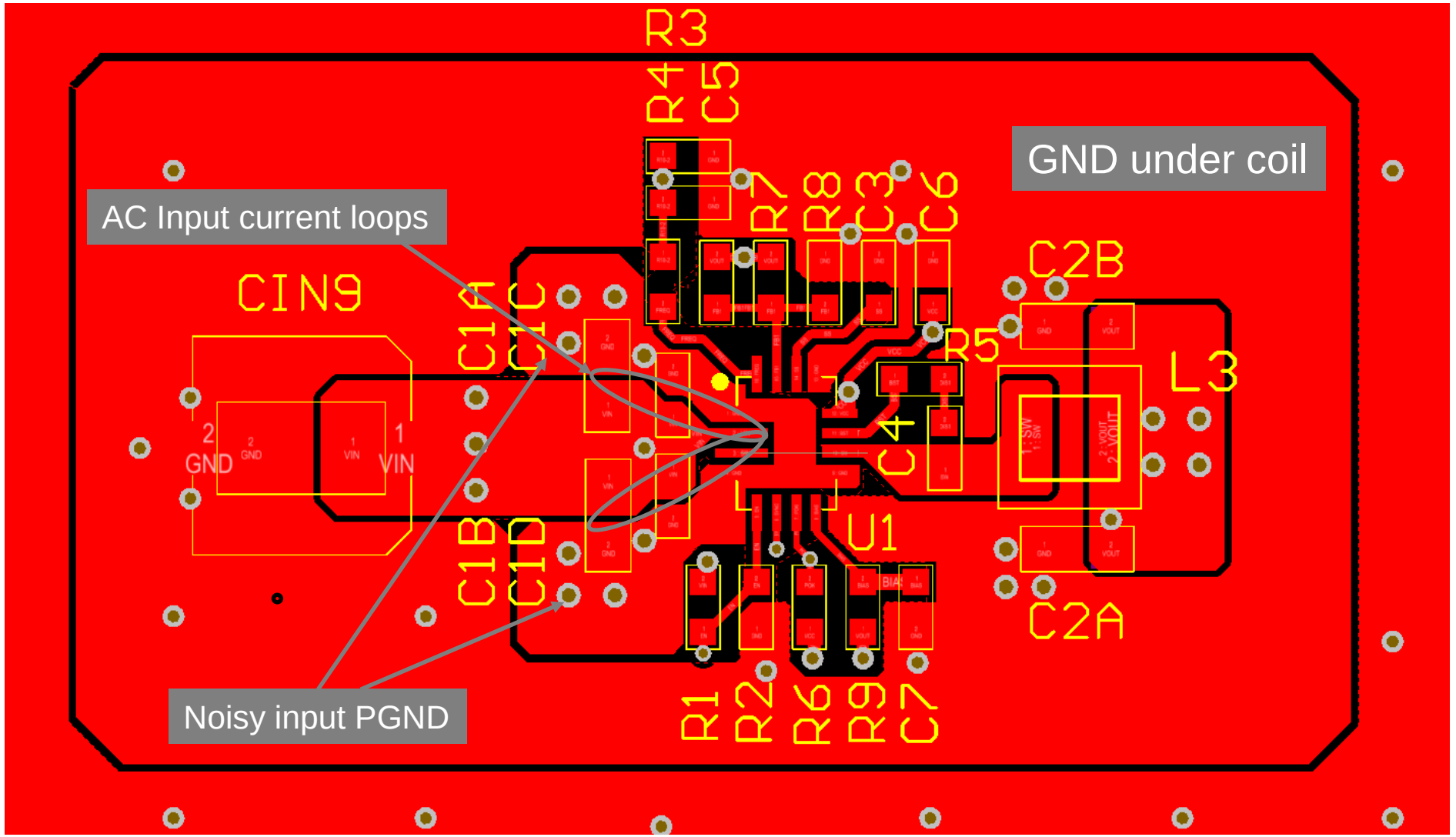
This shields part of E-Field radiation

Symmetric Cin arrangement

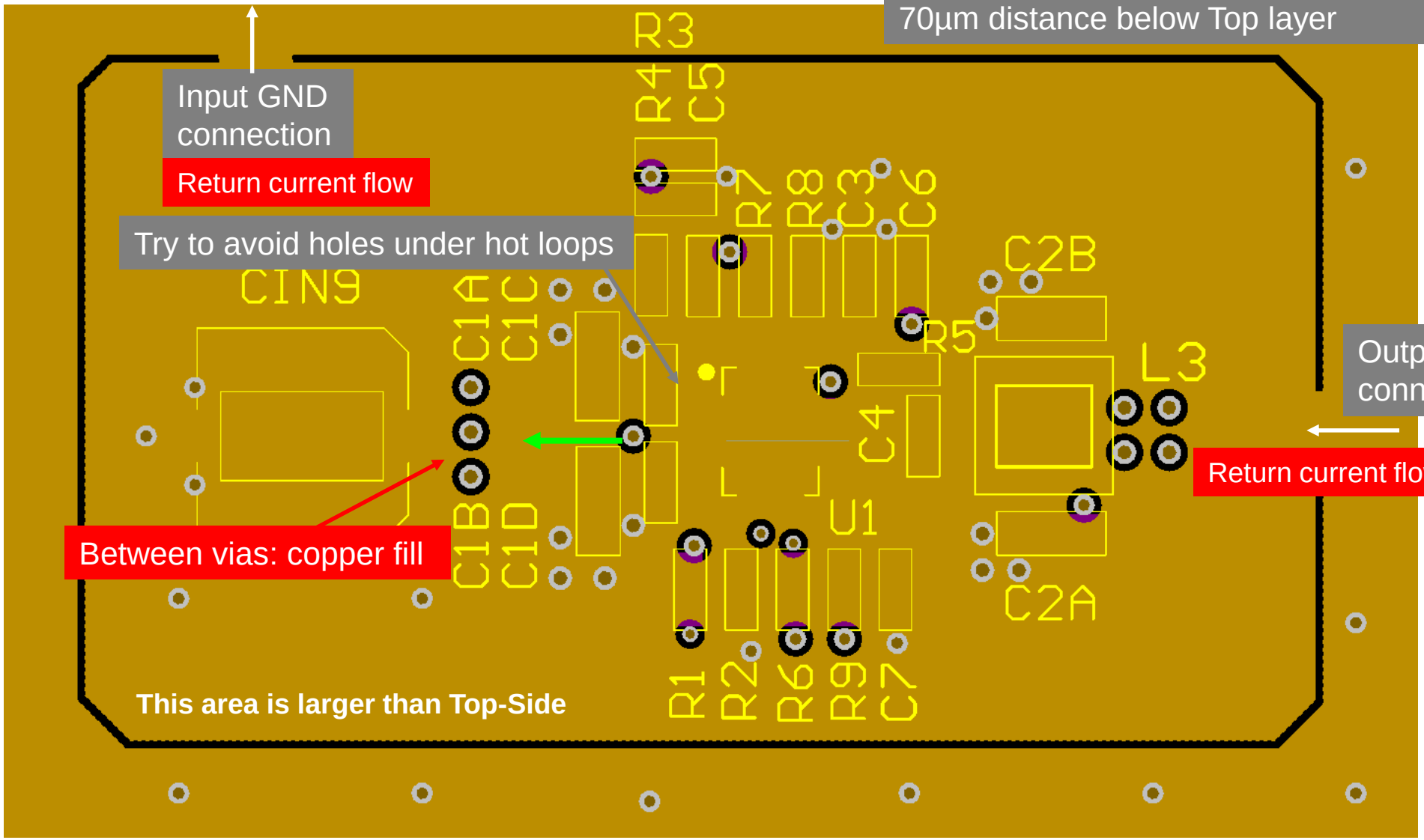
T-EVQ4431-L-00A Bottom Side



T-EVQ4431-L-00A Top Side Detail



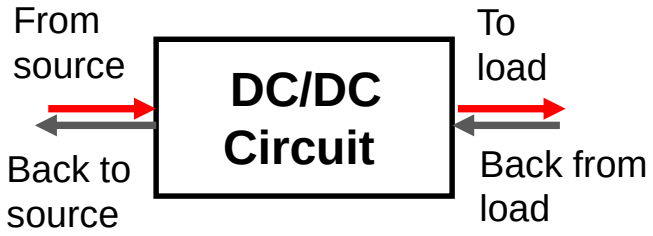
T-EVQ4431-L-00A Inner Layer 1 Detail

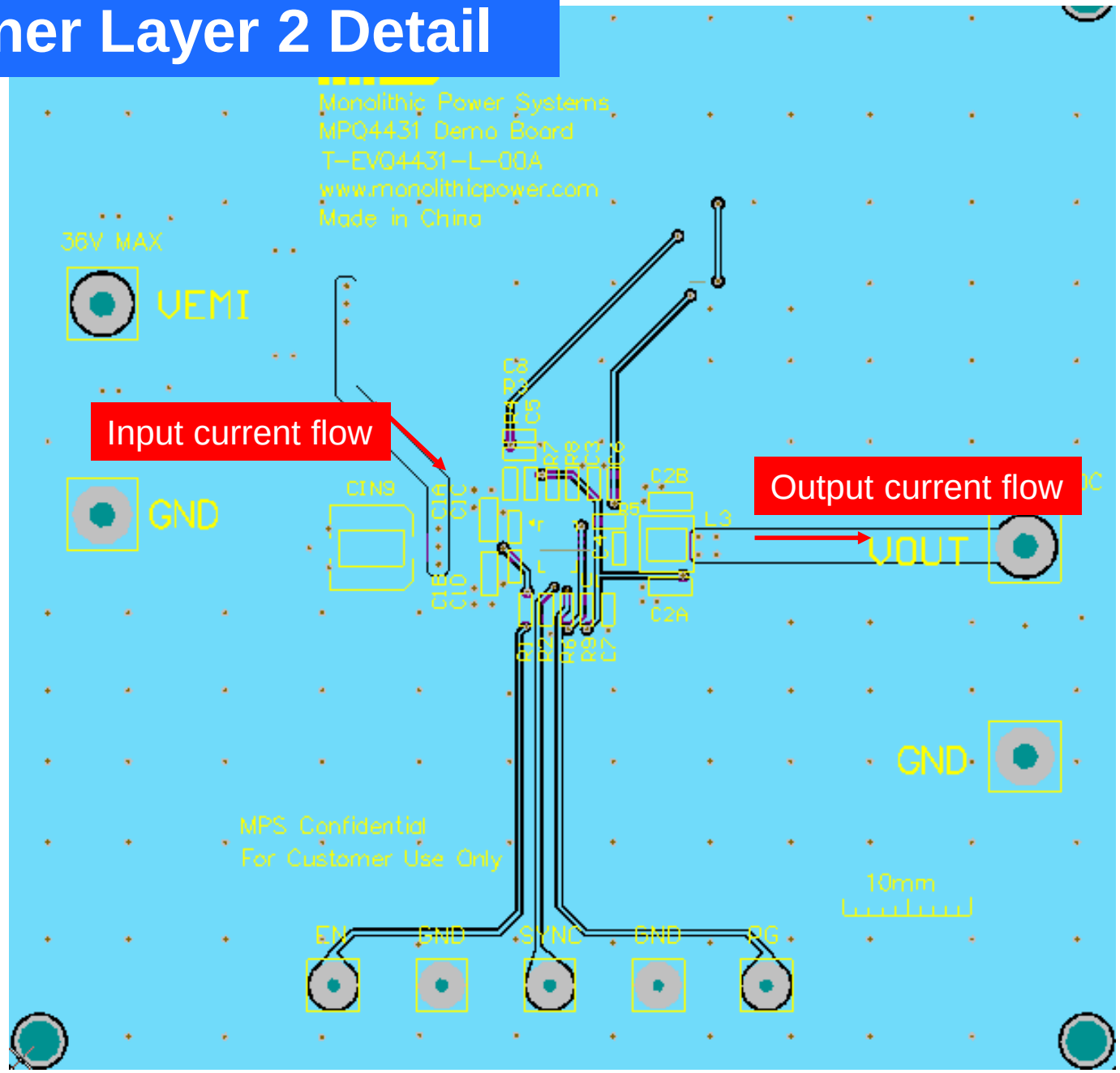


T-EVQ4431-L-00A Inner Layer 2 Detail

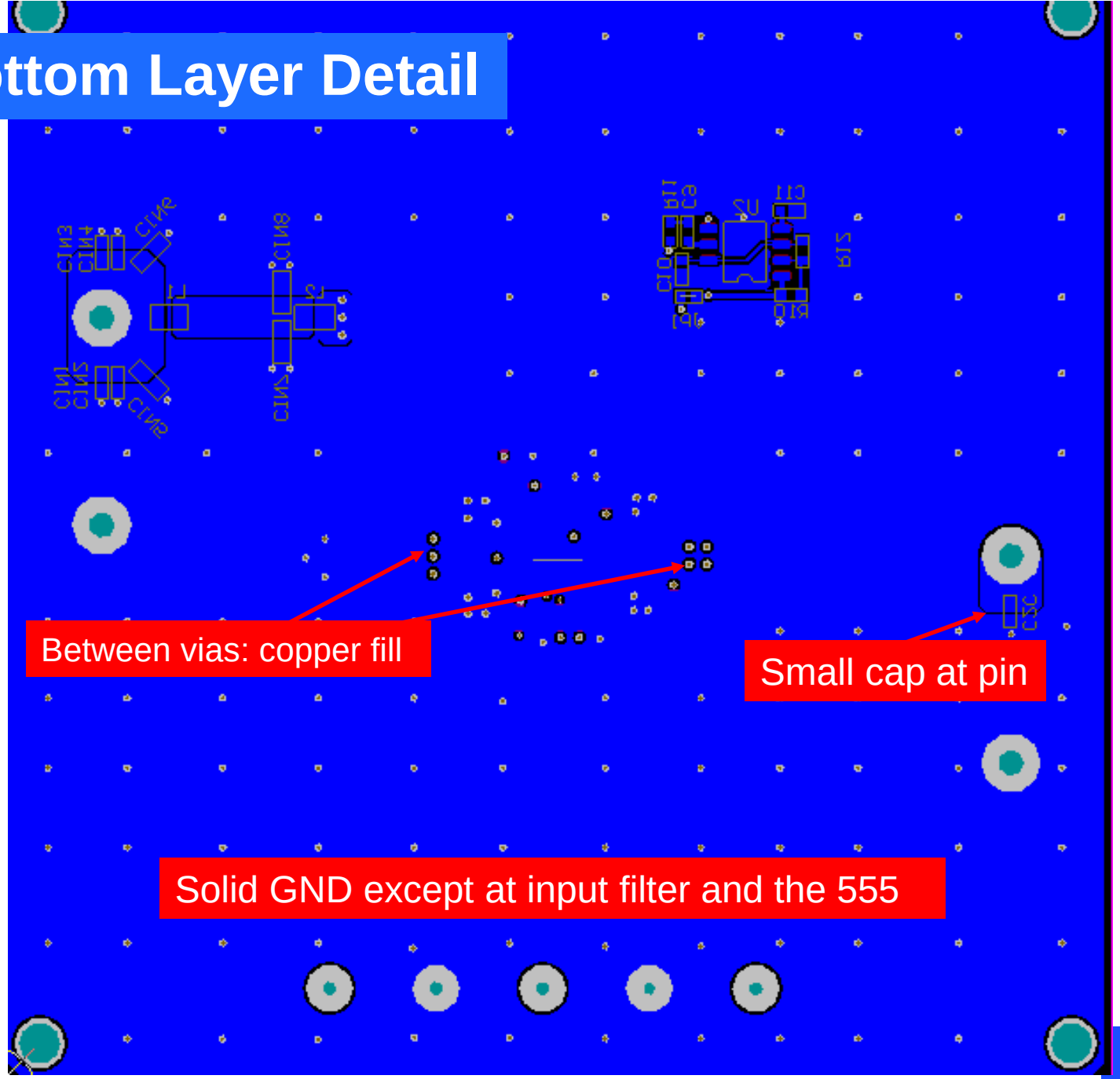
Inner L2 has 70μm distance to bottom layer

Input and Output are routed together with return



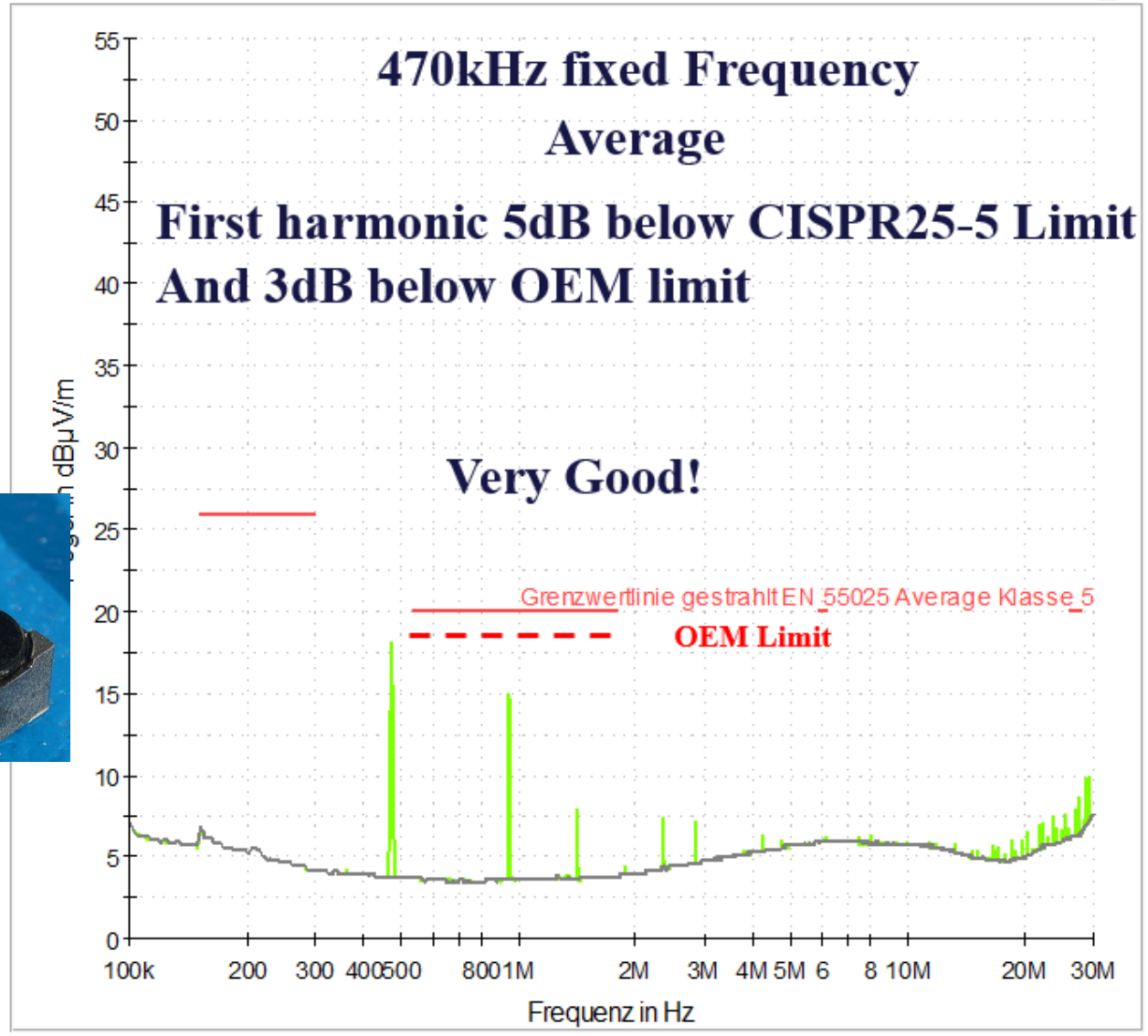


T-EVQ4431-L-00A Bottom Layer Detail



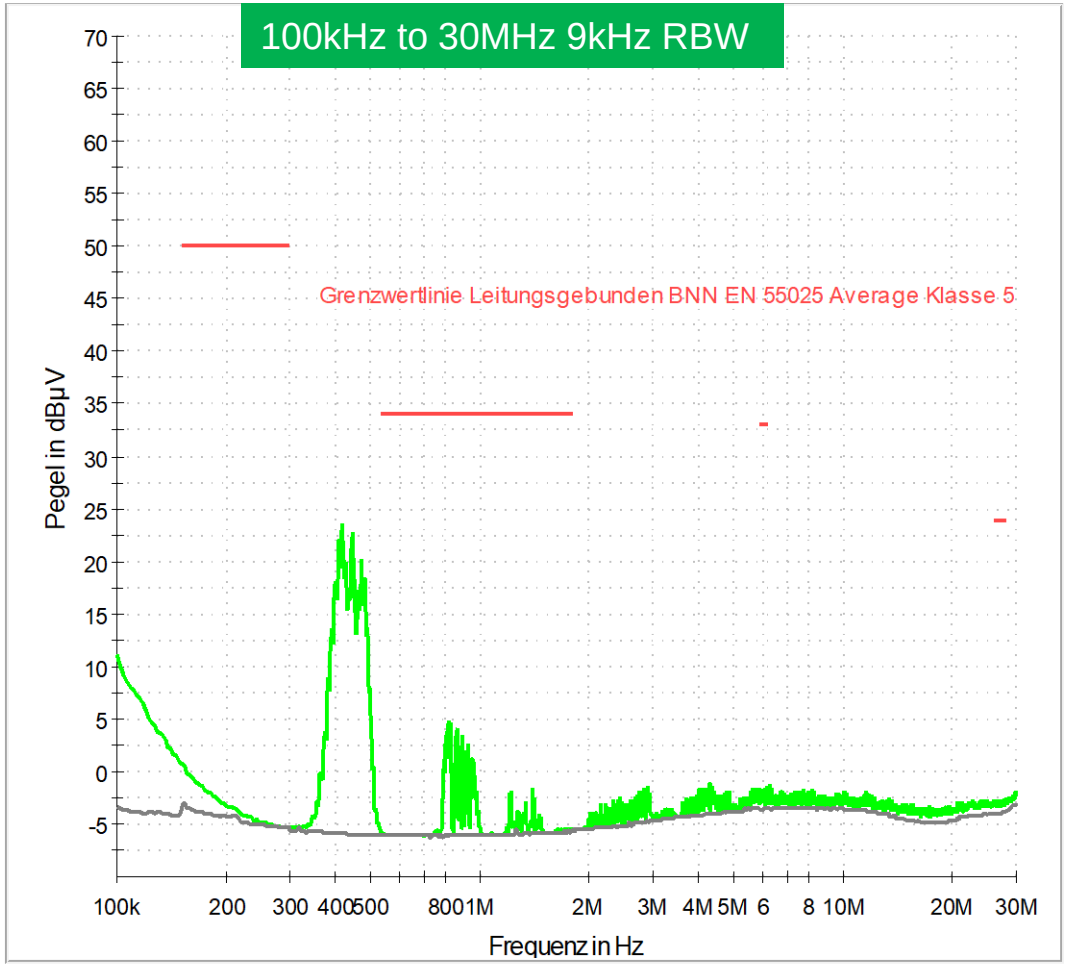
A Good Design

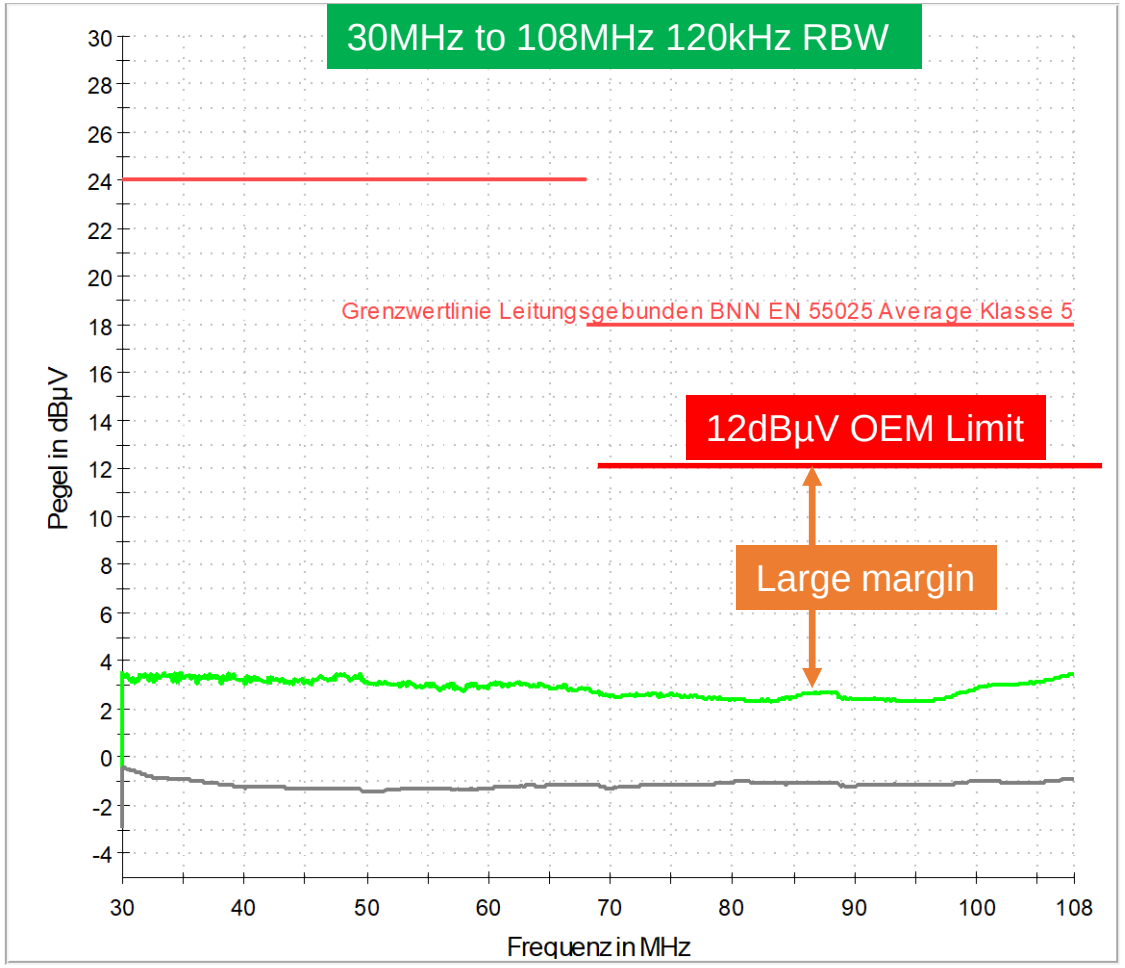
Radiated Emissions – 100kHz – 30MHz Monopole



Conducted Emission Test Results

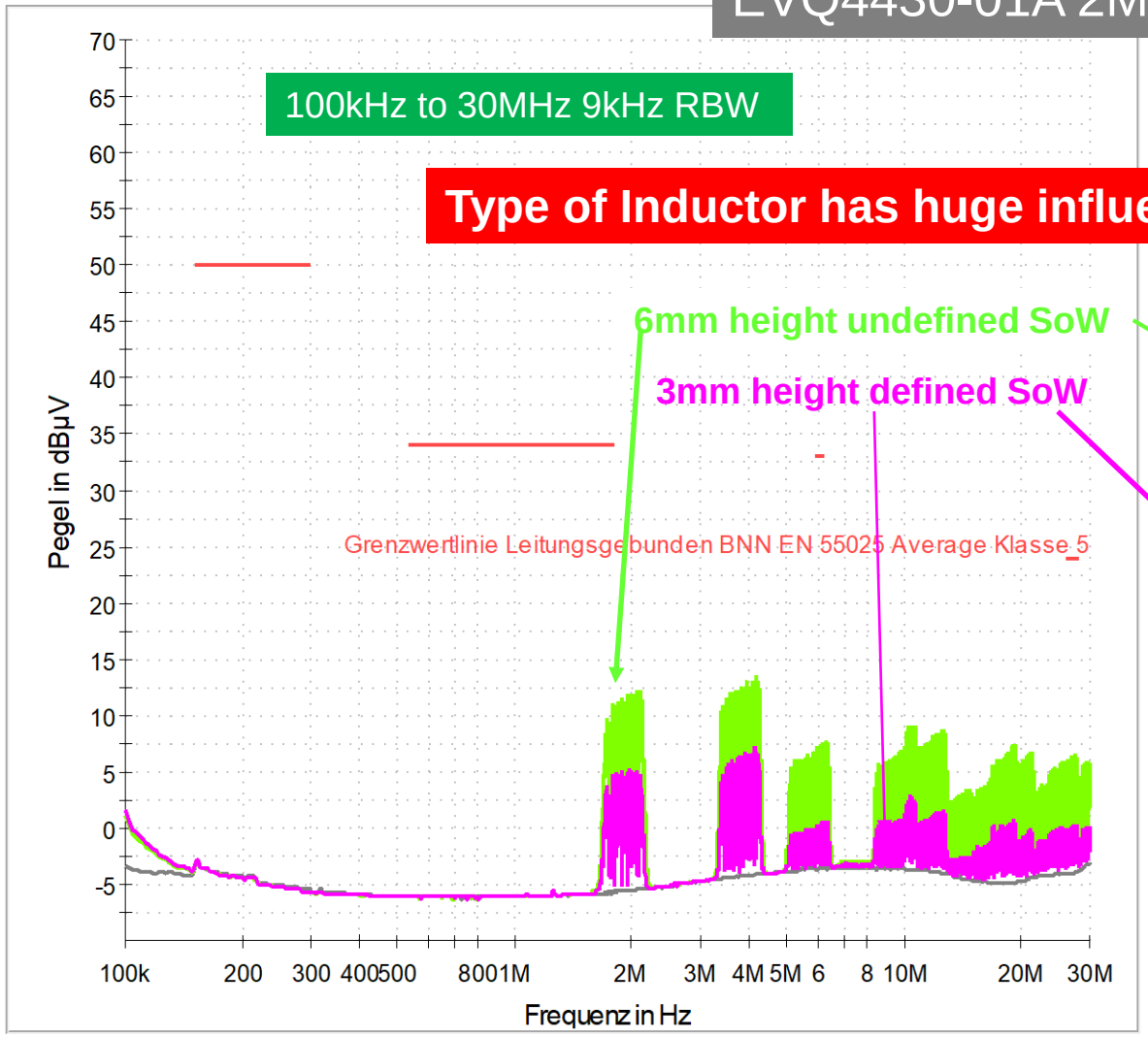
EVQ4430-00A 480kHz Spread Spectrum

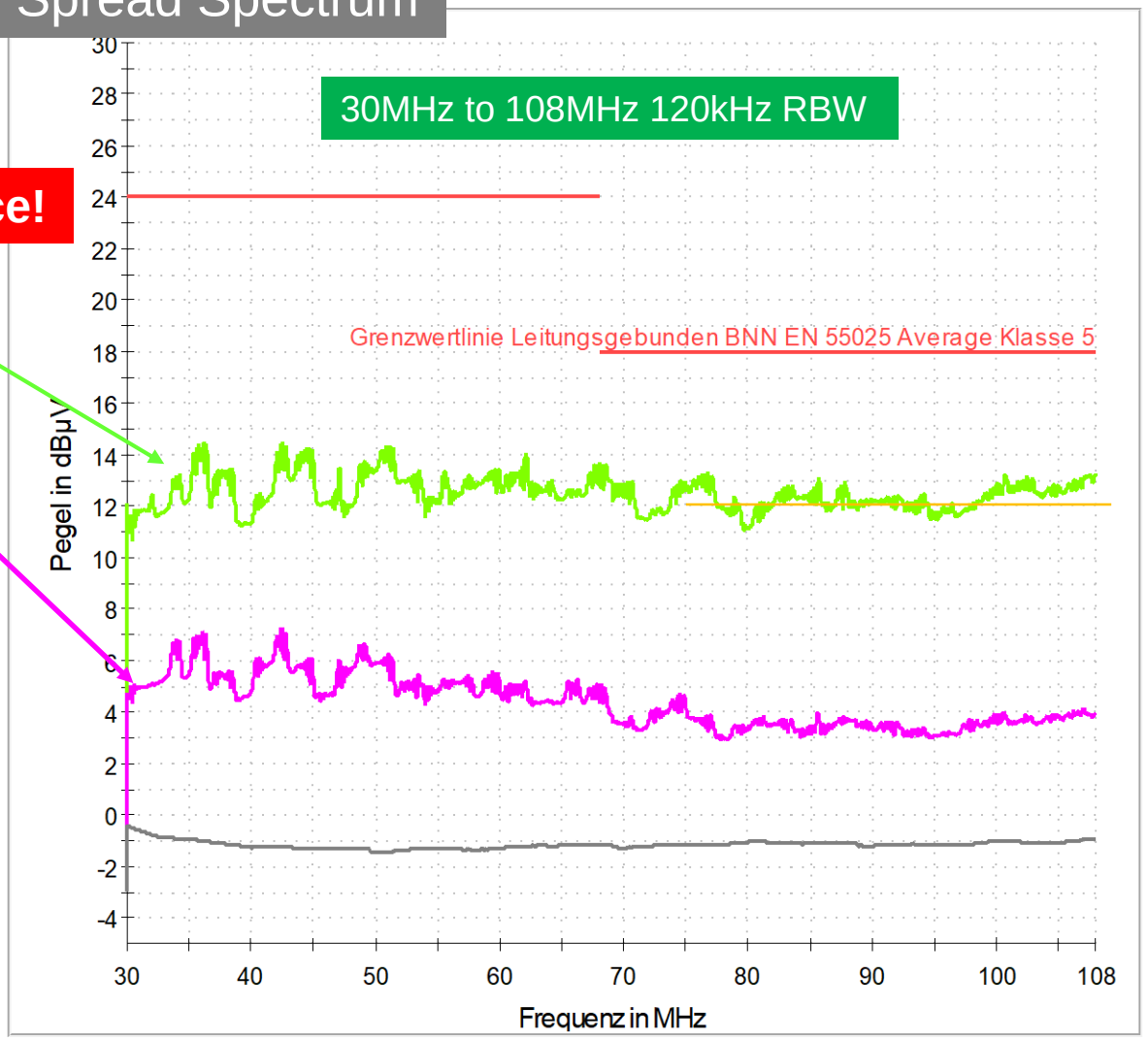




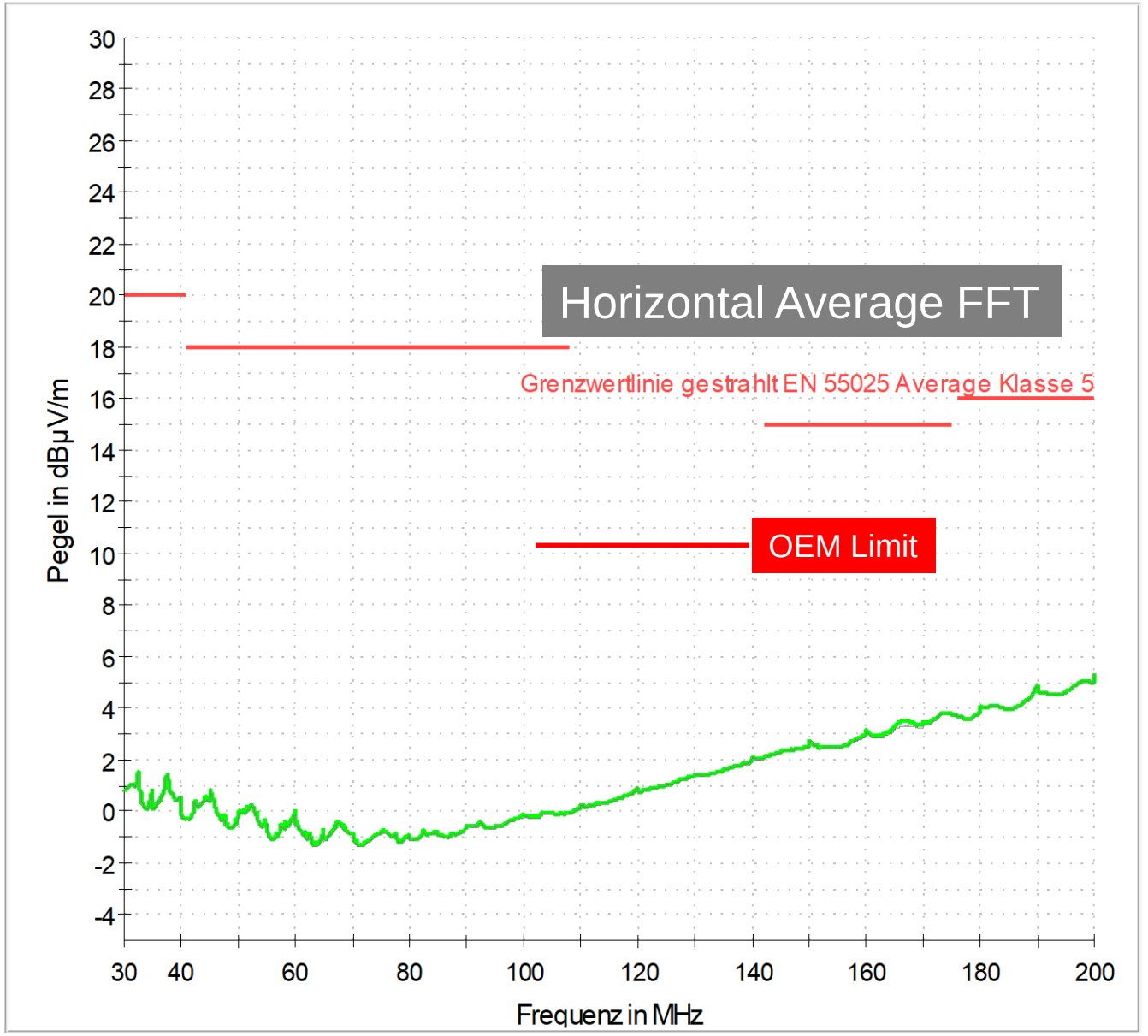
CE Test (avg) of 3A part with different 6x6mm coils

EVQ4430-01A 2MHz Spread Spectrum





Radiated Emissions 30MHz to 200MHz



Some Frequently Asked Questions About Layout for EMC

1. Why Al-Elco at Vin?
2. Is there any difference in output filtering for buck and boost topology? How about 4 switch buck boost?
3. Shall I connect AGND and PGND at the power IC or somewhere else?
4. When do you go for more than 4 layers?
5. Should you keep areas free of copper?
6. What to do with isolated copper islands?
7. Does the input connector shape / elevation above the board has any influence on EMI?
8. How to treat NC pins and thermal pad of the IC?
9. Optimum number/spacing of via holes to connect top layer ground to internal ground?

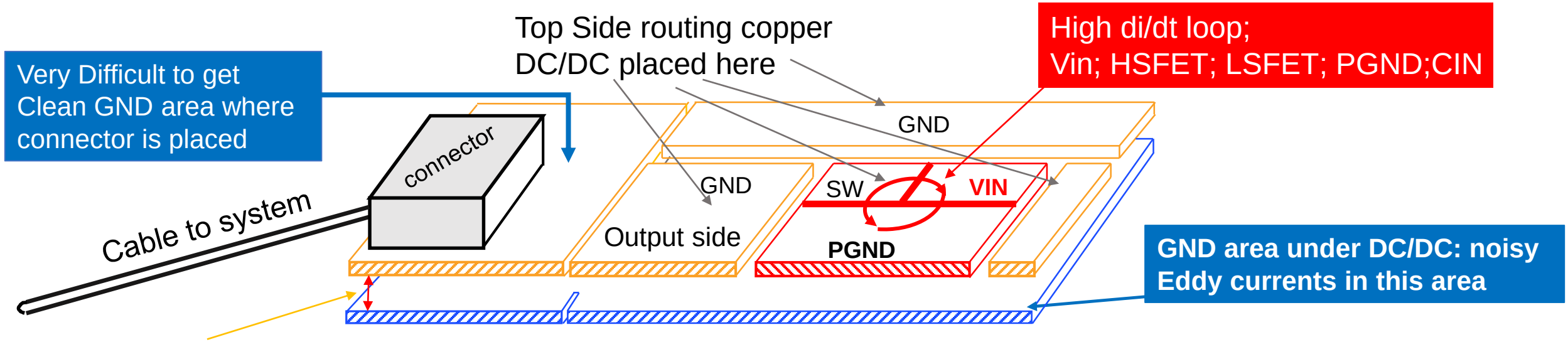
Thank You – Q&A

For more information, contact:
automotive@monolithicpower.com

Check out our AEC-Q100 Power Management Solutions at **MonolithicPower.com**

Backup Slides

How About A Two Layer Board?

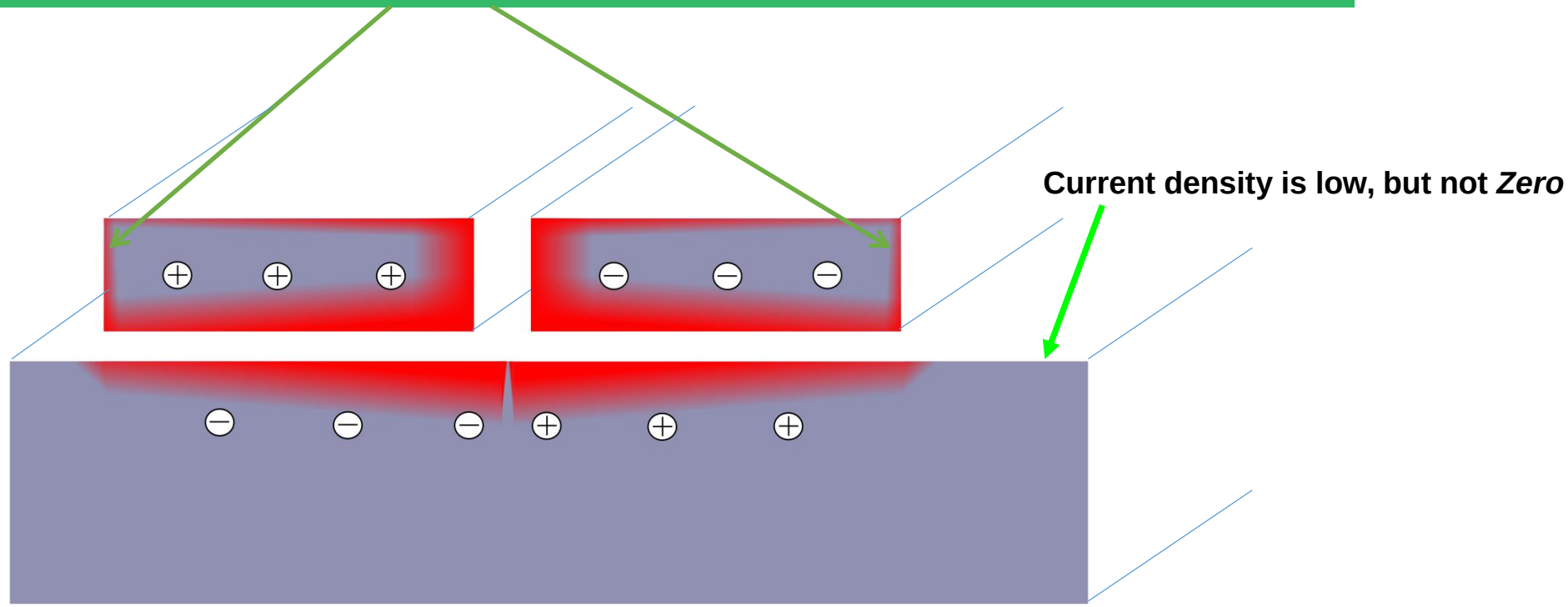


A) With two layer PCB it is difficult to provide solid GND area under the DC/DC circuit, as Bottom side is also for routing.

B) Compromise system reference GND vs. separation of noisy GND and clean GND. No clean Reference point!

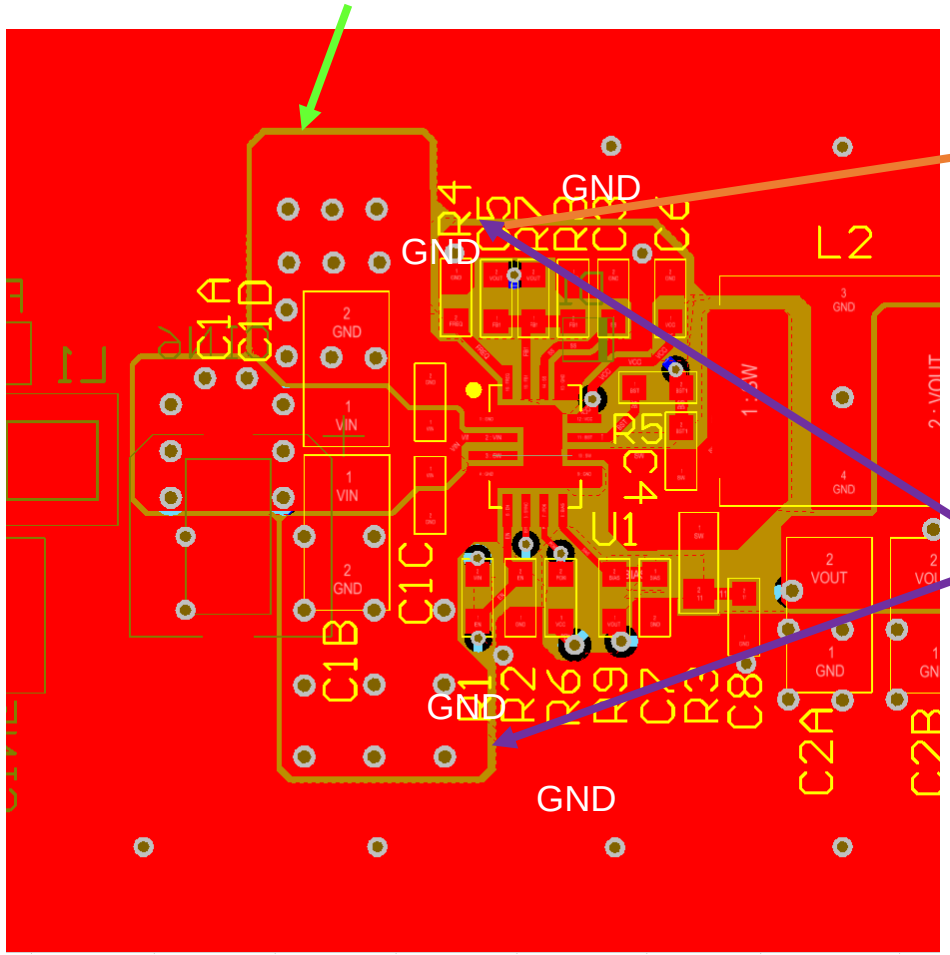
Magnetic Antennas

On AC current loops like hot loops, there is still an increased current density at the outside boundary of the loop

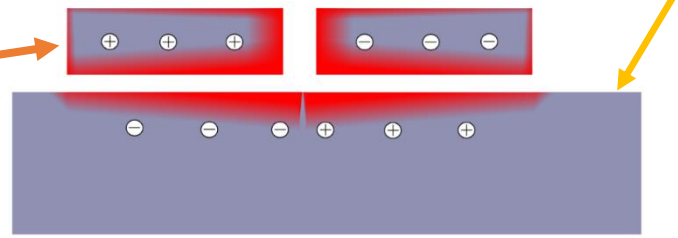


Magnetic Antennas

Cut around PGND to prevent AC current to disturb to layer



Still significant AC current here



That's the reason you might cut even the GND of the hot loop on the top side.

Otherwise there will still be some current density left at the edge of your PCB where it will radiate, and eddy current shielding is less effective