

Introduction

Whether traditional or cutting-edge, most high-voltage power converter topologies are comprised of transistors placed either in half-bridge or full-bridge combinations. Typically, a bootstrap technique is used to drive the high-side transistor when a negative voltage is not required for the gate. While this technique seems simple and straightforward, special care must be taken when dealing with AC grid periods, such as in a totem-pole converter application, due to their low frequency.

This article will describe potential challenges when driving these totem-pole transistors with a focus on the slow leg in a totem-pole converter, as well as how to resolve this challenge.

Slow Leg in a Totem-Pole Converter

The slow leg in a totem-pole converter can be implemented with diodes, but this can lead to high conduction losses; instead, it is recommended to use totem-pole transistors (Q_1 and Q_2) with a low resistance to improve efficiency (see Figure 1).

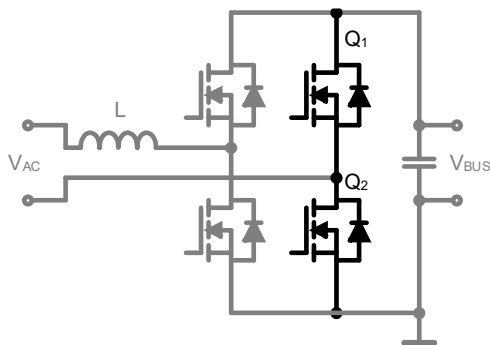


Figure 1: Slow Leg in a Totem-Pole Converter

In this set-up, the current flows through the body diode and the totem-pole transistor switches on when a threshold is reached. Figure 1 shows how the same gate-source waveform for both transistors is shifted 180° (see Figure 2).

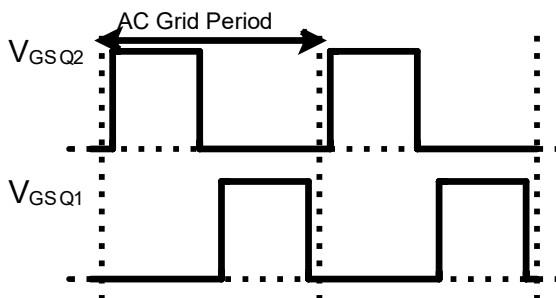


Figure 2: Gate-Source Waveforms of Both Transistors

Figure 3 shows the waveforms when a high-side transistor gate is not properly driven in a 3kW totem-pole converter (50Hz grid).

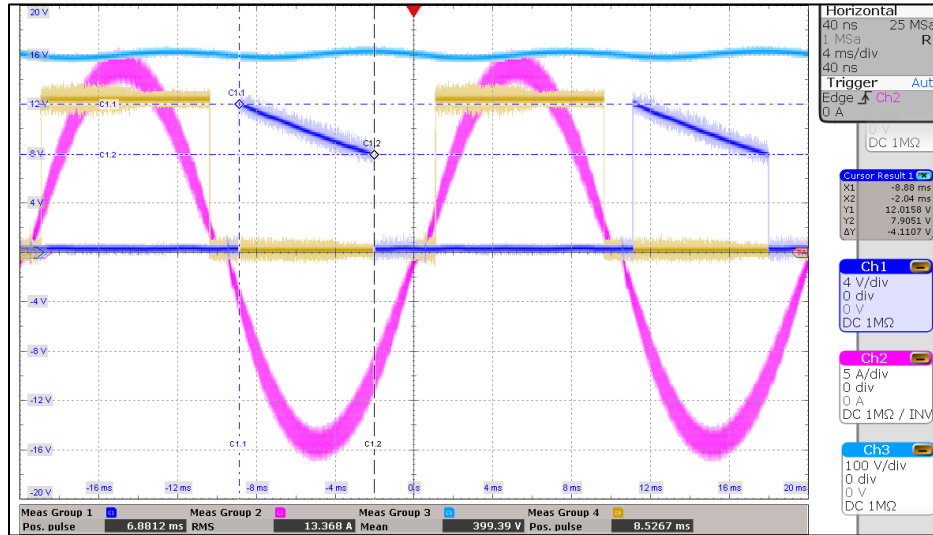


Figure 3: TP Waveforms with Bad V_{GSQ1} (CH1: V_{GSQ1} , CH2: I_L , CH3: V_{BUS} , CH4: V_{GSQ2})

Both gates should have same pulse width, but this is not the case, as the on times are 8.52 and 6.88ms. This means that Q_1 current flows through the diode instead of the totem-pole transistor's channel for 1.64ms, which increases losses.

If we take a closer look, we realize that Q_1 switches off at $V_{GSQ1} = 8V$, which makes sense because this is the driver's under-voltage lockout (UVLO) threshold. To have the same on time (t_{ON}) for both switches, we could select a driver with a lower UVLO threshold; however, this is not a good solution because the transistor will not have the gate voltage needed to operate normally. Additional analysis is required to determine the problem.

Bootstrap Technique

When no negative voltage is needed to turn off the transistor, the bootstrap technique is the simplest way to power the high-side gate driver in a half-bridge configuration. Figure 4a shows the half-bridge driver using the [MP18831](#), while Figure 4b shows the half-bridge driver when Q_1 turns on.

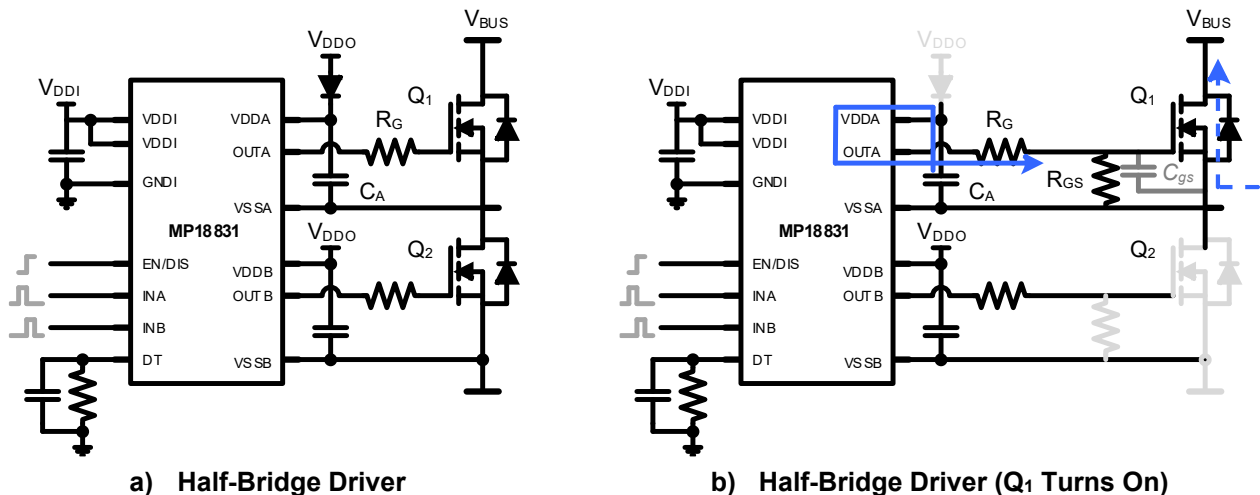


Figure 4: Half-Bridge Driver Schematic

Table 1 shows the most common behaviors for a half-bridge driver.

Table 1: Bootstrap Steps

State	Q ₁	Q ₂	Comments
0	0	0	VSSA floating.
1	0	1	VSSA to GND > D is forward biased > C _A is charged to about V _{DDO} .
2	1	0	VSSA to V _{BUS} > D is reverse biased, blocking V _{BUS} > C _A is discharged to drive Q ₁ .
3	1	1	Not allowed (V _{BUS} short circuit). Most half-bridge drivers have dead-time protection.

However, since the half-bridge driver is being used for a synchronous rectifier leg, there are two main differences regarding the capacitor (C_A) that stores the energy needed to turn on Q₁.

- C_A is charged before Q₂ turns on because current is already flowing through the body diode of Q₂ (see Figure 5).
- C_A is still being discharged even though Q₁ has already switched off (but with a smaller slope).

Figure 5 is similar to Figure 3, but Figure 5 shows the waveform while overlapping the C_A voltage (denoted in gray).

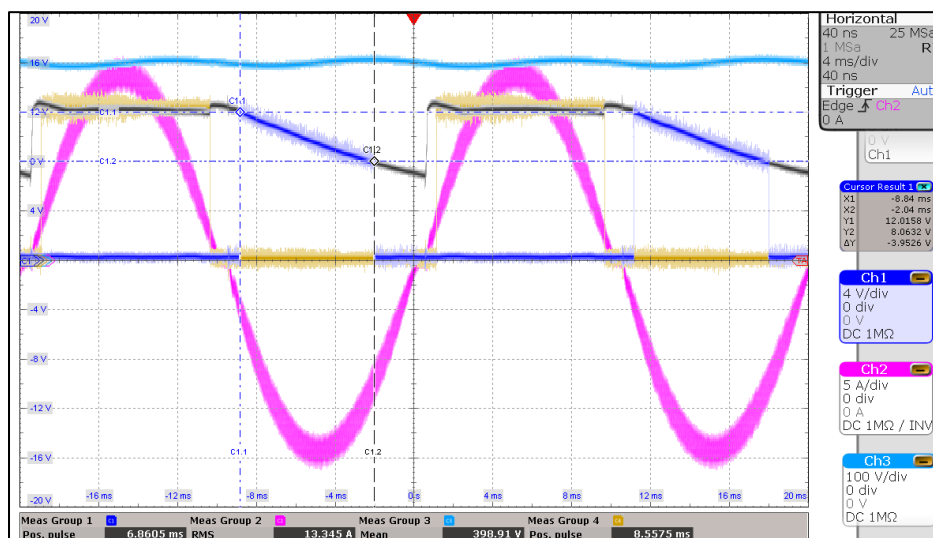


Figure 5: Adding the Capacitor Voltage (CH1: V_{GSQ1}, CH2: I_L, CH3: V_{BUS}, CH4: V_{GSQ2}, REF: V_{CA})

Even when no voltage being applied to the gate, why is the capacitor still being discharged?

The next sections will describe what causes a slow leg to occur.

Causes of Malfunctions

The capacitor discharges even when no voltage is applied to the gate because the half-bridge driver draws current from the capacitor to supply its inner circuits (e.g. bandgap and UVLO). In this scenario, the current drawn is the output-side quiescent current.

When focusing on the state in which Q₁ is on, the energy stored in the capacitor is used to power the drive. When Q₁ is on, there is some leakage through the gate-source resistance (R_{GS}). The gate resistance (R_G) is not considered because R_G << R_{GS}.

The total charge (Q_{TOT}) can be calculated with Equation (1):

$$Q_{TOT} = Q_G + Q_Q + Q_R \quad (1)$$

Where Q_G is the transistor's total gate charge, Q_Q is the charge related to the driver's high-side quiescent current, and Q_R is the charge related to R_{GS}.

The transistor's total gate charge can be obtained from the datasheet, while Q_Q and Q_R can be estimated with Equation (2) (considering constant values):

$$Q_{Q/R} = I \times t \quad (2)$$

Equation (1) and Equation (2) can be applied for Equation (3):

$$Q_{TOT} = Q_G + [I_Q + (V_{CA} / R_{GS})] \times t_{ON_Q1} \quad (3)$$

$$Q_{TOT} = 275nC + (2.182mA + 10V / 10k\Omega) \times 6.86ms = 22.1\mu C$$

Where I_Q is the driver's output-side supply current, I_{RGS} is the current through R_{GS} (denoted as V_{CA} / R_{GS} in Equation (3)), t_{ON_Q1} is the high-side resistor's on time, and V_{CA} is the capacitor's average voltage during t_{ON_Q1} . ^{(1) (2) (3)}

Notes:

- 1) I_Q has been measured.
- 2) t_{ON_Q1} was obtained from the oscilloscope's waveform.
- 3) The average value has been used for V_{CA} .

Two capacitors in parallel are used for C_A (1 μ F and 4.7 μ F). Based on the datasheet value and considering the DC bias, we obtain a C_A of 5.14 μ F.

The capacitor's voltage drop (ΔV_{CA}) can be estimated with Equation (4):

$$\Delta V_{CA} = Q / C_A \quad (4)$$

$$\Delta V_{CA} = 22.1\mu C / 5.14\mu F = 4.3V$$

This result is close to the value observed in the previous figures (about 4V), and the main error is the capacitor's tolerance.

For this example, the half-bridge driver causes 67.7% of the voltage drop; meanwhile, the resistance causes 31% of the voltage drop, and the totem-pole transistor contributes only 1.2%. With this in mind, the best way to improve the voltage drop is to choose a better driver.

Comparing Half-Bridge Drivers

The output-side quiescent current for one channel was measured with the three half-bridge drivers, including the MP18831 (see Table 1).

Table 2: Quiescent Current Measurement

Driver	Measured (IN = 0 / IN = 3.3V) (μ A)	Datasheet (Typ) (μ A)	Datasheet (Max) (μ A)
MP18831 (Driver 1)	898 / 934	1000	1300
Driver 2 ⁽⁴⁾	1086 / 1194	1000	1800
Driver 3 ^{(4) (5)}	2143 / 2182	2300	2800

Notes:

- 4) Drivers with same specifications were selected (4A, UVLO threshold = 8V, dead time, enable).
- 5) The conditions: VDDI = EN = 3.3V, VDDb = 12V. Chroma 12061 Multimeter used for measuring.

Due to its small quiescent current, the MP18831 is a suitable choice for half-bridge legs with a low frequency. Figure 6 shows a waveform where the MP18831 is denoted in blue and Driver 3 is denoted in gray.

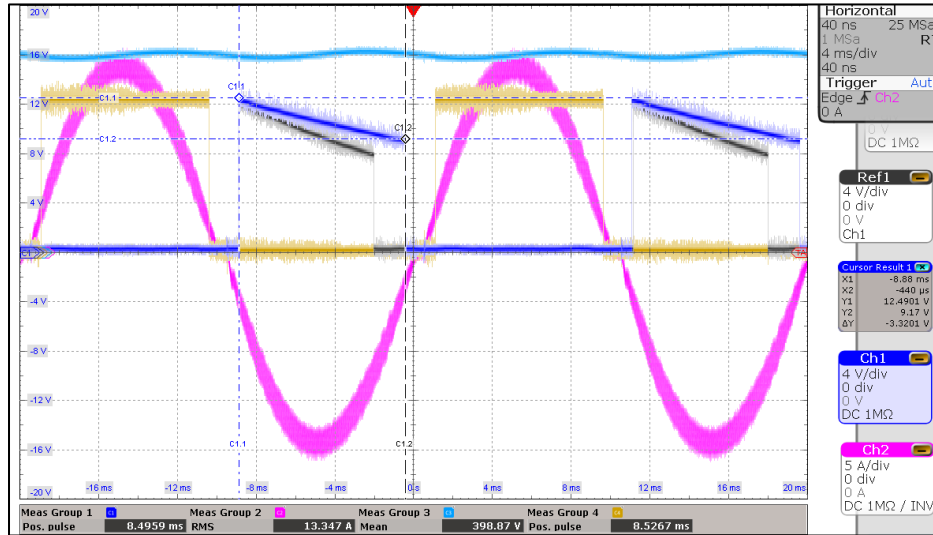


Figure 6: MP18831 vs. Driver 3 (CH1: V_{GSQ1_MPS} , CH2: I_L , CH3: V_{BUS} , CH4: V_{GSQ2} , REF: $V_{GSQ1_DRIVER2}$)

In this scenario, the high-side and low-side pulses have the same width (no extra current flows through the body diode of Q_1). The voltage drop is about 3.32V, which is close to its theoretical value of 3.39V.

The voltage drop was calculated with Equation (3) and Equation (4). Table 3 shows the parameters.

Table 3: Parameters

Q1 Gate Charge Q_G (nC)	Quiescent Current (I_{VDDX_Q}) (mA)	Q1 On Time (t_{ON_Q1}) (ms)	HS Capacitor (C_A) (μF)	HS Voltage (V_{CA}) (V)	Resistor GS (R_{GS}) (k Ω)
275 ⁽⁶⁾	0.934 ⁽⁷⁾	8.5 ⁽⁸⁾	5.14 ⁽⁶⁾	10.83 ⁽⁸⁾	10

Notes:

- 6) Obtained from datasheet.
- 7) Obtained from measurement.
- 8) Obtained from oscilloscope waveform.

If we double R_{GS} , the voltage drop can be reduced to 2.69V (2.52V if calculated) (see Figure 7).

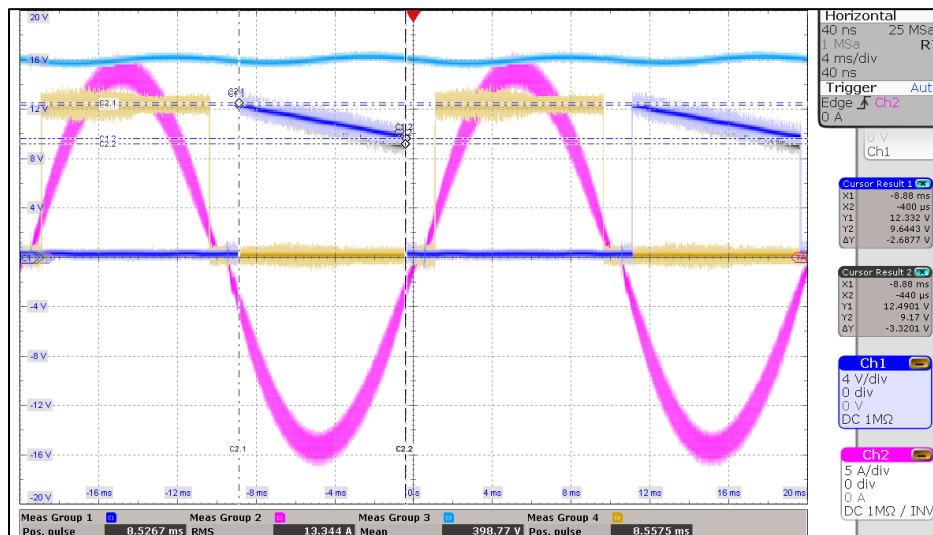


Figure 7: 10k Ω vs. 20k Ω (CH1: $V_{GSQ1_20k\Omega}$, CH2: I_L , CH3: V_{BUS} , CH4: V_{GSQ2} , REF: $V_{GSQ1_10k\Omega}$)

Although the converter is working properly, the design must be improved for better reliability.

Proper and Reliable Solution

Because it determines the voltage drop, the capacitor is a key component when determining design reliability. Considering the tradeoff between a 0V voltage drop and the minimum voltage drop to avoid triggering UVLO. In the worst-case scenario, the voltage drop is about 1.5V.

By reorganizing Equation (3) and Equation (4), we can calculate the required capacitance with Equation (5):

$$C_A = Q_G + [I_Q + (V_{CA} / R_{GS})] \times t_{ON_Q1} / \Delta V_{CA} \quad (5)$$

Table 4 shows the relevant parameters.

Table 4: Parameters

Q1 Gate Charge Q_G (nC)	Quiescent Current (I_{VDDX_Q}) (mA)	Q1 On Time (t_{ON_Q1}) (ms)	Voltage Drop (ΔV_{CA}) (V)	HS Voltage (V_{CA}) (V)	GS Resistor (R_{GS}) (k Ω)
275 ⁽⁹⁾	0.934 ⁽¹⁰⁾	8.53 ⁽¹¹⁾	1.5 ⁽¹²⁾	11.25 ⁽¹²⁾	20

Notes:

- 9) Obtained from the datasheet.
- 10) Obtained from measurements.
- 11) Obtained from the oscilloscope waveform.
- 12) Desired values.

Based on Equation (5), the required capacitance is 8.69 μ F. However, this value was calculated under the assumption of a worst-case scenario, so designers must consider the following factors:

- **Tolerance:** Tolerance can be reduced by placing more than one capacitor in parallel, rather than using a single capacitor.
- **DC bias:** The higher the voltage to withstand, the lower the capacitance. Larger SMD packages are better.
- **Dielectric:** The dielectric determines the capacitance variation due to the operating temperature.
- **Aging:** Consider aging, as the capacitance decreases at a constant rate over time for most ceramic capacitors. ⁽¹³⁾

Notes:

- 13) For simplification, again will not be considered in this example.

The chosen capacitor is 4.7 μ F with $\pm 10\%$ tolerance, 12.3% bias at 11.25V, and $\pm 15\%$ variation due to temperature (X7R dielectric). Under the worst-case scenario, this results in a capacitance of 3.15 μ F. Therefore, the design requires three capacitors in parallel for the capacitance to be equal to or greater than the calculated required capacitance. The voltage drop when using three 4.7 μ F capacitors is about 1V (see Figure 8).

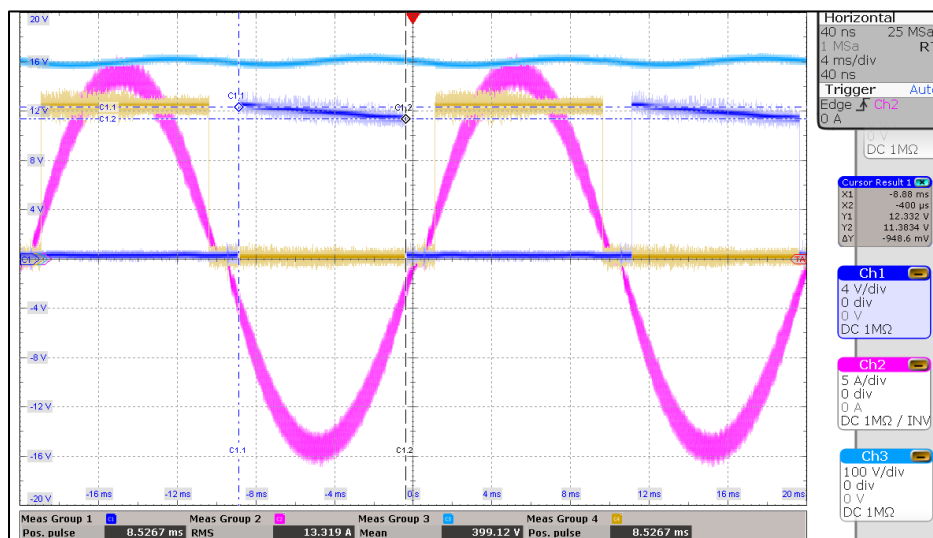


Figure 8: Waveforms with Three 4.7µF Capacitors (CH1: V_{GSQ1}, CH2: I_L, CH3: V_{Bus}, CH4: V_{GSQ2})

This voltage drop is very similar to its calculated value, which is 1.15V. Table 5 shows the relevant parameters.

Table 5: Parameters

Q1 Gate Charge Q _G (nC)	Quiescent Current (I _{VDDX_Q}) (mA)	Q1 On Time (t _{ON_Q1}) (ms)	HS Capacitor C _A (µF)	HS Voltage V _{DDA} (V)	Resistor GS R _{GS} (kΩ)
275 ⁽¹⁴⁾	0.934 ⁽¹⁵⁾	8.53 ⁽¹⁶⁾	11.53 ⁽¹⁵⁾	11.86 ⁽¹⁶⁾	20

Notes:

14) Obtained from the datasheet.

15) Obtained from measurements (the capacitor with bias correction).

16) Obtained from the oscilloscope waveform.

So far, a ferrite bead has been used in series with the bootstrap diode. However, a resistor is typically used instead to limit the diode's peak current when the capacitor is charged.

The peak current through the diode can be estimated with Equation (6):

$$I_{D_PK} = (V_{DDA} - V_{FW}) / R_{BTS} \quad (6)$$

Where V_{FW} is the diode's voltage drop, and R_{BTS} the resistance in series with the diode.

Figure 9 shows the difference between using a 5.6Ω resistor (denoted in blue) and a ferrite bead (denoted in gray).

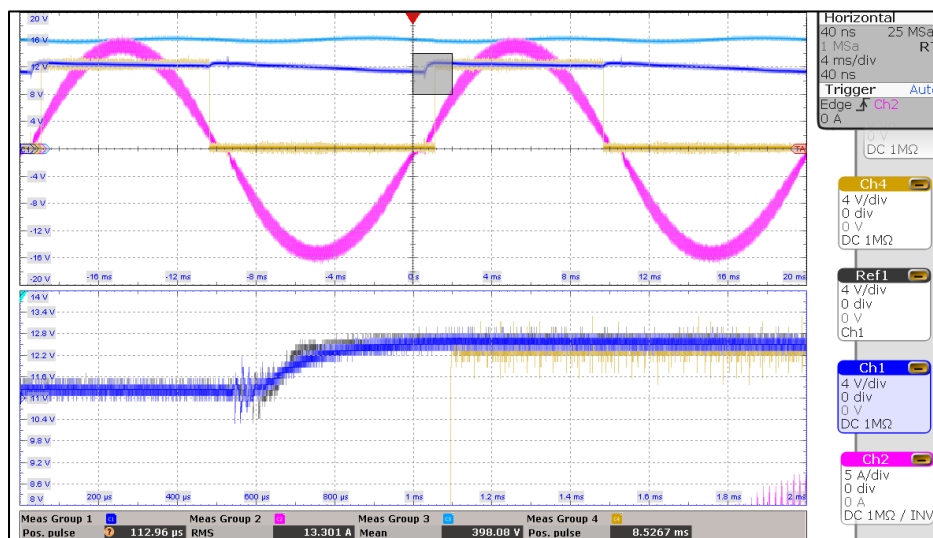


Figure 9: Waveforms when Adding a Resistor (CH1: $V_{CA_5.6\Omega}$, CH2: I_L , CH3: V_{BUS} , CH4: V_{GSQ2} , REF: $V_{CA_0\Omega}$)

The capacitor charge is smoother, but the overall waveform remains the same, which means we can conclude that the previous calculations are still valid.

Conclusion

When successfully driving the slow leg of a totem-pole converter, it is vital to select the proper half-bridge driver and ensure that the driver's capacitor is properly sized. If the slow leg isn't properly driven, a PFC totem-pole converter is inefficient and may even trigger protections erroneously.

Protections are typically triggered because the driver's high-side output is not the same as its input. Under these conditions, UVLO may occur. This means that the slow leg's high-side transistor stays on for an insufficient amount of time, leading to higher losses. To avoid triggering UVLO protection, designers must reduce the voltage ripple of the capacitor supplying the energy to charge the transistor's gate.

This article described how one of the main parameters responsible for the voltage ripple is the driver's quiescent current, which is needed to power its inner circuits and should be as low as possible. The other main component responsible for the voltage ripple is the capacitor. Designers must make the necessary calculations for both the capacitance and voltage to reduce the capacitor's voltage ripple.

The [MP18831](#) driver is an excellent choice in this application due to its very small quiescent current, and MPS offers a robust portfolio of [isolated gate drivers](#) to suit every application's needs.