An Equation-Driven Guide to Designing a CrM/DCM Boost PFC

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Introduction

Designing compact and efficient power factor correction (PFC) stages for low-power to mid-power applications often requires operating in critical conduction mode (CrM) or discontinuous conduction mode (DCM). These modes offer improved efficiency and simplified control at light loads, but require careful design to ensure correct valley detection and mode transitions across the entire input range and load range.

CrM/DCM boost PFC topology is a highly recommended solution for applications up to 200W. This topology remains a compelling choice for the 200W to 400W range, particularly when cost-effectiveness and light-load performance are primary design constraints. However, it is important to select the most suitable mode depending on the power level and system constraints.

This article presents a step-by-step methodology for designing a boost PFC stage that operates in CrM under worst-case conditions and falls back to discontinuous conduction mode at lighter loads (see Figure 1).

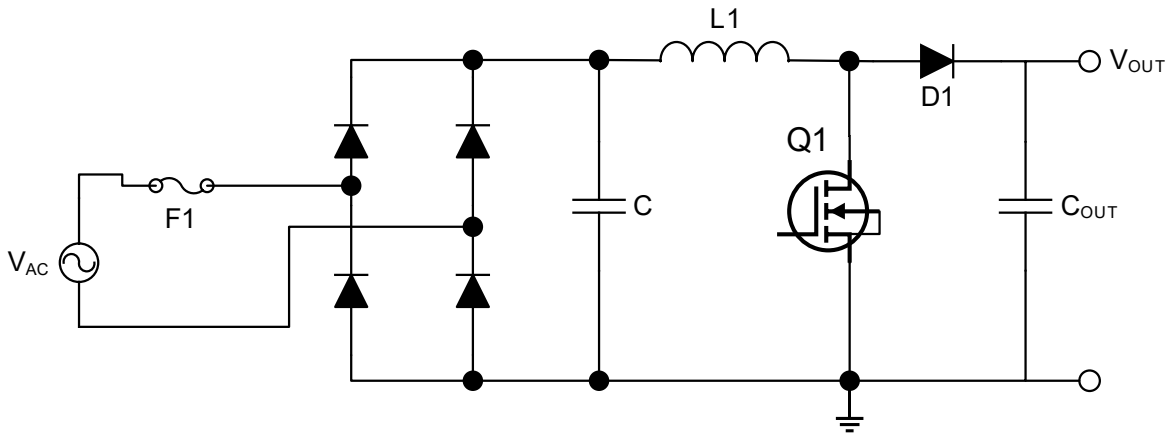

Figure 1: Boost Power Factor Correction Stage

The inductor is selected to achieve critical conduction at the minimum input voltage (V_{IN}) and a full load, ensuring proper zero-current switching. Key aspects such as variable frequency behavior, inductance, and peak current calculation are addressed in this article through a formula-driven approach.

Step 1: Define the Operating Parameters

An effective power design should include a clear set of specifications and consider the worst-case scenario. The operating parameters for a universal input PFC converter are the minimum AC RMS input voltage and maximum output power (P_{OUT_MAX}).

Table 1 shows the power converter specifications for a practical example, which will be applied to the following calculations in this article.

Table 1: Power Converter Specifications

Parameters	Value	Units
Input voltage (V_{IN}) range	85 to 265	V_{AC}
Output voltage (V_{OUT})	395	V_{DC}
Output power (P_{OUT})	150	W
Target efficiency	94	%
Minimum switching frequency (f_{SW})	70	kHz

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Based on Table 1, the minimum switching frequency (f_{SW}) is at the peak of the low AC line and at P_{OUT_MAX}. Figure 2 shows that the inductor current dependent on time (i_L (t)) follows the AC input voltage and its average value (I_{L_AVG}) in CrM.

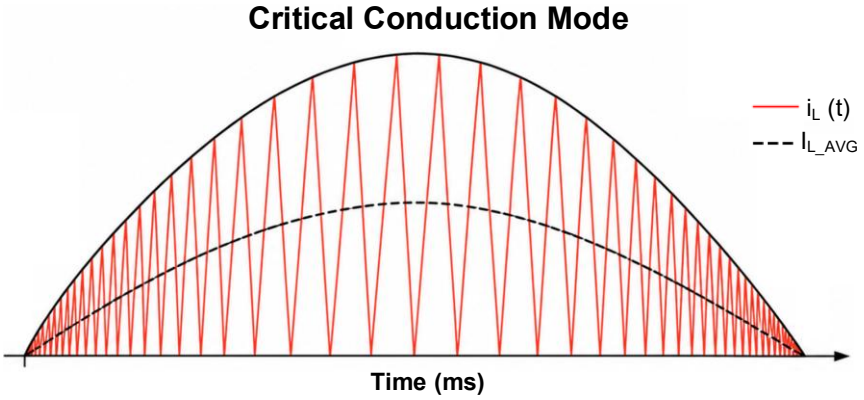

Figure 2: Inductor Current in CrM

The worst-case conditions can be determined using the power converter specifications from Table 1.

The maximum input power (P_{IN_MAX}) can be calculated with Equation (1):

$$P_{IN_MAX} = \frac{P_{OUT_MAX}}{\eta} \quad (1)$$

If P_{OUT_MAX} is 150W and η is 0.94 under the worst-case conditions, then P_{IN_MAX} is 159.57W.

The minimum peak AC voltage ($V_{IN_PK_MIN}$) can be calculated with Equation (2):

$$V_{IN_PK_MIN} = V_{AC_MIN} \times \sqrt{2} \quad (2)$$

If V_{AC_MIN} is 85V, then $V_{IN_PK_MIN}$ is 120.21V.

Step 2: Calculate the Inductance

The single most important component in this design is the boost inductor (L). Figure 3 shows an example of a power inductor for the power factor correction boost stage.

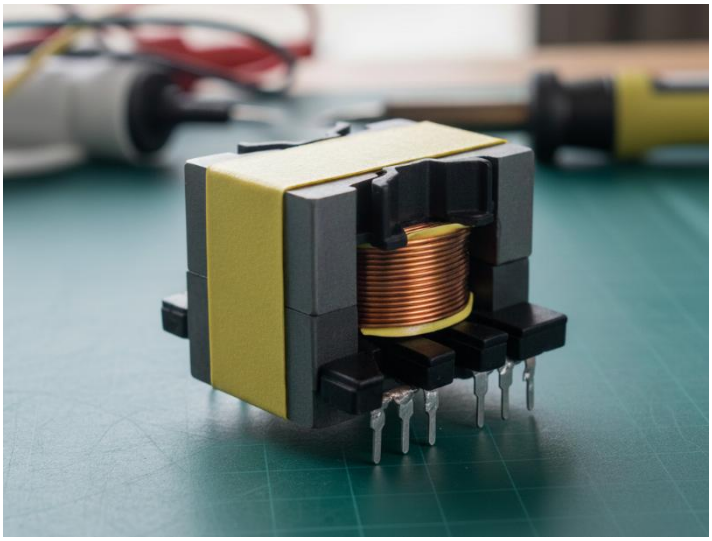

Figure 3: Power Inductor for PFC Boost Stage

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The boost inductance determines the energy storage per cycle and mode. The converter must be in CrM at the minimum AC input voltage under full loads. This ensures that the inductor has sufficient energy storage capability for all other operating conditions.

The required inductance (L) for CrM can be calculated with Equation (3):

$$L = \frac{(V_{IN\ PK\ MIN})^2 \times (V_{OUT} - V_{IN_PK_MIN})}{2 \times P_{IN_MAX} \times f_{SW_MIN} \times V_{OUT}} \quad (3)$$

Where $V_{IN_PK_MIN}$ is the peak input voltage at the minimum AC input voltage, V_{OUT} is the DC output voltage, P_{IN_MAX} is the input power at full load, and f_{SW_MIN} is the target minimum switching frequency.

The inductance based on Equation (3) and the power converter specifications provided in Table 1 is 450µH, as shown below.

$$L = \frac{(120.21V)^2 \times (395V - 120.21V)}{2 \times 159.57V \times 70000Hz \times 395V} = 450\mu H$$

At the highest current demand (low line peak at full loads), a 450µH inductor ensures that the current returns to 0A by the end of a 70kHz cycle. For any other current demand levels, the cycle completes faster, causing the part to operate in discontinuous conduction mode.

Step 3: Calculate the Maximum Component Stress

With a fixed inductance, the absolute maximum peak current tolerated by the MOSFET and diode at the peak of the low AC line voltage can be calculated. In CrM, the inductor current waveform is a triangle starting from 0A, where the peak current (I_{SW_PK}) is exactly twice the average input current. The average current at the peak of the sinusoid ($I_{IN_PK_AVG}$) can be calculated with Equation (4):

$$I_{IN_PK_AVG} = \frac{2 \times P_{IN_MAX}}{V_{IN_PK_MIN}} \quad (4)$$

The absolute peak switch current ($I_{SW_PK_MAX}$) can be calculated with Equation (5):

$$I_{SW_PK_MAX} = 2 \times I_{IN_PK_AVG} = \frac{4 \times P_{IN_MAX}}{V_{IN_PK_MIN}} \quad (5)$$

The calculation for the practical example is shown below:

$$I_{SW_PK_MAX} = \frac{4 \times 159.57W}{120.21V} \approx 5.31A$$

This means that the MOSFET (Q1) and boost diode (D1) must be rated to handle a repetitive peak current of at least 5.31A. The RMS current rating is lower, but this peak value determines the component's survivability.

Step 4: Analyze Variable Frequency Operation

A defining characteristic of a CrM/DCM PFC is its variable switching frequency (f_{SW}). f_{SW} changes dynamically throughout each half-cycle of the AC line, and is the lowest at the peak of the AC voltage (where the most power is processed) and highest near the zero-crossings.

The instantaneous f_{sw} (t) can be calculated with Equation (6):

$$f_{sw}(t) = \frac{v_{in}(t)^2 \times (V_{OUT} - v_{in}(t))}{2 \times L \times p(t) \times V_{OUT}} \quad (6)$$

Where v_{in} (t) is the instantaneous input voltage, and p (t) is the instantaneous input power.

v_{in} (t) can be calculated with Equation (7):

$$v_{in}(t) = V_{IN_PK} \times |\sin(\omega t)| \quad (7)$$

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p (t) can be calculated with Equation (8):

$$p(t) = P_{IN_PK} \times \sin(\omega t)^2 \quad (8)$$

Figure 4 shows f_{SW} across a half-line cycle, which has a characteristic U shape.

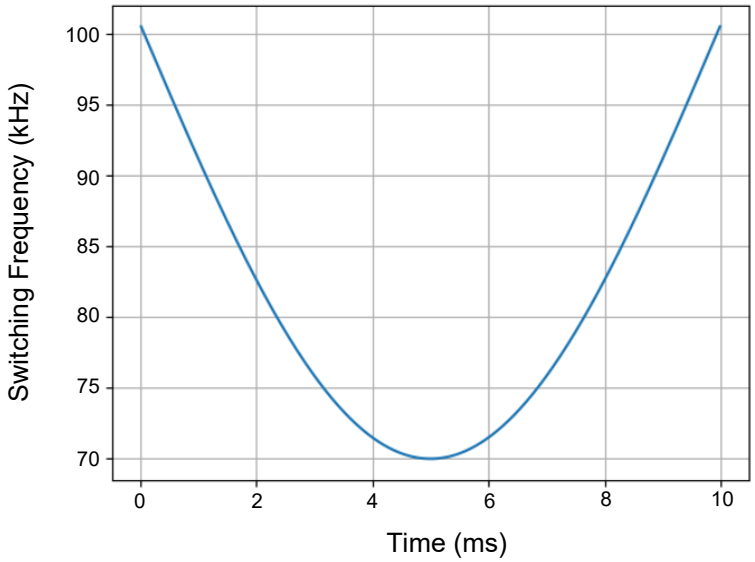

Figure 4: f_{SW} across a Half-Line Cycle

The designed minimum 70kHz switching frequency (f_{SW_MIN}) is lowest at the peak of the sinusoid, while the frequency rises dramatically near the zero-crossing. The controller IC must have a maximum frequency clamp to prevent excessively high-frequency operation, which would lead to high switching losses. A typical clamp is about 250kHz.

Step 5: Understanding the Control Loop and Zero-Current Detection (ZCD)

Compared to a fixed-frequency CCM design, a CrM/DCM PFC uses on-time control and zero-current detection (ZCD). The voltage loop sets the on-time command to regulate the output voltage (V_{OUT}), while the ZCD signal and the controller's internal timing logic determine when the next switching cycle can begin. As a result, f_{SW} depends on the on time (t_{ON}), the inductor demagnetization time, and any additional delay introduced by the controller.

On-Time Control

The main control loop adjusts the MOSFET's t_{ON}. A longer t_{ON} results in a higher peak current and more power delivered to the output. The controller's error amplifier (EA) compares V_{OUT} to a reference voltage and sets the required t_{ON} to keep V_{OUT} in regulation. The t_{ON} behavior across the AC line cycle depends on the control method implemented between constant-on-time (COT) control and variable-on-time (VOT) control.

- Constant-on-time (COT): In this standard approach, the controller maintains a fixed t_{ON} throughout a single mains half-cycle. The peak current (I_{PK}) can be calculated with Equation (9):

$$I_{PK} = \frac{v_{in}(t) \times t_{ON}}{L} \quad (9)$$

  The current naturally follows the sinusoidal shape of V_{IN}, providing inherent power factor correction. The voltage loop updates this constant value slowly across several cycles to regulate the output load.

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- Variable-on-time (VOT): To further minimize total harmonic distortion (THD), advanced controllers may modulate t_{ON} within the half-cycle. For example, intentionally extending t_{ON} near the V_{IN} zero-crossings can compensate for dead zones and crossover distortion, resulting in a purer sinusoidal input current.

Zero-Current Detection (ZCD)

Rather than use a fixed-frequency clock to start a new cycle, the controller waits for a signal from the ZCD circuit indicating that the inductor current (I_L) has dropped to 0A. An auxiliary winding is added to the boost inductor. When I_L decays and reaches 0A, the voltage on the main winding collapses, inducing a voltage swing in the auxiliary winding. This voltage swing is detected by the ZCD pin on the PFC controller, which immediately initiates the next MOSFET turn-on event.

Final Design

By calculating the required boost inductance and current on the semiconductor devices, a power factor correction boost converter design can be completed using the MP44020, a multi-mode CrM/DCM PFC controller. Table 2 shows the key design results for a 150W application.

Table 2: Design Results for a 150W Application

Parameters	Value	Units
Input voltage (V_{IN})	85 to 265	V_{AC}
Output voltage (V_{OUT})	395	V_{DC}
Output power (P_{OUT})	150	W
Magnetizing inductance	450	µH
Maximum peak current	5.31	A

The MP44020 provides simple and high-performance active PFC using minimal external components. To enhance system performance across all load conditions, f_{SW} is reduced at light loads via dead time (DT) extension technology, which improves efficiency and helps achieve very low standby power consumption. The MP44020 also achieves lower THD by implementing VOT control, a significant advantage over conventional COT methods.

Protections include over-voltage protection (OVP), over-current limit (OCL), brown-in (BI) and brown-out (BO), VCC voltage (V_{CC}) under-voltage lockout (UVLO), and over-temperature protection (OTP).

Due to the MP44020's high integration, the PFC stage requires only a few external components to function effectively. Figure 5 shows the PFC boost converter schematic using the MP44020.

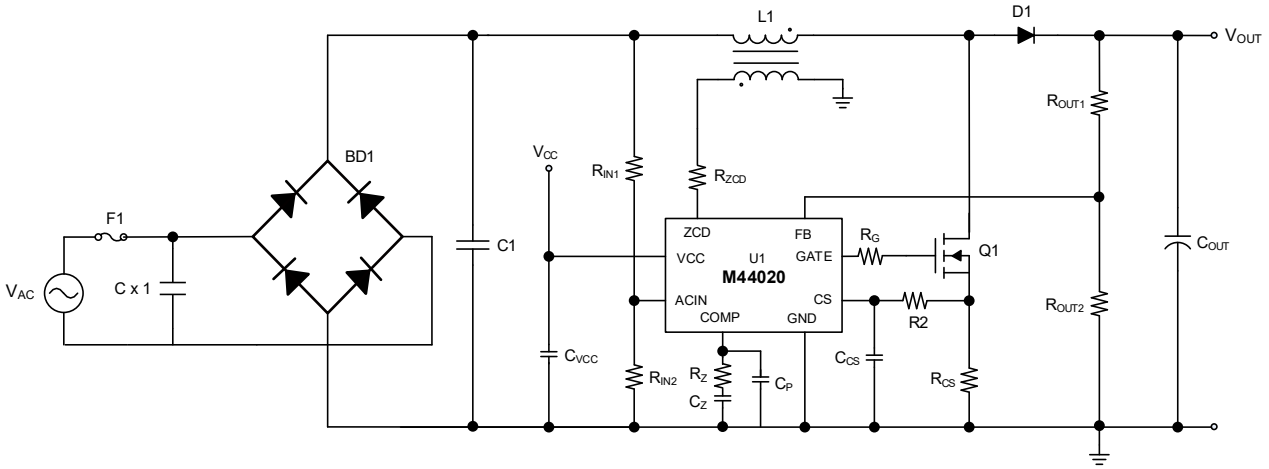

Figure 5: PFC Boost Converter Using the MP44020

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Conclusion

Implementing an active power factor correction (PFC) boost converter is a critical first stage for modern AC/DC power supplies. This ensures compliance with harmonic current standards and maximizes power quality. In particular, critical conduction mode (CrM) topology offers a cost-effective solution for applications up to about 400W.

By adhering to the design principles for CrM, such as selecting the appropriate boost inductor and managing the variable f_{SW}, engineers can design efficient and reliable PFC circuits. Moreover, a modern controller like the MP44020 significantly simplifies this task. The MP44020's variable-on-time (VOT) control scheme ensures low THD in addition to integrated protections and efficiency-boosting features for light-load conditions that achieve a robust and high-performance design.

For more solution options, explore MPS's selection of integrated, high-performance PFC controllers.

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