A 4-Step Guide to Selecting PFC Conduction Mode: CrM/DCM vs. CCM

By Rafael Collado, Supervisor at MPS

Introduction

The power factor correction (PFC) boost converter is the industry-standard topology for meeting harmonic current regulations such as IEC 61000-3-2. This circuit is essential in modern AC/DC power supplies, where it shapes the input current (I_{IN}) to follow the input voltage (V_{IN}) sinusoidal waveform, achieving a power factor near unity.

The key to successful PFC design lies in its operating mode. While three basic modes exist — continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrM) — the fundamental design choice is between a system built for CCM and a system optimized for CrM. A controller designed for CrM naturally operates in DCM at lighter loads, meaning CrM and DCM are often analyzed together as a single design path (CrM/DCM).

Selecting between CCM and CrM/DCM presents a fundamental tradeoff that directly impacts the converter's efficiency, physical size, cost, and EMI performance. Figure 1 shows the typical PFC boost converter schematic.

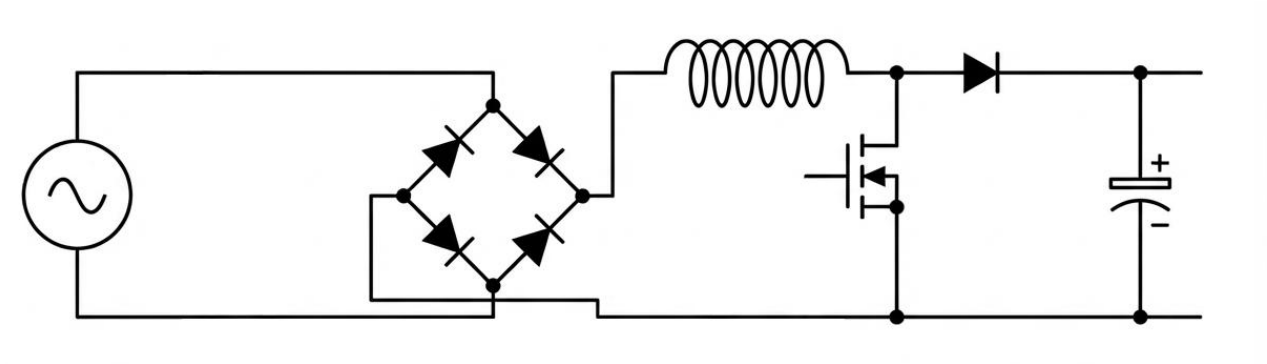

Figure 1: Typical PFC Boost Converter Schematic

Step 1: Identify the Primary Design Constraint

Before analyzing technical specs, the primary design constraint must be defined, as this informs the rest of the decision-making process. Common design constraints include:

- Maximum power density: Make the power supply as small and compact as possible.
- Minimum cost: Reducing the BOM is the most critical design factor.
- Maximum efficiency: Target a specific efficiency rating (e.g. 80 PLUS Titanium), where every fraction of a percentage point matters.
- EMI performance: The product is intended for a sensitive environment (e.g. medical, avionics, or high-fidelity audio), where passing strict EMI regulations is a major challenge.

Once the primary design constraint is identified, the next step is to analyze core tradeoffs.

Step 2: Analyze the Core Tradeoffs of the Selected Power Range

While the ideal conduction mode is heavily dependent on the application's power range, it is crucial to first understand the inductor current (I_L) behavior in each mode, as this determines all the other performance characteristics.

Figure 2 shows the fundamental difference between the I_L waveforms of the PFC boost modes (CCM and CrM) across a few switching cycles around the peak of the line half-cycle, where the average inductor current (I_{L_AVG}) is highest.

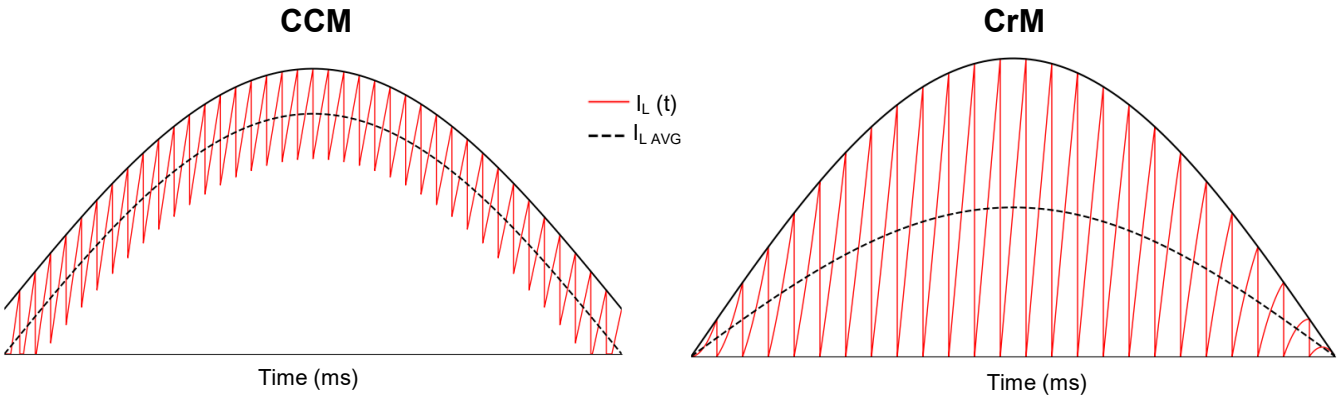

Figure 2: PFC Boost Modes

The I_L behaviors in CCM and CrM are described below:

- CCM: I_L always remains above 0A and has a relatively small triangular ripple current superimposed onto a large average inductor current (I_{L_AVG}).
- CrM: I_L is a series of triangles, where each cycle begins at 0A. The current ramps up to a peak, then ramps back down to 0A, at which point the next cycle immediately begins.

For selecting component stress and size, the peak switching current (I_{SW_PK}), required inductance (L_{PFC}), and dominant power losses must be calculated. These calculations are typically evaluated at the peak of the low-line AC input voltage (e.g. 85V_{AC}), which represents the worst-case scenario for the RMS inductor current (I_{L_RMS}) and peak inductor current (I_{L_PEAK}).

Peak Switching Current

I_{SW_PK} determines the required current rating of the MOSFET and diode. The baseline for comparison is the average input current at the sinusoid peak ($I_{IN\_PK\_AVG}$).

The CCM peak switching current ($I_{SW\_PK\_CCM}$) can be calculated with Equation (1):

$$I_{SW\_PK\_CCM} = I_{IN\_AVG} \times \left(1 + \frac{K_R}{2}\right) \quad (1)$$

Where I_{IN_AVG} is the average input current, and K_R is the ripple factor (typically between 0.2 and 0.4).

The CrM peak switching current ($I_{SW\_PK\_CRM}$) can be calculated with Equation (2):

$$I_{SW\_PK\_CRM} = 2 \times I_{IN\_AVG} \quad (2)$$

The peak current flowing through the switch and diode in CrM is about twice the peak current in CCM for the same input power (P_{IN}). This directly impacts conduction loss (I^2R).

Required Inductance

L_{PFC} determines the main magnetic component size. The required CCM inductance (L_{PFC_CCM}) can be calculated with Equation (3):

$$L_{PFC\_CCM} = \frac{V_{IN\_PK} \times D_{PK}}{K_R \times I_{IN\_AVG} \times f_{SW}} \quad (3)$$

Where D_{PK} is the duty cycle at the peak input voltage (V_{IN_PK}), and f_{SW} is the switching frequency.

The required CrM inductance (L_{PFC_CRM}) can be calculated with Equation (4):

$$L_{PFC\_CRM} = \frac{(V_{IN\_PK})^2 \times (V_{OUT} - V_{IN\_PK})}{2 \times P_{IN} \times f_{SW} \times V_{OUT}} \quad (4)$$

The required boost inductance depends strongly on the target ripple current and f_{SW} strategy. In many practical PFC designs, CCM uses a higher inductance to limit current ripple, while CrM can use a lower inductance at the expense of higher peak and RMS current.

Dominant Power Losses

Efficiency requires a tradeoff between conduction loss and switching loss. Table 1 shows the dominant power losses in CCM compared to CrM/DCM.

Table 1: Dominant Power Losses in CCM vs. CrM/DCM

Loss Type	Continuous Conduction Mode (CCM)	Critical Conduction Mode (CrM/DCM)
Conduction loss	Proportional to the RMS current in CCM ($I_{RMS\_CCM}^2$), which is lower due to the quasi-DC current.	Proportional to the RMS current in CrM ($\mathbf{I_{RMS\_CRM}^2}$), which is higher due to the triangular current shape.
Turn-on switching loss (P_{SW_ON})	$P_{SW\_ON} \approx V_{DS} \times I_{RR} \times f_{SW}$, which is very high. Where V_{DS} is the MOSFET's drain-to-source voltage. The high P_{SW_ON} is caused by the diode reverse recovery current (I_{RR}), and is the main source of loss and EMI.	$P_{SW\_ON} \approx 0W$, meaning it is negligible. It achieves zero-voltage switching (ZVS) or zero-current switching (ZCS) because the current is at 0A at turn-on.

Based on Table 1, CCM reduces conduction loss with the disadvantage of high switching loss, meanwhile CrM eliminates the worst switching losses with the disadvantage of higher conduction loss. This understanding can be applied to different power ranges.

For low-power applications below 200W, CrM/DCM is preferred. The high switching loss in CCM (from I_{RR}) is the dominant factor for power loss, which are eliminated in CrM. This leads to higher overall efficiency. For high-power applications exceeding 400W, CCM is preferred. The total current is high enough to result in massive conduction losses from the I_{RMS}^2 penalty in CrM. These $I_{RMS}^2 \times R_{DS(ON)}$ losses far outweigh the advantages of lower switching loss, meaning CCM is more efficient overall.

Step 3: Verification Using the Design Decision Map

A visual decision map can be used for verification by plotting the output power (P_{OUT}) against typical switching frequencies (see Figure 3).

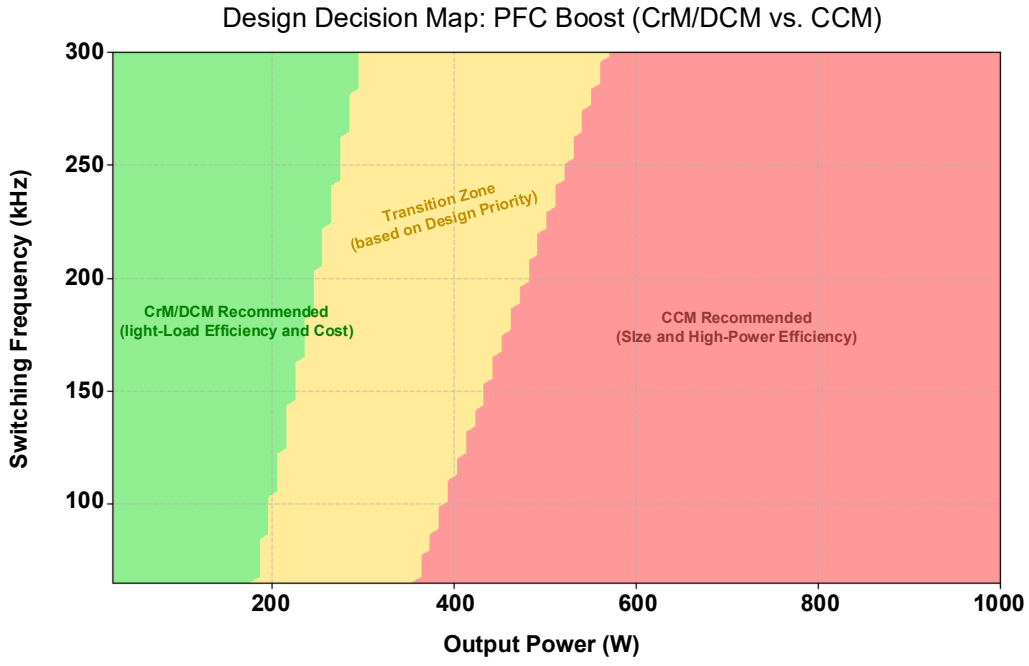

Figure 3: PFC Mode Design Decision Map (CrM/DCM vs. CCM)

The ideal operating regions for each mode are described below:

- CrM/DCM recommended (green region in Figure 3): As established in step 2 when analyzing the core tradeoffs, this region is ideal for CrM due to superior efficiency at light loads and lower cost.
- CCM recommended (red region in Figure 3): The lower conduction losses and smaller inductor size in CCM are ideal for high-power, high-density designs. Moreover, CCM offers advantages for conducted EMI and EMI filter designs due to its lower inductor current ripple and higher continuous input current.
- Transition zone (yellow region in Figure 3): The decision between selecting CrM/DCM and CCM depends on the primary design constraint identified in step 1.

Step 4: Select the Controller and Explore Alternatives

If a CrM/DCM controller is selected based on step 3, the design typically benefits from lower cost, good light-load efficiency, and reduced reverse-recovery-related switching stress.

If a CCM controller is selected based on step 3, using a fast-recovery or SiC boost diode can significantly reduce reverse-recovery-related losses and ease thermal design.

When selecting between a CrM/DCM and CCM controller, interleaved power factor correction (PFC) architecture provides an alternative design that achieves higher performance, low switching loss, and EMI benefits. Interleaved PFC architecture can significantly reduce input current ripple and RMS current in both the input and output capacitors. This improves thermal stress and can reduce filtering requirements while preserving many of the switching loss advantages associated with transition mode.

Final Design Checklist

By following the 4-step guide to selecting PFC conduction mode, the correct topology can be selected according to the design specifications. A final checklist is provided below, summarizing the rules of thumb to keep in mind:

1. If the power is below 200W, select CrM/DCM.
2. If the power exceeds 400W, select CCM (with a SiC diode).
3. If the power is between 200W and 400W, select the PFC conduction mode based on the primary design constraints defined in step 1:
    - Cost or EMI: CrM/DCM
    - Size: CCM
    - Performance: Interleaved CrM

Final Design

Designing the CrM/DCM PFC stage is based on the calculation of the boost inductance and the peak stress on key switching components. Table 2 shows the design results.

Table 2: Design Results

Parameters	Value	Units
Input voltage	90 to 265	V_{AC}
Output voltage	400	V
Output power	240	W
Boost inductance	170	µH
Maximum peak current	8.11	A
Switching frequency range	63 to 250	kHz

The MP44018A is employed for the power factor correction (PFC) stage as a multi-mode controller operating in CrM and DCM via the ZCD pin (see Figure 4). It is designed to provide high-performance active PFC with a minimal number of external components. This PFC controller's very low supply current achieves low standby power loss, with a typical no-load power consumption below 30mW. Light-load efficiency is improved through dead-time extension technology, which reduces the switching frequency under such conditions. Furthermore, the MP44018A achieves lower total harmonic distortion (THD) compared to conventional constant-on-time (COT) control by utilizing a variable-on-time control strategy while in DCM.

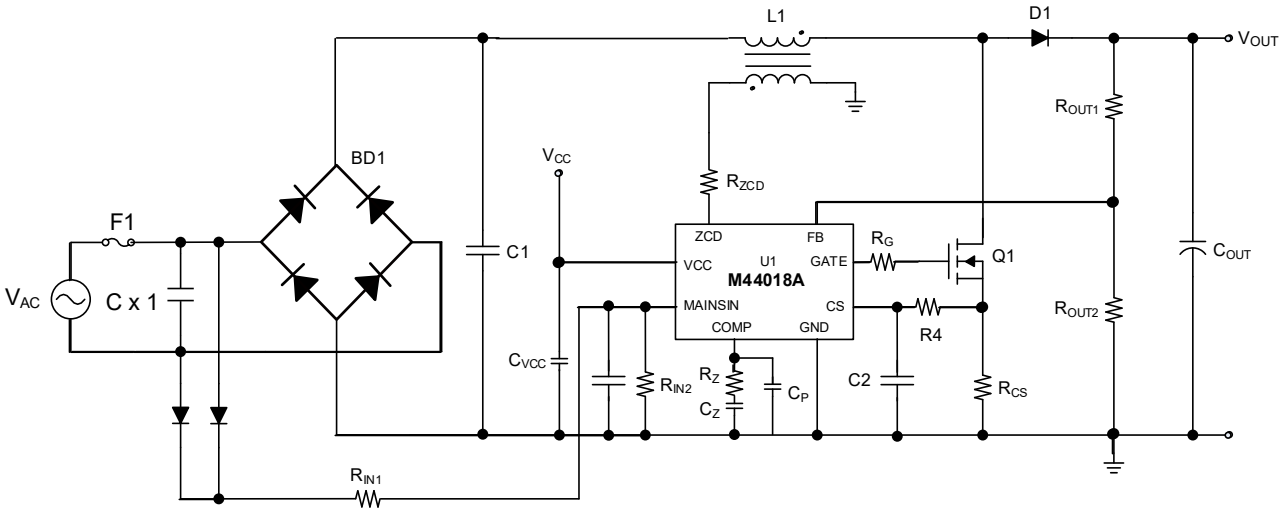

Figure 4: CrM/DCM PFC Boost Using the MP44018A

Figure 5 shows the measured input current harmonic spectrum at V_{IN} = 230V_{AC} and P_{OUT} = 240W in a compliance-oriented view of boost PFC performance. The red bars correspond to the harmonic content achieved by the implemented PFC solution with the MP44018A. The blue bars show the applicable IEC 61000-3-2 harmonic current limits for the target equipment class.

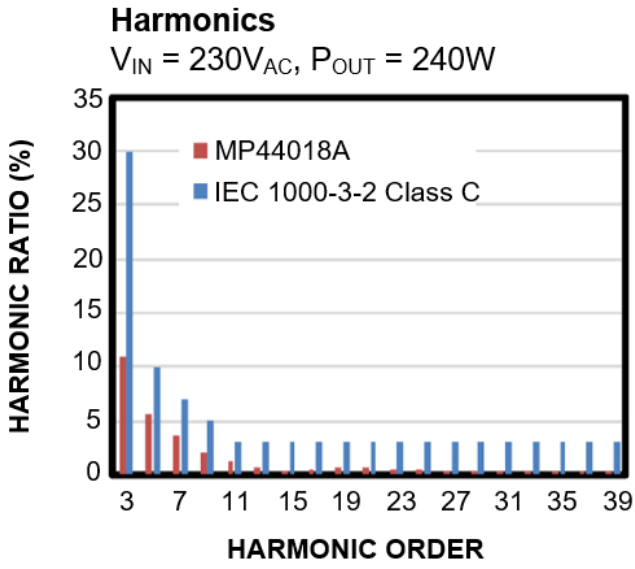

Figure 5: Harmonics Results Compared to IEC 1000-3-2 Class C

Conclusion

Implementing an active power factor correction (PFC) front-end is a critical requirement for modern AC/DC power supplies to ensure high efficiency and compliance with harmonic current regulations. This article demonstrated that selecting the proper conduction mode is foundational for PFC construction, directly impacting the converter's efficiency, physical size, cost, and EMI performance.

The 4-step guide to selecting PFC conduction mode provides a clear methodology for navigating these tradeoffs, beginning with the primary design constraint and culminating in an informed topology selection. A strategic approach to conduction mode selection helps optimize the final design to meet its specific application targets, whether that is maximum power density, minimum cost, or peak efficiency. For designs that follow the CrM/DCM path, a multi-mode controller such as the MP44018A can provide an effective solution for achieving strong light-load efficiency and harmonic performance with a low external component count.

A PFC front-end with a stable DC bus provides an ideal foundation for a high-efficiency secondary stage. Pairing this PFC front-end with a resonant LLC converter is a particularly effective strategy, enabling high-performance and high-density power solutions for markets ranging from consumer adapters to industrial supplies. For more solution options, explore MPS's selection of integrated, high-reliability PFC controllers.