Power Modules Make PCIe Accelerator Cards More Powerful

In the 5G era, everything is interconnected, and the quick developments in cloud computing are staggering. Major internet companies, cloud computing service providers, and communication service providers are demanding further improved server computing performance and data processing speed. The traditional CPU can no longer meet today's data processing requirements.

Although a hardware accelerator card with a GPU functioning as the core is still far in the future, there is a present-day solution to consider. The advantages of an accelerator card with FPGA as its core are obvious due to the system's configurability, flexibility, short development cycle, high parallel computing speed, and low latency.

In the future, the market for pluggable accelerator cards based on PCIe interfaces and FPGAs will drive incredible growth. For today's hardware, accelerators can still prove advantageous.

New Challenges

Behind this explosive growth is the continuous development of technology. Whether it is increasing computing speed or enhancing processor functions, there are no small challenges when designing power supplies (see Figure 1).

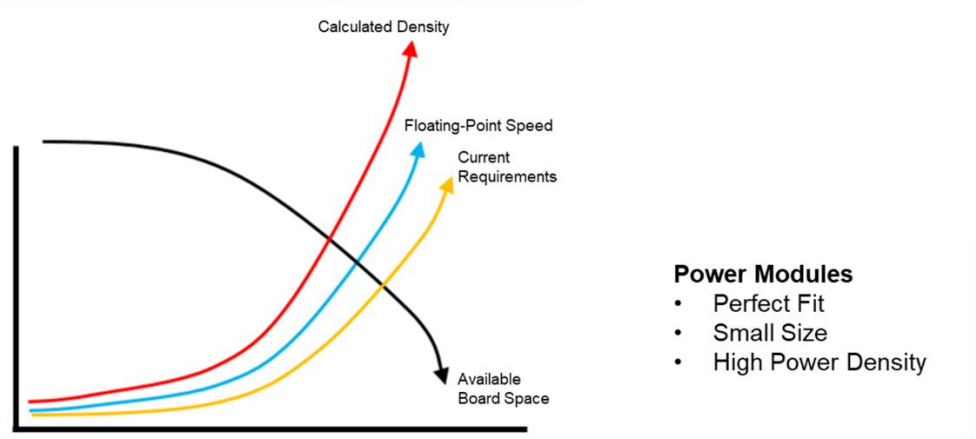

Figure 1: Development Trends for Accelerator Cards

Processors demand more current and power as the data processing bandwidth and requirements become more robust. The calculation density and floating-point speed requirements for accelerator cards is also becoming more difficult for the industry to meet.

The accelerator card slot is usually PCIe-standardized, so the size of the board is fixed. Due to increasing computing requirements, the size of the processor has grown, leaving little room for the power supply.

Under the new challenges, the power module stands out with its advantages of high integration, small size, and high power density, which perfectly meets the power supply requirements of the accelerator card.

New Requirements

At the same time that accelerator cards pose new challenges, FPGA power supply requirements have also become more and more complicated. Figure 2 shows the new requirements, described in detail below:

1. Output voltage offset: The output voltage deviation of the voltage rail must be less than ±3%, and sufficient margin should be left in the design. By optimizing the control loop to increase the bandwidth and ensure its stability, the decoupling capacitor should be applied and designed carefully.
2. Monotonic start: The start of all voltage rails must rise monotonically, and the design should avoid the output voltage from returning to its starting value.
3. Output voltage ripple: In steady state operation, the output voltage ripple of all voltage rails (except the analog voltage rail) must be at least 10mV.
4. Timing: FPGAs must meet specific timing requirements during start-up and shutdown.

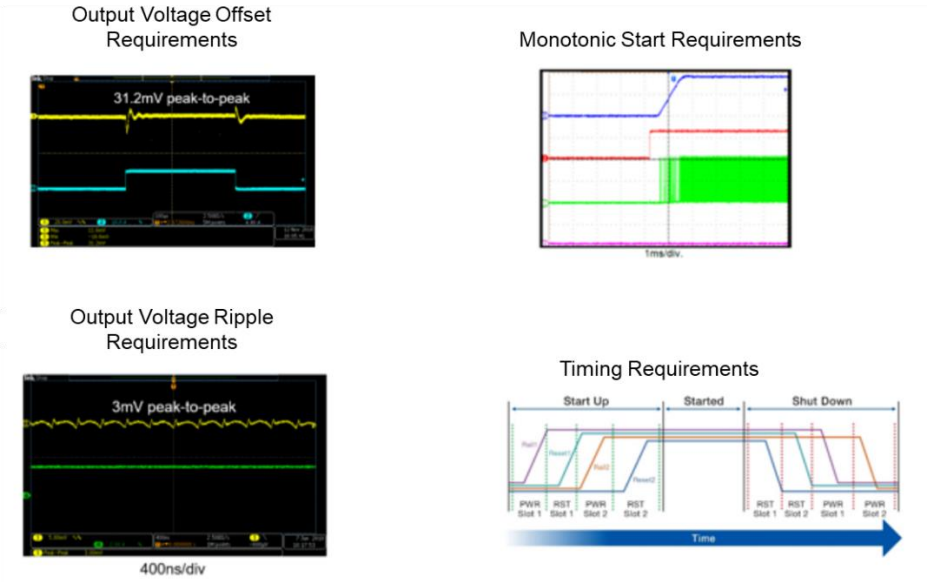

Figure 2: FPGA Power Supply Design Requirements

In response to the new challenges and requirements for power supplies, MPS's senior application engineers conducted a technical live broadcast specifically on the PCIe interface and FPGA pluggable acceleration cards, and introduced several MPS main power module products:

- The MPM3695-100 – A 100A power module that offers out-of-phase operation mode
- The MPM82504 – The first 4-channel, 25A module with an output that can be connected in parallel
- The MPM54304 – Offers four 3A output power modules with built-in start-up timing configurations

The live broadcast also introduced MPS's unique dual-input power supply solution, which can solve the need for high-power accelerator cards for dual input (PCIe power supply + aux power supply) (see Figure 3).

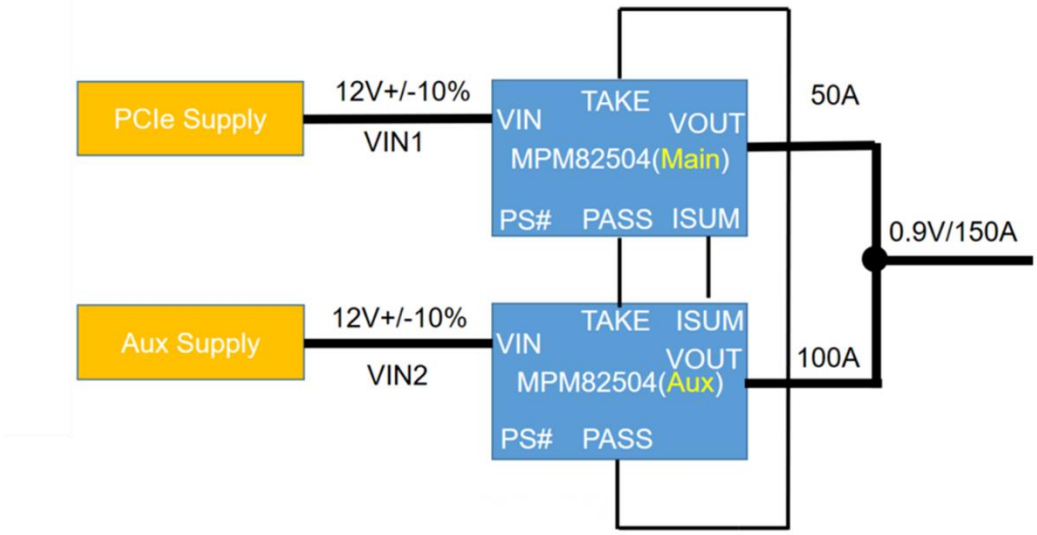

Figure 3: Dual-Input Power Supply Solution

With MPS's proprietary, multi-phase constant-on-time (MCOT), this solution can ensure current sharing of the power module in a dual-input environment, and work normally under single PCIe power supplies while the dual input also runs normally.