

## Power Path Management in Charger ICs

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A commonly used power path manage scheme, dynamic power path management (DPPM), is discussed in this article. The DPPM control loop adjusts the charge current dynamically based on the input source current capability and load current level to achieve a minimum charge time for a given source and system load. With DPPM, the system can obtain power immediately once the input source is applied, even with a deeply discharged battery. The system voltage regulation method is also discussed.

In mobile devices with a rechargeable battery, a charger IC is needed to charge the battery when an external power source is applied. The system load inside the mobile device could be provided by the battery, the input source, or both, depending on the connection of the battery and system load. A power path management scheme is needed to handle this kind of power source selection.

Dynamic power path management (DPPM) is the most popular scheme for power path management in mobile applications. The basic power stage structure for DPPM is shown in Figure 1.

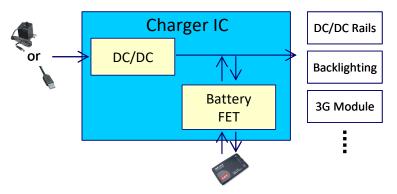


Figure 1: NVDC Power Path Management Structure

In the DPPM system, the system load is connected to the system bus  $(V_{SYS})$ .  $V_{SYS}$  can be powered from the battery through the battery FET, or from the input source through a DC/DC convertor or LDO. When the input source is not available, the battery FET is fully on, so the battery provides power to the system load.

When the input source is applied,  $V_{SYS}$  is regulated by the input DC/DC converter or LDO. Simultaneously,  $V_{SYS}$  provides a charge current to the battery through the battery FET. In this charging mode, priority is given to the system load, and the remaining power is used for charging. The charge current is adjusted dynamically based on input source capability and system load level, achieving a minimum charge time.

During the above charging process, if the system load is over the power capability of the input source,  $V_{SYS}$  will drop. Once  $V_{SYS}$  drops to a DPPM threshold, the DPPM control loop activates and reduces the charge current automatically to prevent  $V_{SYS}$  from dropping further. This process is also called DPPM mode.

In DPPM mode, if the charge current is reduced to zero, and the system load is still over the input power capability,  $V_{SYS}$  continues dropping. Once  $V_{SYS}$  drops below the battery voltage ( $V_{BAT}$ ) level, the battery provides power to  $V_{SYS}$  through the battery FET. This is called supplement mode. In supplement mode, the input source and battery provide power to the system simultaneously.

Before entering supplement mode, if the battery FET is in linear mode (not fully on, for example when  $V_{BAT} < V_{SYS\_MIN} + DV$ , or during a start-up transient), to ensure a smooth transition in and out of supplement mode, an ideal diode mode is preferred to control the battery FET, such as the one in the MP2624A.





During the ideal diode mode, the battery FET operates as an ideal diode. When the system voltage is 40mV below the battery voltage, the battery FET turns on and regulates the gate driver of the battery FET. The voltage drop ( $V_{DS}$ ) of the battery FET is about 20mV. As the discharge current increases, the battery FET obtains a stronger gate drive and smaller on-state resistance ( $R_{DS}$ ) until the battery FET is completely turned on. When the discharge current goes lower, the ideal diode loop generates a weaker gate drive and larger  $R_{DS(ON)}$  to keep a 20mV difference between the battery and system until the battery FET is turned off.

 $V_{SYS}$  regulation in DPPM mode can be flexible depending on the system requirement. If the front-end converter from the input to the system is an LDO,  $V_{SYS}$  can be set at a level to specially benefit the system requirement. For example,  $V_{SYS}$  is 4.65V for the <u>MP2661</u> and 5.0V for the <u>MP2660</u>.

If the front-end converter from the input to the system is a DC/DC converter, V<sub>SYS</sub> is usually set to follow the battery voltage to improve efficiency. This is commonly referred to as a narrow voltage DC (NVDC).

There are several advantages for DPPM control. First, the system gains power immediately once the input source is applied, regardless of whether the battery is depleted or not. Second, the charge current is adjusted dynamically based on the input source and system load to achieve a minimum charge time.

The limitation for DPPM control lies on the fact that it is complicated to ensure a smooth transition between the different operation modes. Usually, a V<sub>SYS</sub> loop, ideal diode loop, charge voltage, and charge current loop are required for battery FET control.

## Conclusion

With DPPM control, the system can obtain power as soon as the input source is applied, even if the battery is depleted. The charger IC with DPPM control can also optimize the charge current to fully utilize the input source current capability. Although the control for DPPM is complicated, DPPM is widely used in charger ICs that require power source selection, such as in MPS's MP2624A, MP2660, and so on.