



MPS Smart-Ramp Technology – A Solution to Voltage Change-Induced Audible Noise

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Audible noise in voltage regulator (VR) systems has been a problem for a very long time now. In the PC industry, the issue became more pronounced as the CPU became responsible for significant and repetitive voltage changes that induced noise through the VR. Those voltage changes, along with the physical properties of ceramic capacitors and the motherboard, produce an audible noise problem for the PC manufacturer with no good solutions so far. MPS had addressed the voltage change-induced audible noise issue by introducing MPS Smart-Ramp technology.

Ceramic capacitors are commonly used in the decoupling of the VR input and output stages because of their low cost and small size. The piezoelectric property of ceramic capacitors results in movement within the component body when a voltage change is induced. With a voltage change in one direction, the capacitor flexes one way, and then flexes in the opposite direction when the voltage change is reversed. When the voltage is changed repetitively within the audible frequency range, those ceramic capacitors follow a repetitive flexing. However, this alone is not enough to create noise. The flexing capacitors act like the voice coil in a speaker system. The voice coil moves the cone, and the cone actually creates the sound.

The motherboard is the cone in our speaker analogy. The motherboard is secured inside of a shell by several points, but there is typically enough unsecured board area to flex. When enough ceramic capacitors are flexing together, they can flex the motherboard quite easily within the shell vertically enough to create audible noise.

The final component needed to create audible noise in a VR is the repetitive voltage change. For many years now, the CPU has managed its own performance, frequency, thermals, and power consumption dynamically. A significant part of this management has been through adjusting the input voltage to the CPU. In high performance needs, the voltage is increased. When not needed for high performance, the voltage is reduced to reduce the leakage current within the CPU, thus saving power. These voltage changes are the area MPS has addressed to resolve audible noise in a PC.

Figure 1 shows an example of voltage identification (VID) changes from the CPU and the voltage response from the VR. A higher voltage is required for more performance, and then the voltage is lowered to reduce leakage current.

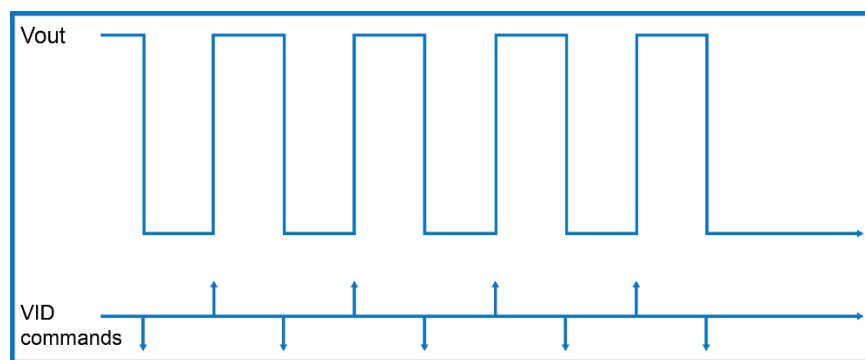


Figure 1: VID Changes from CPU and the VR Vout Voltage Response

The MPS Smart-Ramp audible noise reduction technology is shown in Figure 2. If the new VID from the CPU is both lower than the present VID and a voltage step greater than a value defined in a register X, then the beginning of the voltage ramp down is delayed for a duration defined in register Y. Figure 2 shows an example of a short delay which may be enough of a change to disrupt the flexing of the motherboard and thus reduce audible noise. The operation of the CPU and the commands coming from the CPU are unchanged.

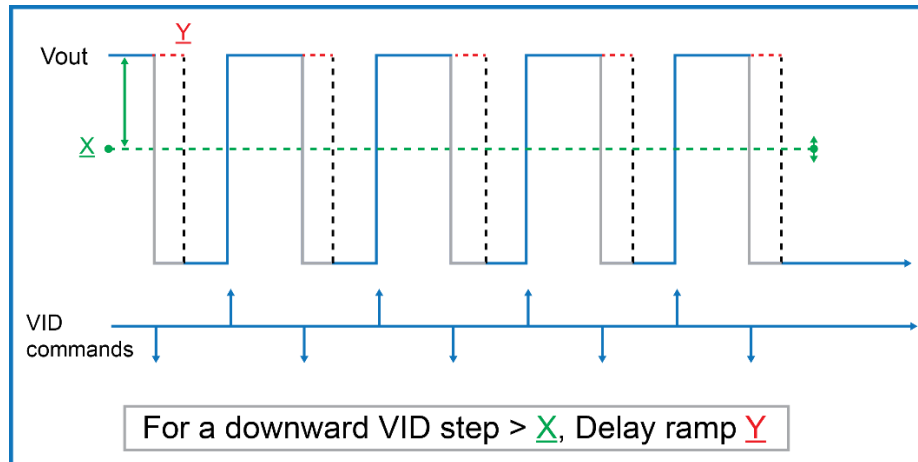


Figure 2: MPS Smart-Ramp Audible Noise Reduction Technology

Another implementation of the MPS solution is to extend the delay duration of the ramp down until the next VID command to a higher level has been received. When the repetitive voltage change has been removed completely, there is no more audible noise (see Figure 3).

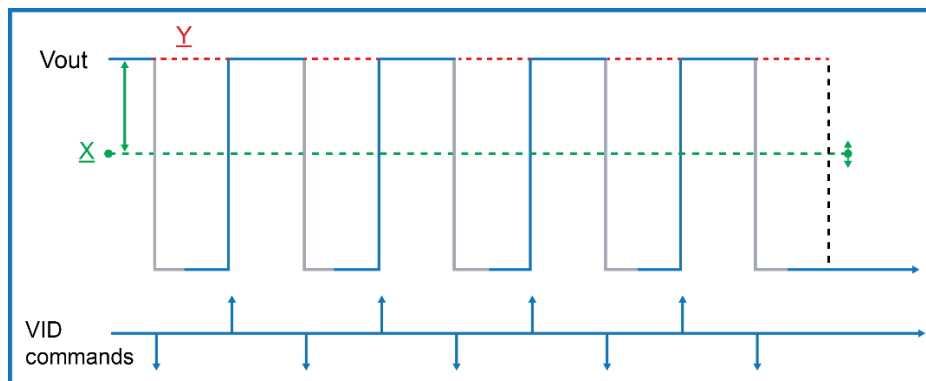


Figure 3: Voltage-Induced Audible Noise Removed

As previously stated, the advantage of voltage reduction to the CPU is a reduced leakage current, so the MPS Smart-Ramp solution impacts that power saving feature, albeit minimally. The greater power savings are in the CPU operating in lower C-states. The MPS Smart-Ramp technology does not interfere with the CPU's ability to enter its own power-saving C-states. The only power impact is an increased leakage current into the CPU during the short durations when the voltage would have been low if the voltage output had followed every VID command without delay.

However, changing the voltage also has a power cost which would need to be subtracted from the increased leakage power to understand the full power impact. When the VID is reduced, that charge is discarded (wasted) by the system by forcing that charge to ground. Then, additional power is required to re-charge the output when the VID is increased again. In some systems, the power cost of discharging and re-charging the output could be more than the leakage power seen when using the MPS Smart-Ramp audible noise reduction solution.

Additionally, it is only the short periods at the lower voltage during noise-causing events where the leakage current is higher. Once the repetitive voltage changes stop, there is one last delay before the MPS Smart-Ramp technology sets the voltage to the lower VID to save that leakage current during the intended long durations of CPU power-saving states.

The configurability of the MPS Smart-Ramp technology means customers have the option to be as conservative or aggressive as they desire. In one model, a customer may wait until a noise issue is discovered and then re-program the MPS VR controller through a BIOS change to activate and configure the feature to address their specific noise issue. Another method would be to proactively configure the VR controller for all but the smallest of VID changes coupled with a long delay setting. This would remove all voltage change-induced noise from the VR, but would obviously come with the potential for a larger power impact.

Conclusion

Voltage level changes to the processor input power are a necessary power-saving feature that will likely be used for many PC generations to come. When those changes result in audible noise in the PC, manufacturers have had few and expensive options to make their platforms viable for the marketplace. MPS Smart-Ramp audible noise reduction technology provides PC manufacturers with an effective option that is easily implemented.