Modern Efficiency is Powered by Digital Flexibility

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The efficiency requirements of power supplies have been evolving quickly in the recent decades, and are now very different from what was conventionally taught in textbooks. High efficiency at a certain rated condition is only the first step; a fully qualified and competitive power supply design must achieve high efficiency across the whole operating range.

The most popular efficiency-related regulations and agencies — such as Energy Star, 80 PLUS, EISA by U.S. Department of Energy, and the European Commission's ErP and CoC — all have clear but different requirements across a wide operating range, typically from 10% to 100% load, as well as no load condition.

At the same time, different applications also have various specifications at certain operating conditions based on the practical application demands. For example, PC power supplies may have particular efficiency specifications at a certain load condition below 10% of the rated power, depending on the sleep mode power consumption of each brands and each models. TV power supplies care most about the efficiency at standby mode, usually at 300mW input power, which is the upper limit of the power consumption when the TV is turned off by remote. Adapters usually have the strictest requirement on the no load power, even below 10mW sometimes, because most often adapters work without any load plugged in. With so many different specification, there is no way to cover all of them with a unified design, even for the same rated power.

Furthermore, any attempt on efficiency optimization inevitably has systematic influence on ripple, transient response, and audible noise, which are also very essential performances. As a result, today's fully qualified and competitive power supply products always need tremendous work on the design adjustment, parameter fine-tuning, and tradeoffs.

As the most popular topology combination for power supply designs, PFC with LLC has been commonly used for decades, by way of conventional analog control schemes. However, with new trends and growing efficiency requirements, today's design solutions must be much more flexible to support all kinds of system needs effectively.

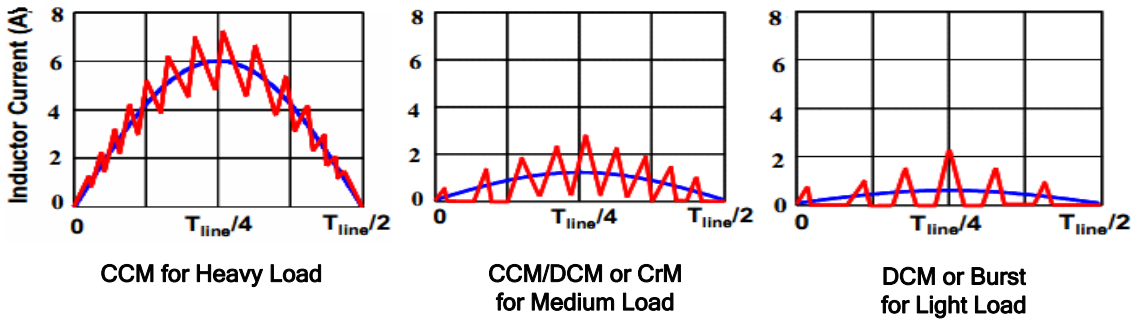

Figure 1: PFC Control Mode Options for Different Conditions

The PFC stage can benefit significantly from a multi-mode control scheme other than the conventional options of simple critical conduction mode (CrM) or continuous conduction mode (CCM).

CCM operation at heavy load conditions is able to minimize the peak current, reducing the size of the inductor and EMI filter (see Figure 1). Under medium-load conditions, a hybrid of CCM and discontinuous conduction mode (DCM) or CrM is able to create a balance between peak current amplitude and switching loss. Complete DCM or burst operation in light-load conditions lead to the best light-load efficiency by minimizing the switching loss. Therefore, a multi-mode control scheme with programmable switching frequency and a transition point for each operation mode helps fine-tune the efficiency performance curve.

On the LLC stage, the market is moving from relying on conventional voltage control mode to current control mode, which can offer better stability and transient response. In other words, new designs based on current control mode allow much more room for the loop adjustment amidst a range of application demands.

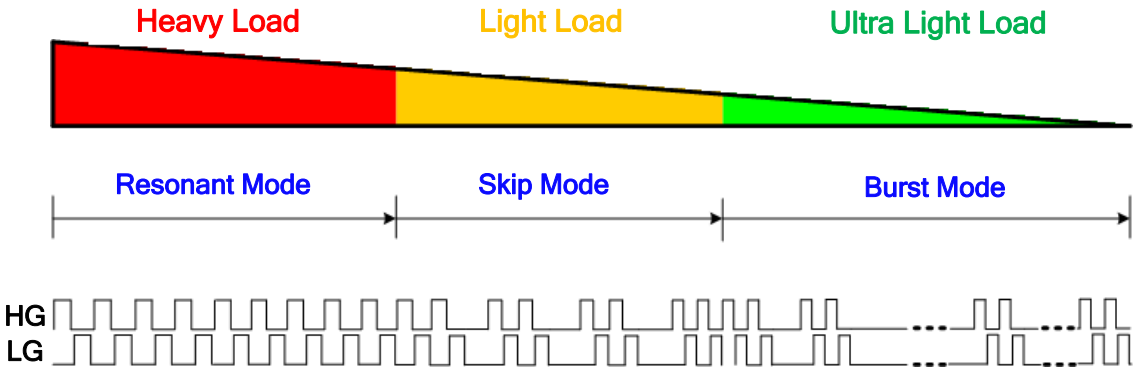

Figure 2: LLC Control Mode Options for Different Conditions

Similarly, the LLC control scheme is also developing multi-mode approaches. For example, Figure 2 shows three different operation modes, targeting efficiency and other performance optimizations for different load conditions. Under heavy-load conditions, the resonant mode achieves optimum efficiency with guaranteed zero-voltage switching and minimal RMS current.

In skip mode, a switch-idle period is implemented every couple of switching cycles. This reduces the switching loss and magnetic loss, while keeping the envelope frequency above the audible noise range. As the load reduces further, it can go into burst mode operation to minimize the switching loss.

There are also a number of settings that can be adjusted in burst operation, such as the envelope frequency limitation and soft on/off. All of these techniques can be adopted to help a solution meet all the requirements for efficiency, ripple, and audible noise. A solution that offers these features with programmable operating points and entry/exit thresholds is an ideal choice for modern power supply designs.

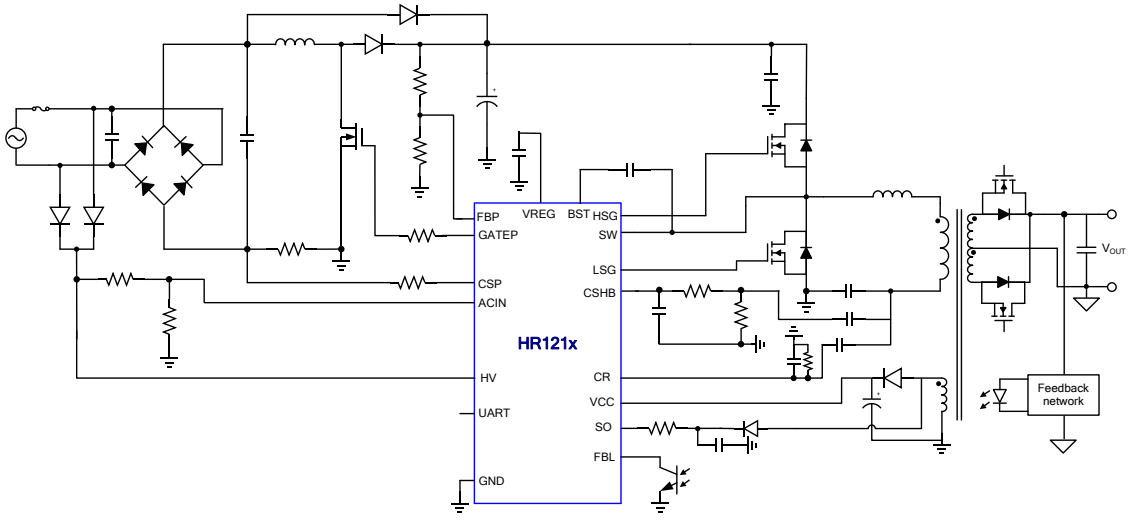

Figure 3: Typical Application Circuits of the HR121x

As MPS's second generation of digital PFC and LLC combo controllers, the HR121x family of parts has all the features and flexibility needed for a modern power supply design. Designing a power supply with an HR121x part allows the user to meet all kinds of efficiency requirements, as well as significantly improve the efficiency of R&D work. The HR121x family combines the merits of both analog and digital ICs, and is optimized comprehensively for PFC and LLC applications.

By integrating a high-voltage current source, an X capacitor discharge with safety certification, and a low-side driver for PFC and half-bridge driver for LLC, the external circuits remain simple and clean (see Figure 3). The fast response feature of analog circuit is also well retained, as all the functional blocks that are delay sensitive are still implemented by analog and mixed-signal design on the chip. As a result, the HR121x is able to achieve cycle-by-cycle current limitation, capacitive mode protection, and dead time adaptive adjusting just as effectively as any analog controller.

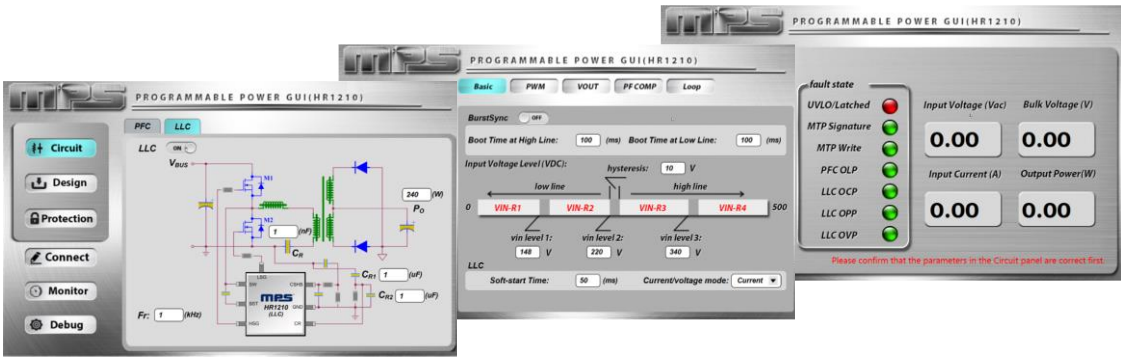

Figure 4: Graphic User Interface of the HR121x

On the other hand, the digital core and the multiple-time programmable (MTP) memory implemented on the chip enable great flexibility for the solution. The key parameters, switching characteristics at critical points, and transition thresholds among different operation modes can be programmed through a UART-based dongle and the user-friendly GUI (see Figure 4). In this way, it provides the flexibility to meet different efficiency requirements from a variety of applications, power ratings, and performance requirements.

The programmability of the HR121x can be even leveraged to a next level of usage, accelerating the whole R&D progress by automatically searching for the most optimized digital code. Through the UART communication, the HR121x can be linked to automatic test equipment systems.

By sweeping targeted registers with defined ranges and steps, all the test results for efficiency, ripple, power factor, etc. can be derived. Then, the most optimized code combinations can be determined by screening across the test data. This work can be done automatically with very few labor resources. Moreover, the judgement is made by real tested data, which is the most objective way to determine the best code design.

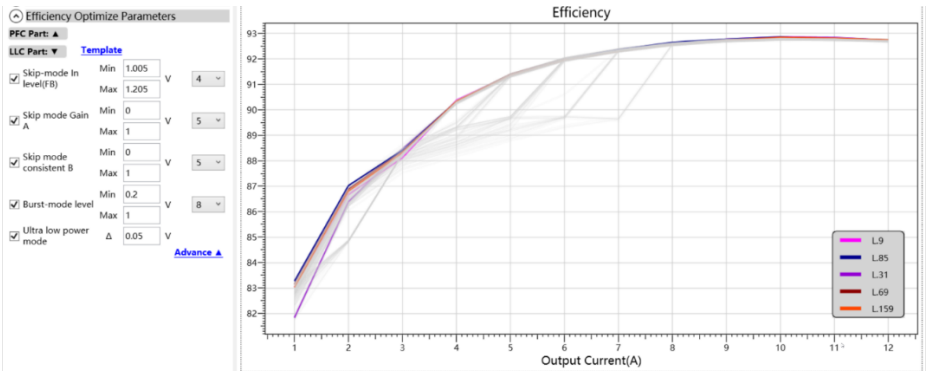

Figure 5: Automatic Efficiency Optimization Based on the HR121x

Figure 5 illustrates a LabVIEW-based automatic test system with the HR121x. In the demonstration, the PFC and LLC control mode related registers are swept, and all test results are collected as the total database. Then the top five are filtered out based on the recommendation of the most optimized digital code for the highest average efficiency. Similarly, the same database can be used to derive the most optimized digital code for the highest efficiency at certain load conditions, power factors above a certain specification, an output ripple below a certain specification, or any combination of these parameters.

Power supply designs are always about high efficiency, and it is more crucial than ever to have high efficiency in all aspects. Therefore, it is time to move to solutions like the HR121x, which not only has cutting-edge control schemes, but also provides the digital flexibility to be able to adapt and meet targets for a number of applications and operating conditions, and to achieve high efficiency for R&D work at the same time.