

# PCB Layout Design Guidelines for NB67x Series

## Application Note

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## **ABSTRACT**

This application note gives the details layout guidelines for a better and stable performance of NB669, NB670, NB671, NB671A, NB675, NB670L, NB671L, and NB675L.

### **LAYOUT FOR HIGH CURRENT INTERGRATED DC-DC CONVERTERS**

Other than the traditional converter that combines the controller with external power FETs, the NB67x series provides high power density fully integrated solutions for DC-DC converters, with output current around 6-12A in a small QFN3\*3 or QFN3\*4 package, this kind of integrated structure makes the converter much smaller and can also reduce the leakage parameters, contribute to higher switching frequency and also higher efficiency. However, the fully integration of the logic circuit and the power FETs makes these parts more noise sensitive once the PCB layout is not well designed, the high dv/dt noise will easily be coupled into logic circuit and leads to system instability, hence, a carefully designed PCB Layout is required to ensure a proper operation.

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## INTRODUCTION

### HOW IMPORTANT A LAYOUT IS TO THE HIGH CURRENT DC-DC CONVERTERS

The NB67x series is a family of fully integrated high frequency synchronous rectified step-down switch mode converters, these parts offers a very compact solution to achieve 6A-12A output current in a small QFN3\*3 or QFN3\*4 package . For these highly integrated DC-DC converters with high current and high switching frequency, a poor layout will degrade the performance of the converter, cause ground bounce, EMI problems, resistive power loss, high voltage stress on power FETs, poor line and load regulation and even system instability

### GENERAL DESIGN GUIDELINES

There are some general design guidelines for a proper layout.

The power trace (VIN, PGND, SW) should be placed short and wide with minimized loop area. That means, the input and output capacitor should be placed as close as possible to the IC, the input capacitor should be placed next to VIN and PGND, and the output capacitor should be placed in a way that its GND is close to the IC's PGND, also, the inductor should be placed close to the SW PIN and connect directly to the output capacitor.

The VCC decoupling capacitors should be placed close to VCC and AGND PIN, also the feedback resistor, usually named as R1 and R2, should be placed close to the IC and directly connect to FB and AGND. It is important that the signals do not conducts power, such as Feedback resistors, VCC decoupling capacitors should be connected to AGND (Analog ground), not PGND. Also the AGND should be well separated from PGND and finally single point connected to PGND

For a better thermal performance, at least two layers are required to form VIN and PGND trace, add several Vias with 10mil\_drill/20mil\_copper width close to the IN and GND pads to help on thermal dissipation. Four-layer layout is strongly recommended to achieve better thermal performance

The sensitive nodes like FB, VCC and AGND should be placed far from high dv/dt signals,( e.g SW,).

Keep the BST voltage path (path from BST to SW) as short as possible.

### CRITICAL DESIGN NOTES FOR THE PCB LAYOUT

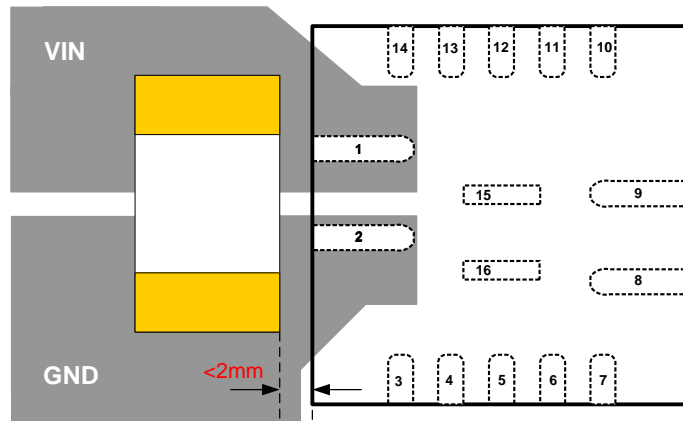
The above section describes some general layout recommendations that should be considered for an integrated converter, this section will focus on some specific layout suggestions that are critical for NB67x series. One should strictly follow these design notes for a better and strong performance. Since most of the parts have similar PIN out and structure, these parts are separated into two series in this section by packages as listed below:

- 1) The NB670/1 series, 6A part with QFN3\*3 Package including: NB669, NB670, NB671, NB671A, NB670L, NB671L
- 2) The NB675 series, 10A part with LDO in QFN3\*4 Package including: NB675, NB675L

**INPUT CAPACITOR**

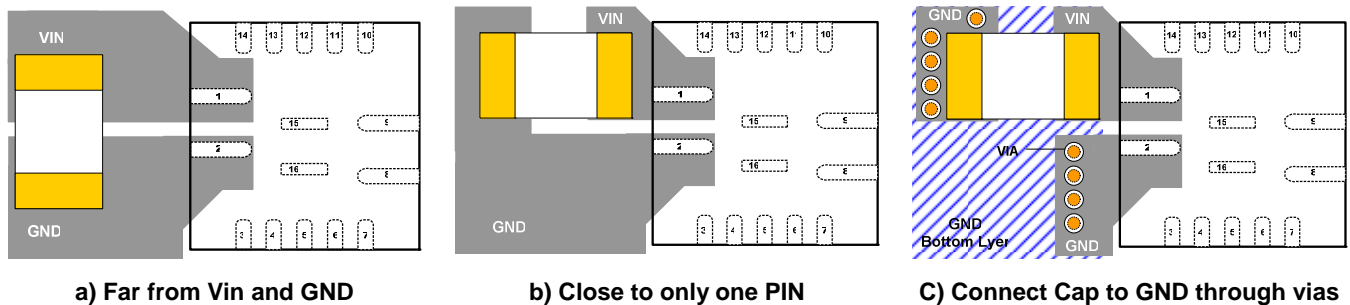
The input capacitors should be placed as close to the IN and PGND PINs as possible, these connections should be done with short, direct and wide traces. **It is strongly recommended to place the input cap <2mm distance from the Chip.**

Figure 1 describes the optimized input cap placement based on NB670/1 series



**Figure 1—Optimized and recommend input capacitor placement**

This input cap should be carefully placed to reduce the leakage inductance, the layout shown in Figure 2 are some common unqualified VIN capacitor layouts which will degrade the performance and stability.



**Figure 2, Unqualified Input Cap layout examples**

For a), the input cap is put far away from Vin and GND PIN, this will increase the leakage from Vin to HS MOS and also the leakage from LS MOS to GND, leading to higher voltage stress during switching periods

For b) The input cap is placed quite close to the VIN PIN, however, the trace from the ground side of the cap to the PGND PIN is not short enough.

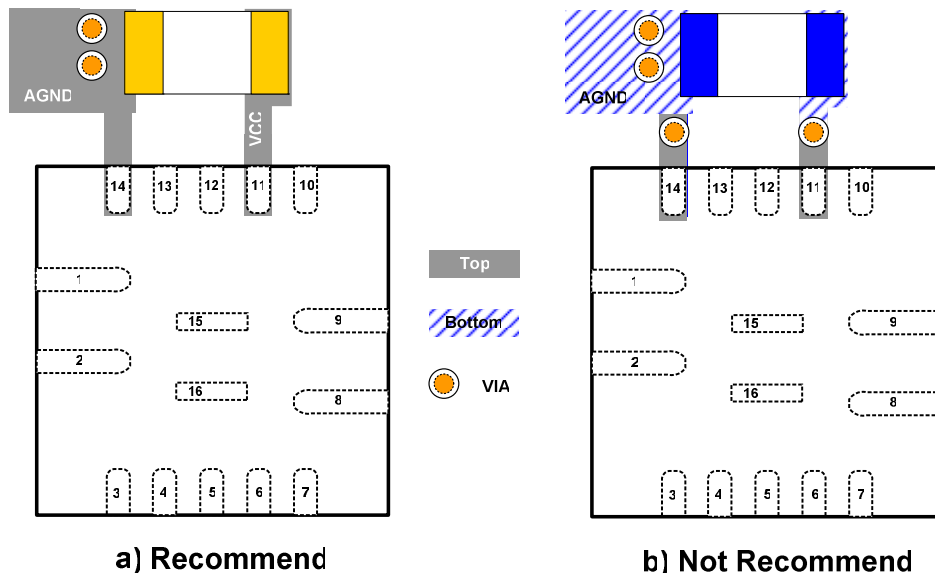
For c), the cap is also placed close enough to  $V_{in}$ , however, the trace from the Cap to the PGND PIN is more longer than b) as it was connected through vias, these vias will then make considerable leakage inductance to degrade the converter performance.

### VCC DECOUPLING CAPACITORS AND AGND TO PGND CONNECTION

The VCC is a 5V LDO output that powers internal logic and driver, VCC decoupling capacitors plays an important role in the DC-DC converters to make the logic circuits not noised coupled and then a stable operation. Hence,

- 1) The VCC cap is required to be placed as close to the VCC and AGND as possible, recommend to place the VCC cap <2mm distance from the Chip. It is highly recommended to put the VCC cap in the same layers with the converter so that less or no via is required since via will induce additional leakage inductance.
- 2) Besides the VCC cap place, the connection from AGND to PGND is recommend to set close to the cap by at least two vias, and this connection is the only bridge from AGND to PGND.

Figure 3 - a) describes the recommend VCC cap placement for based on NB670/1 series. For NB670/1 series, the VCC and AGND are on the same side, and the VCC cap could be easily placed next to VCC and AGND. Remember to put the VCC cap in the same layer to the part so that the leakage inductance from the Cap to VCC PIN could be minimized. Figure 3-b) has a VCC cap placed next to VCC and AGND PINs, however, put it in the back side and connect through vias with leakage inductance is not as good as the recommend way.



**Figure 3—VCC capacitor placement for NB670/1 series**

However, for larger current parts like NB675, NB675L, the VCC capacitor is difficult to be placed directly across the VCC to AGND like NB670/1 series since the VCC and AGND are at different side of the part. In this case:

- 1) Still, place the VCC cap in the same layer with the part.
- 2) The VCC cap should be placed next to the VCC PIN to prevent the noise coupled to VCC. Put this cap as close as possible to VCC Pin.
- 3) It is strongly recommended that the AGND is separated with PGND, the PGND includes high frequency noise because it is directly connected to the main power FETs loop. The single point connection from AGND to PGND is recommended to set close to the decoupling capacitor, and this connection is the only bridge from AGND to PGND. Remember do not connect the AGND to PGND at other places. Place at least 4 vias from VCC capacitor to AGND Pin, and 8 vias from capacitor to PGND layer for a smaller leakage inductance.
- 4) The AGND layer should be wide enough since the 2A VTT LDO current will flow through this trace, and this is also the reason why at least 4 vias is required for AGND
- 5) At least 4 layer PCB is recommended for an easy layout and also achieve better thermal performance.

Figure 4 describes the optimized VCC cap placement based on NB675 series.

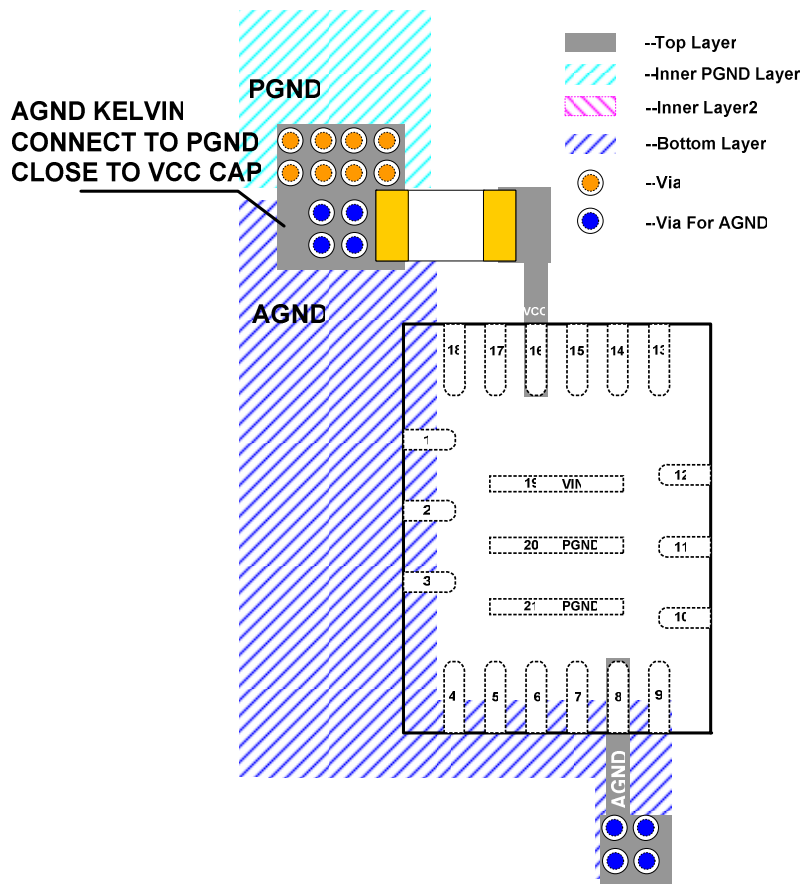


Figure 4—Recommend VCC capacitor placement for NB675 series

### ENHANCE INPUT POWER TRACE

The NB67x series provides high power density solutions for DC-DC converters with output current around 6-12A in a small QFN3\*3 or QFN3\*4 package, hence, a better thermal performance is expected to prevent the converter from a high temp rise. It is recommended that:

- 1) At least two layers is need for the VIN and PGND power trace, keep it short, direct and wide, and connect the two layers with vias. These vias are recommended to have 10mil\_drill/20mil\_copper width.
- 2) The vias placed under the part is quite important for the thermal dissipation, it also helps to reduce the leakage inductance to the power MOS. It is strongly recommended to place vias on the VIN and PGND PIN under the part. For NB670/1 series, place 1-2 vias each under VIN and PGND. For NB675, at least 3 vias each is recommended.
- 3) Also, for a better thermal dissipation, place as many vias as possible (>20) between the two input trace layers next to the VIN and PGND PIN around the input capacitors.

Figure 5 and 6 describe the recommend layer out for the enhanced VIN and PGND trace.



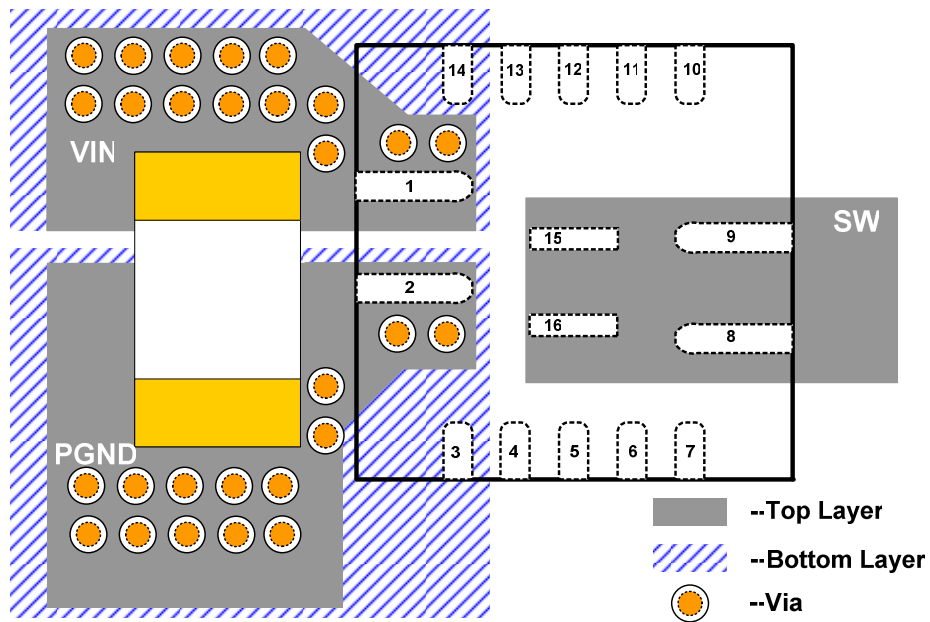


Figure 5—Recommend enhanced VIN and PGND Trace for NB670/1 series

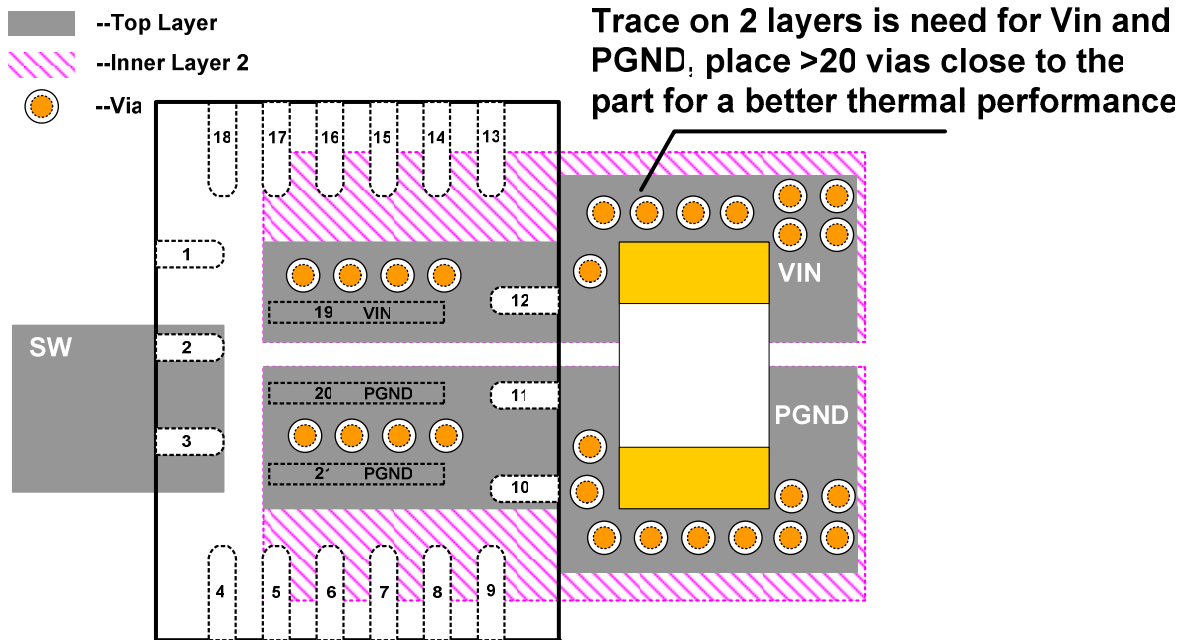


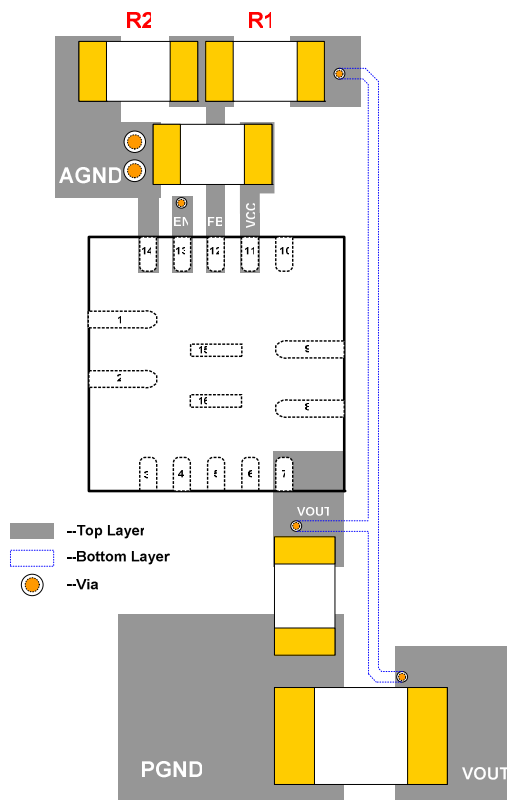
Figure 6—Recommend enhanced VIN and PGND Trace for NB675 series

## FEEDBACK RESISTORS

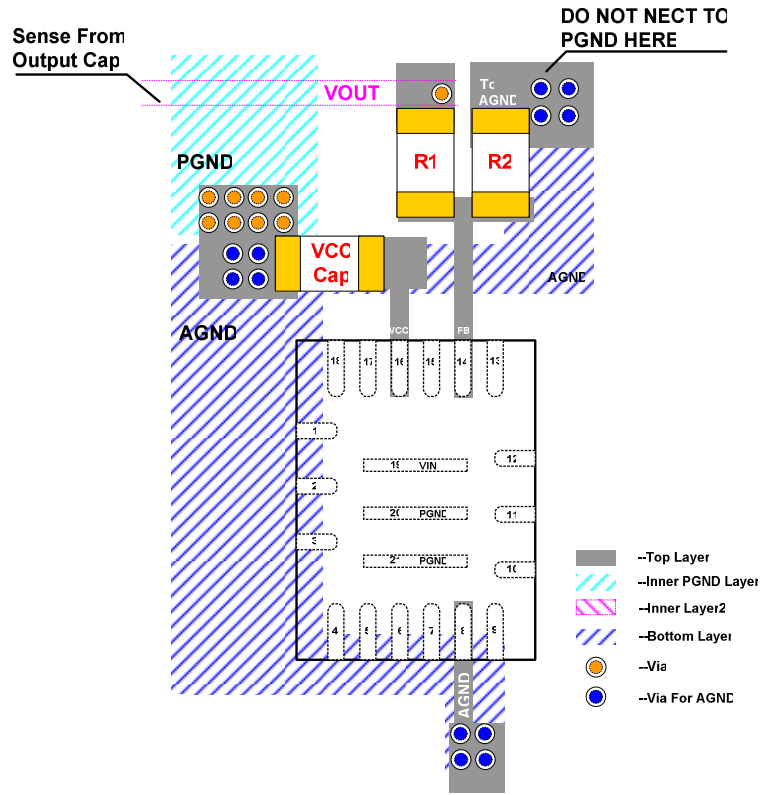
A poor feedback resistor placement will degrade system stability and also leads to poor line and load regulation. Several recommendations are listed below:

- 1) The feedback resistors should be placed next to the FB PIN to reduce the leakage inductance between the resistors and FB PIN. Do not connect FB to these resistors through vias
- 2) The down side resistor, usually named as R2, need to be connected to AGND, not PGND
- 3) The up resistor R1 should be connect to the output cap where you want the  $V_o$  to be at your setting

Figure 7 describes the optimized VCC cap placement for NB671 and NB675 series



a) Recommend NB671 series Feedback resistors placement



b) Recommend NB675 series Feedback resistors placement

Figure 7—Recommend feedback resistors placement

## RECOMMEND PCB LAYOUT

Based on above section, the map of PCB layout with all the design noted included is shown below. We recommend to use at least 4 layer PCB for these parts. The layer structure could be as follow:

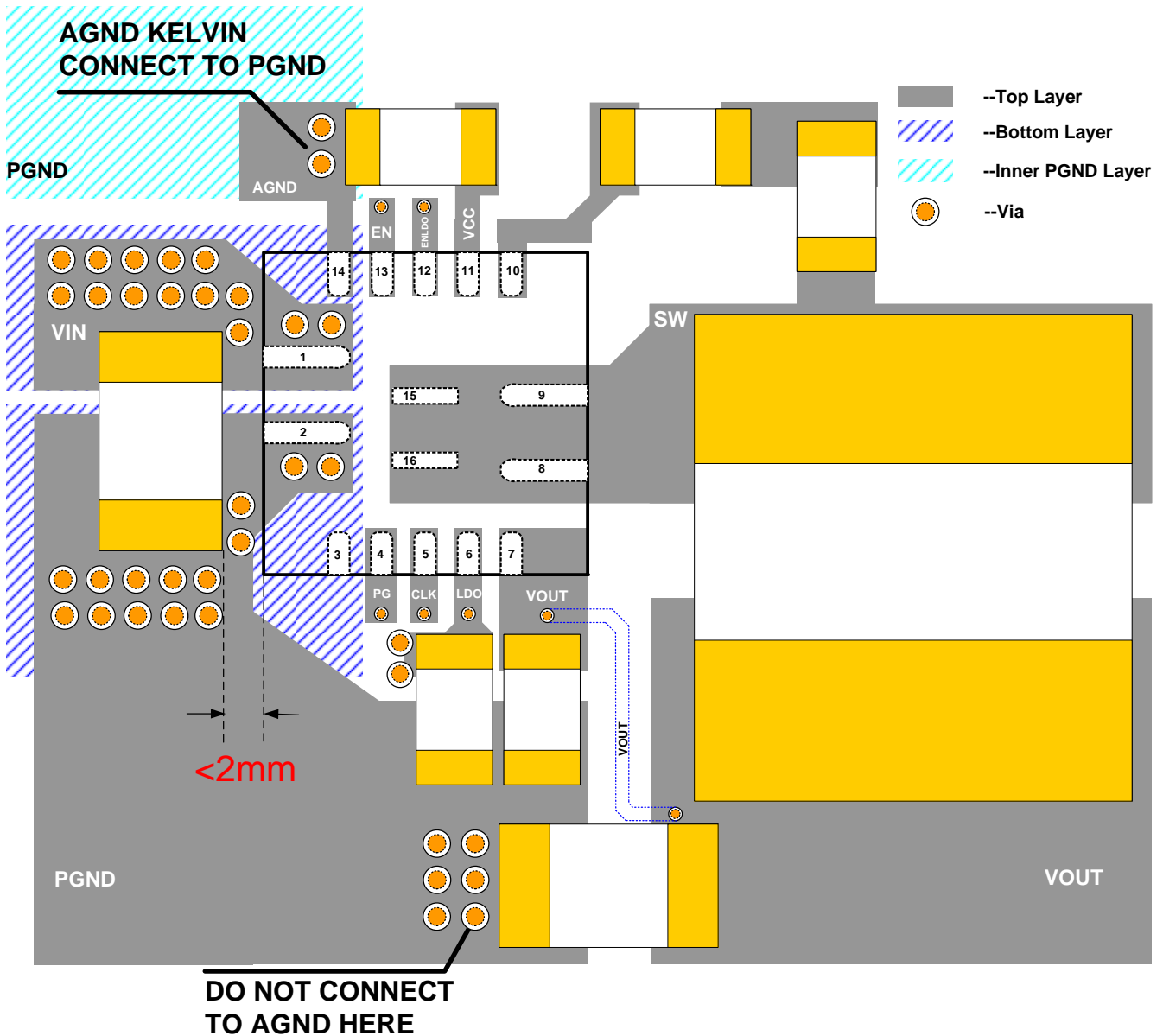
### NB669, NB670 AND NB670L

Top Layer — Vin, PGND, SW, Vout, BST layer.

Inner Layer1 — PGND Layer, only PGND here.

Inner Layer2 — Analog Signal layer, such as PG, EN, ENLDO,CLK

Bottom Layer — Vin, PGND



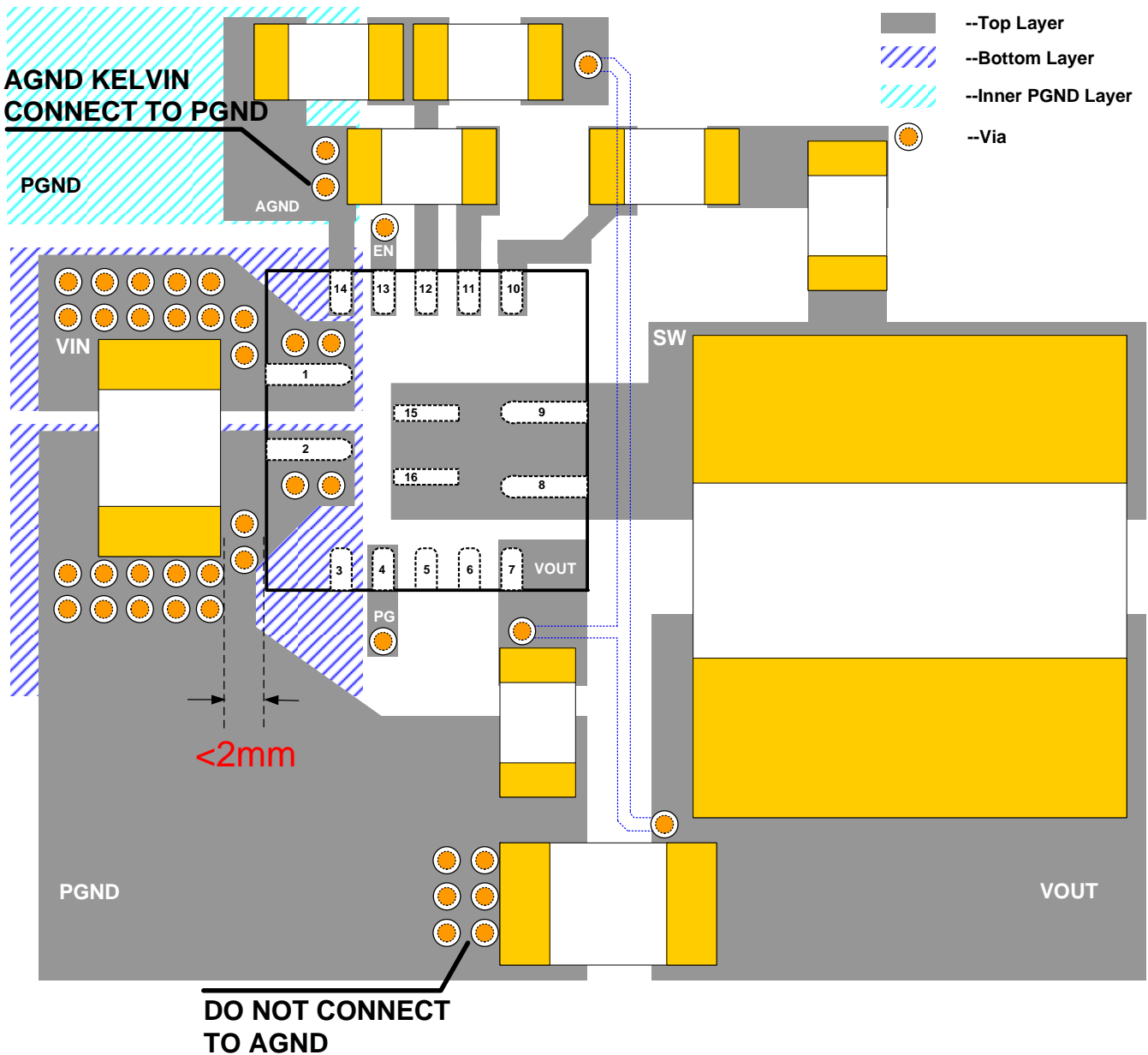
**NB671, NB671A AND NB671L**

Top Layer — Vin, PGND, SW, Vout, BST layer.

Inner Layer1 — PGND Layer, only PGND here.

Inner Layer2 — Analog Signal layer, such as PG,EN

Bottom Layer — Vin, PGND, some other signal layer



**NB675, NB675L**

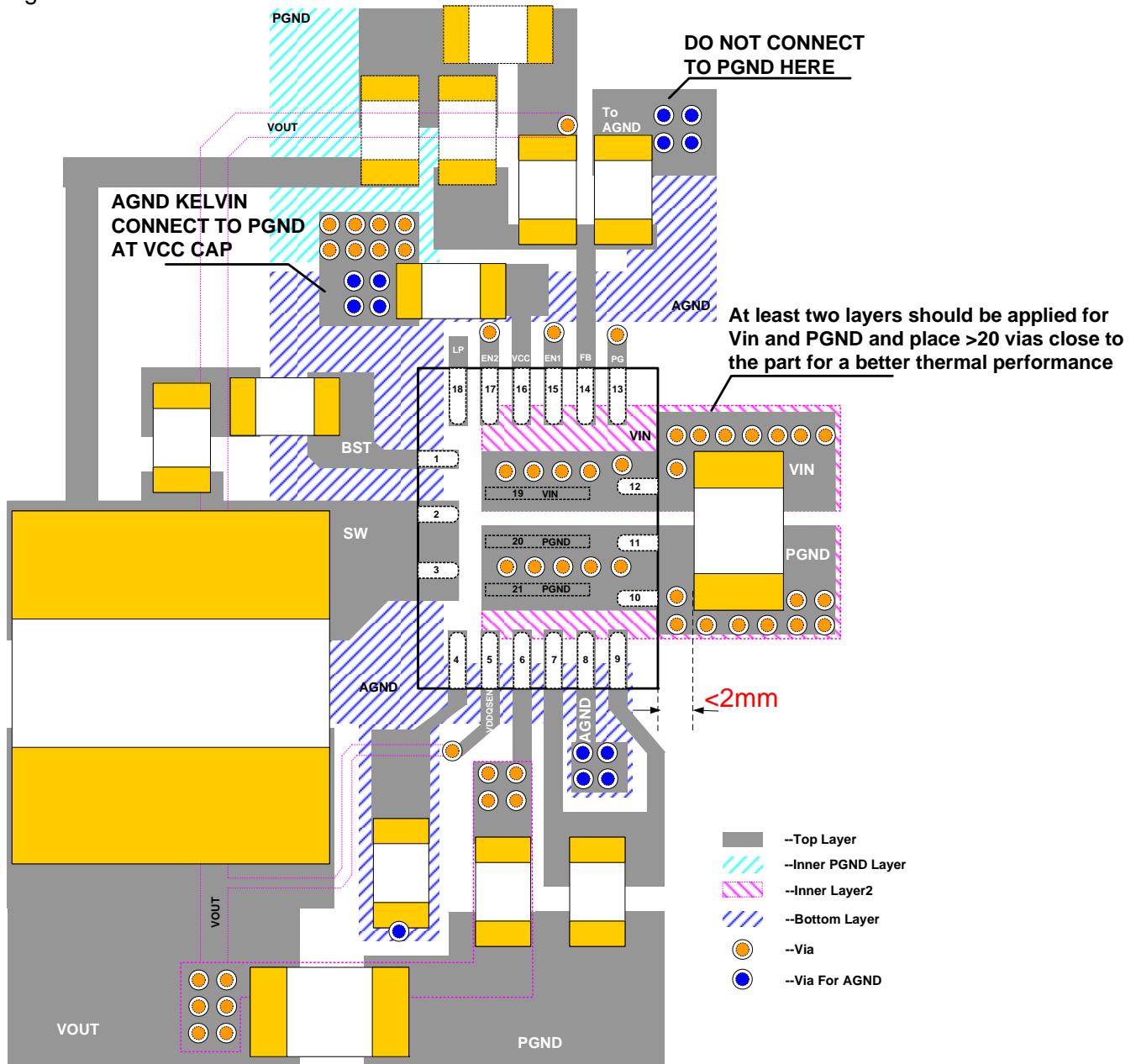
Top Layer — Vin, PGND, SW, Vout layer.

Inner Layer1 — PGND Layer, only PGND here.

Inner Layer2 — Vin, PGND, VDDQsense, VINLDO

Bottom layer — AGND, PGND ,VTT,VTTsense

Note: it is recommended to connect VTT Cap to PGND for a better noise immunity since it will conducts high current



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