Designing a Stable COT Converter for a Desired Load and Line Regulation

Application Note

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ABSTRACT

This application note discusses the relationship between stability and the ramp added to the feedback pin for MPS's Constant-On-Time (COT) control. It also describes how the ramp influences the load and line regulation, and discusses ramp designs that both optimize stability and the load and line regulation.

Getting a Desired Load and Line Regulation Based on FB Ramp Compensation

COT control operates without the need for traditional complicated loop design and has a fast transient response. To realize stability, add a ramp to the FB pin with an appropriate downward slope; the FB ramp stems either from the ESR of the output capacitor, or from the external RC compensation shown in dashed lines in Figure 1. The ramp provides a value of inequality between the average FB value and V_{REF}, and varies with changes to the input line or load. The ramp must be large enough to eliminate jitter even at the sub-harmonic level, though not so large that the load and line regulation degrade.

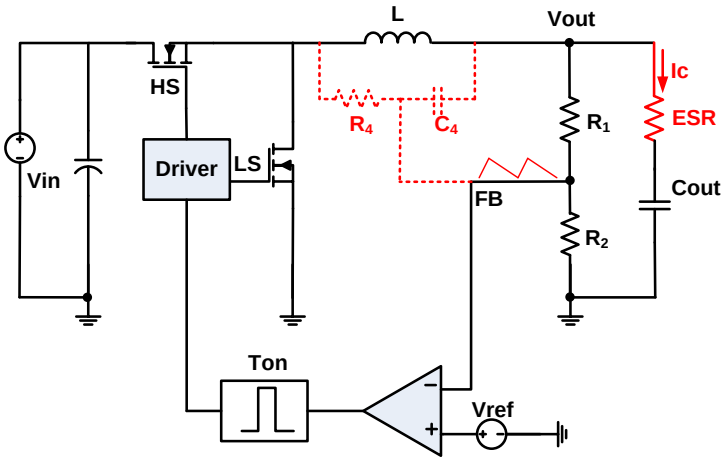

Figure 1: Circuit Diagram of COT Control

This application note describes how the FB ramp affects the load and line, and also provides a solution for optimal ramp design.

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INTRODUCTION

COT Control Introduction

Unlike traditional voltage- or current-mode control, COT control provides a way to eliminate the compensation loop. COT control eliminates the error amplifier and produces a PWM signal with a fixed ON time every time the FB falls below V_{REF}. If during the time where V_{FB} <V_{REF} is monotonic or in phase with the inductor ripple, then the system can operate at a fixed frequency based on the t_{on} setting. One easy and popular way to sense the inductor current is to use a output capacitor with an appropriate ESR value so the ESR×ΔI_L (inductor current ripple) dominates the V_{OUT} ripple, which then transfers to FB through the feedback resistors. FB turns on with a fixed ON time immediately when V_{OUT} falls and remains OFF while V_{FB}>V_{REF} this kind of control produces a fast transient without delays from the compensation loop and internal clock.

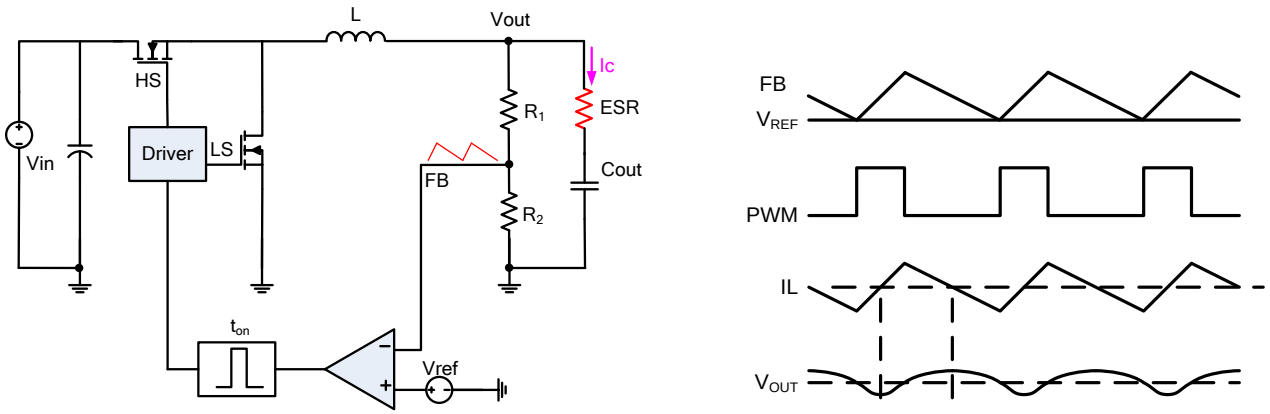

Figure 2: COT Buck Circuit Diagram and Operational Signal Diagram

Relationship between FB Ramp and Jitter

COT control depends on the ramp on FB crossing V_{REF} to stabilize the system, so the ramp on FB should be large enough to reduce the jitter induced by the FB noise. Figure 3 shows jitter reduction with COT control. The noise on the downward V_{FB} slope affects the time before the high-side PWM turns on, where a large ramp slope leads to smaller jitter.

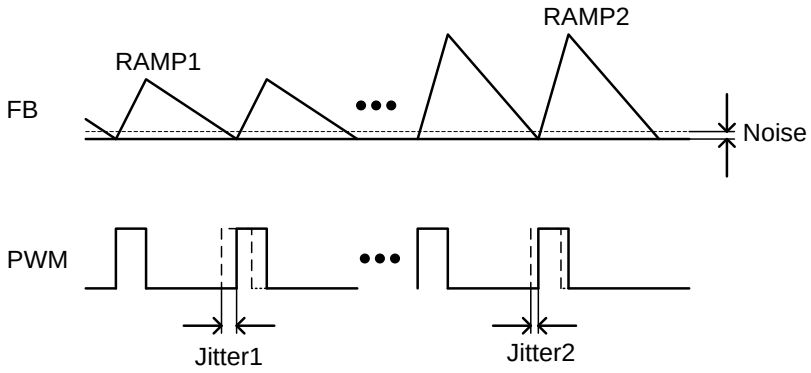

Figure 3: Ramp Slope and Jitter Performance

One major factor that affects jitter and stability is the downward slope when the FB ramp crosses V_{REF}. However, the FB ramp largely results from the ESR sensing the inductor ripple or from the external RC components therefore increasing the ramp amplitude increases the downward slope to reduce jitter.

Relationship between FB Ramp and Stability

A too-small ramp causes more problem than just jitter: a 90° phase delay between the ESR ripple and capacitor ripple makes the combined FB ripple non-monotonic if the capacitor ripple dominates the ramp ripple. Figure 4 compares system operation with either ESR or capacitor ripple dominanating the system. For instance, if the ESR ripple is large enough, it dominates the ramp on FB and the time for the FB downward slope to cross REF remains at the same point. Conversely, if the ESR ripple is too small, then the capacitor ripple dominates the FB ripple, the sub-harmonics become noticeable for non-monotonic FB ripple.

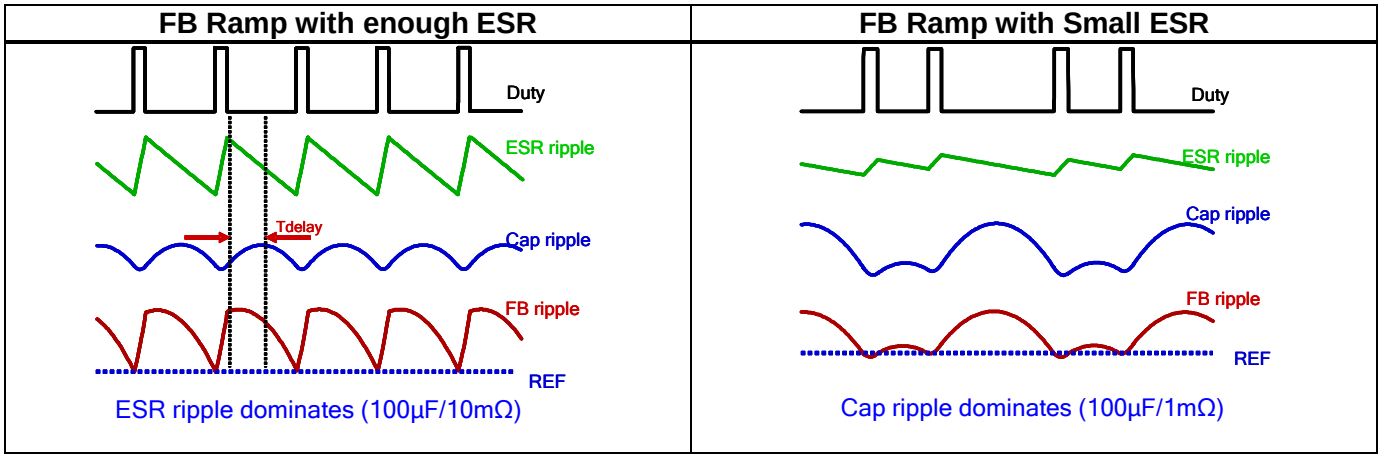

Figure 4: FB Ramp and Stability

Relationship between FB Ramp and Load Regulation

Because COT control turns on the PWM signal every time V_{FB} crosses V_{REF}—which means V_{REF} is just equal to the minimum value of V_{FB}, and the average value of V_{FB}($V_{FB(AVG)}$) does not equal to V_{REF}—$V_{FB(AVG)}$ equals the sum of V_{REF} and the average value of the ramp. COT control provides a seamless transient from the quasi-fixed–frequency CCM mode to pulse-frequency modulation (PFM) mode when the load decreases. During PFM mode, the switching frequency decreases when the load decreases, meaning that the shape of the FB ramp also varies with the load and causes variation in the average value on FB. Figure 5 shows the variation on the FB ramp with different loads.

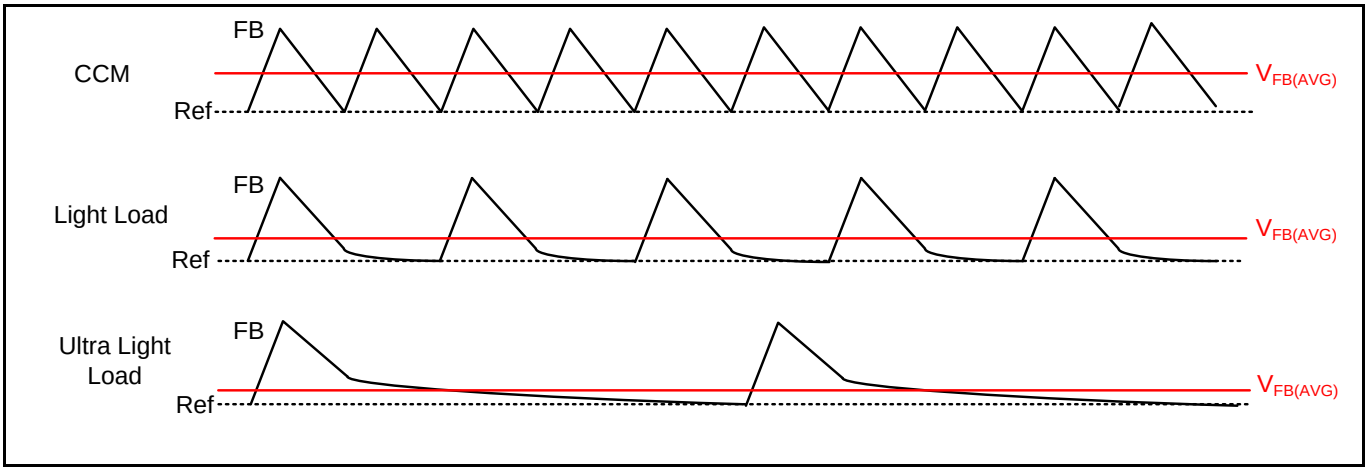

Figure 5: FB Ramp Variations with Different Loads

The FB ramp changes as the load changes from critical CCM mode to no-load; as the load decreases, VFB(AVG) decreases. So we are here mention the load regulation due to the $V_{FB(AVG)}$ change from no load to critical CCM load, the load regulation drop in the CCM mode when the load increase is not included here, and may not relate to this discussion.

Generally, the relationship between the $V_{FB(AVG)}$ and the V_{OUT} could be simplified as:

$$V_{OUT} = \frac{R1+R2}{R2} V_{FB(AVG)} \quad (1)$$

So the ΔV_{OUT} when the load changes from CCM to no-load condition could be estimated as):

$$\Delta V_{OUT} = \frac{R1+R2}{R2} \Delta V_{FB(AVG)} \approx k \frac{R1+R2}{R2} V_{RAMP} \quad (2)$$

Where k is difference between $V_{FB(AVG)}$ during CCM versus PFM—usually around 0.25. Reducing R1 and R2 reduces k. V_{RAMP} is the amplitude of the FB ramp.

If ESR dominates the FB ramp, then,

$$V_{RAMP} = \frac{R2}{R1+R2} \cdot \frac{1-D}{\frac{L}{R_{ESR}}} \cdot V_{OUT} \cdot t_{sw} \quad (3)$$

If the external ramp from R4 and C4 dominates the FB ramp, then

$$V_{RAMP} = \frac{1-D}{R4*C4} \cdot Vo \cdot t_{sw} \quad (4)$$

Where t_{SW} is the switching period, D is the duty cycle period, and L, R_{ESR}, R4, C4 refer to components in Figure 1.

Based on equation (2), better load regulation requires a small ramp on FB. Figure 6 provides a comparison between load regulation when different V_{RAMP} values.

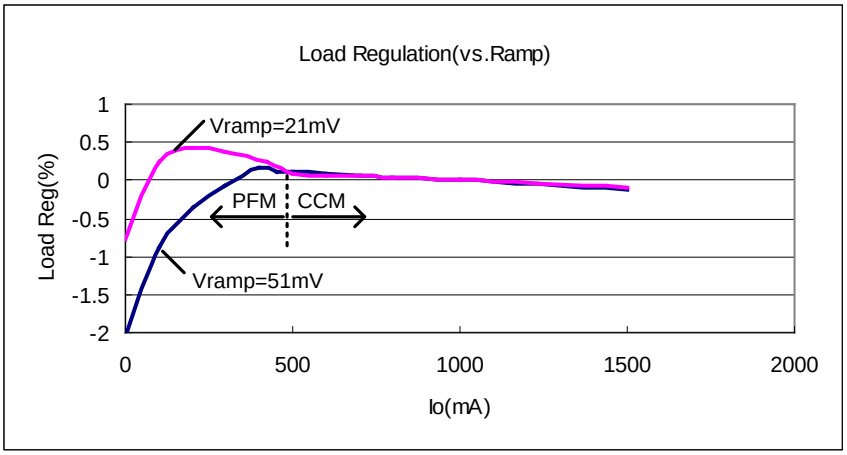

Figure 6: Load Regulation with Different Ramp Values: V_{IN}=12V, V_{OUT}=5V, L=4.7µH, f_{SW}=530kHz, I_{OUT}=1.5A, C_{OUT}=2×22µF (Ceramic)

Relationship between FB Ramp and Input Line Regulation

MPS's COT control provides quasi-fixed–frequency operation in CCM mode; i.e., the switching frequency remains unchanged with V_{IN}, but the FB ramp (and subsequently, $V_{FB(AVG)}$) changes as the inductor current changes. As shown in Figure 5, the largest value of $V_{FB(AVG)}$ during CCM, hence, the worst case for input line regulation occurs CCM. The difference between $V_{FB(AVG)}$ and V_{REF} can be derived from equations (5), (3), and (4) with different output capacitors.

$$V_{FB(AVG)} - V_{REF} \approx \frac{1}{2} V_{RAMP} \quad (5)$$

Based on equations (3) and (4), when V_{IN} increases, $V_{FB(AVG)}$ increases as the duty cycle decreases for V_{OUT} to increase according to equation (2). Figure 7 the FB ramp varying with V_{IN} in CCM mode.

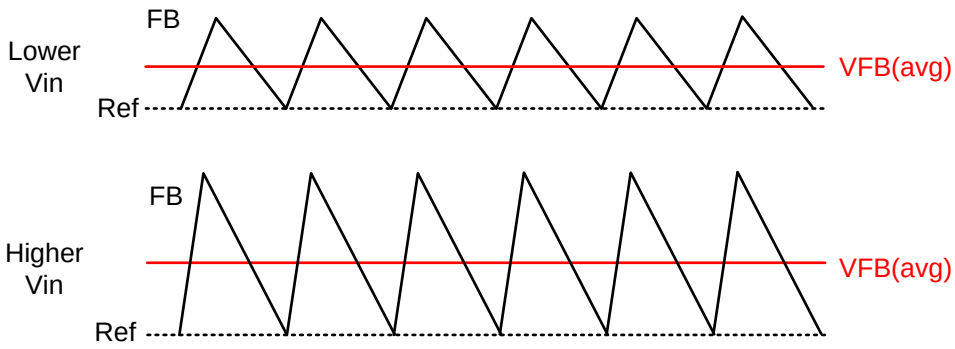

Figure 7: Variation of the FB ramp with V_{IN}

V_{OUT} vs. V_{IN} in CCM mode could be expressed as equations (6) and (7) with different output capacitors

$$\Delta V_{OUT\_ESR} = \frac{R1+R2}{R2}\Delta V_{FB(AVG)} \approx \frac{1}{2}\frac{R1+R2}{R2}\Delta V_{RAMP} = \frac{1}{2}\cdot\frac{\Delta D}{\frac{L}{R_{ESR}}}\cdot V_{OUT}\cdot t_{sw} \quad (6)$$

$$\Delta V_{OUT\_RC} \approx \frac{1}{2}\frac{R1+R2}{R2}\Delta V_{RAMP} = \frac{1}{2}\cdot\frac{R1+R2}{R2}\cdot\frac{\Delta D}{R4\cdot C4}\cdot V_{OUT}\cdot t_{sw} \quad (7)$$

Where ΔV_{OUT_ESR} represents changes in V_{OUT} with different ESR output capacitors, and ΔV_{OUT_RC} represents changes in V_{OUT} based on external RC compensation with ceramic capacitors. ΔD = duty cycle change due to the V_{IN} change.

Generally, a smaller FB ramp results in better line regulation. Figure 8 compares line regulations with different V_{RAMP} using external ramp compensation with ceramic output capacitors.

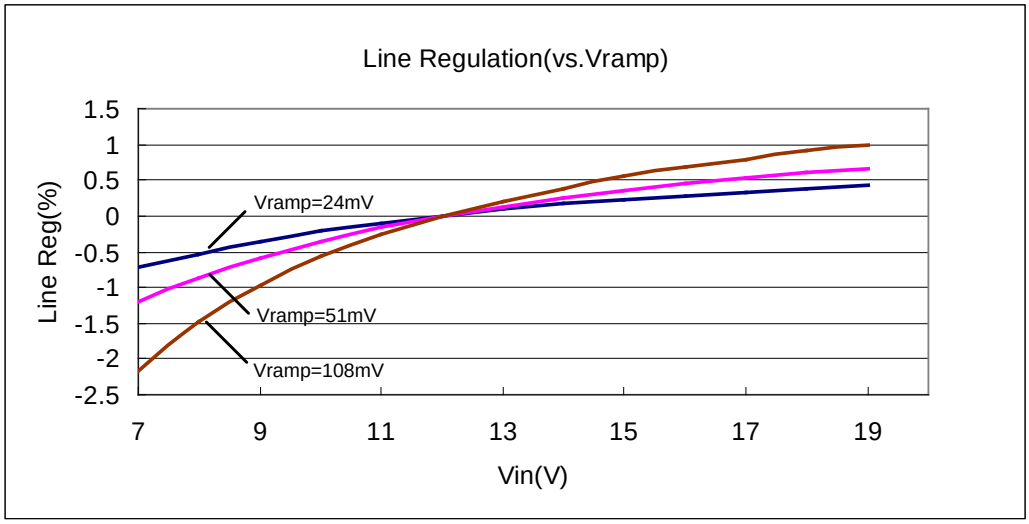

Figure 8: Variation of the FB ramp with V_{IN} (V_{IN}=7-19V, V_{OUT} =5V, L=4.7μH, f_{SW}=720kHz, I_{OUT}=1.5A, C_{OUT}=22μF×2/Ceramic)

DESIGN GUIDE FOR DIFFERENT OUTPUT CAPACITORS

The previous section describes key considerations in the ramp design: stabilizing the system requires the largest V_{RAMP} possible. However, desired load and line regulation requires trading off between the stability and the load and line regulation. Since the ramp results from the ESR of the output capacitors or from the external compensation when ESR is insufficiently large, this design guide is separated into two parts: Large ESR Output Capacitors, and the Small ESR Ceramic Output Capacitors.

LARGE ESR OUTPUT CAPACITORS

Capacitors with large ESR, such as POSCAPs, usually have a capacitance larger than 100μF, meaning that the ESR ripple dominates the output ripple, the ramp on FB is related to the inductor current, and no external compensation is need. Figure 9 shows an equivalent circuit in CCM without an external ramp circuit.

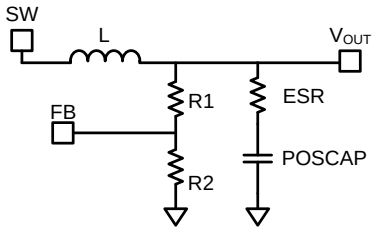

Figure 9: Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability without an external ramp , select an ESR value as follows:

$$R_{ESR} \geq \frac{(\frac{1}{Q \cdot \pi} + \frac{D_{MAX}}{2}) \cdot t_{SW}}{C_{OUT}} \quad (8)$$

Where Q is usually set around 0.7 to 1, D_{MAX} is the maximum duty cycle during the operation: In case V_{OUT} is fixed while V_{IN} varies, the maximum duty cycle can be found at the lowest V_{IN}

The limitation due to the load and line regulation can be expressed as:

$$R_{ESR} \leq \frac{L \cdot}{k \cdot (1\text{-}D_{MIN}) \cdot t_{sw}} \cdot \frac{\Delta V_{OUT\_LOAD}}{V_{OUT}} \quad (9)$$

$$R_{ESR} \leq \frac{2 \cdot L \cdot}{\Delta D \cdot t_{sw}} \frac{\Delta V_{OUT\_LINE}}{V_{OUT}} \quad (10)$$

Where k is usually set around 0.25, D_{MIN} is the minimum duty cycle during the operation, and ΔD= D_{MAX}-D_{MIN}. In addition, $\frac{\Delta V_{OUT\_LOAD}}{V_{OUT}}$ is the acceptable maximum peak-to-peak load-line regulation, and $\frac{\Delta V_{OUT\_LINE}}{V_{OUT}}$ is the acceptable maximum peak-to-peak input line regulation.

In some extreme cases when the differences between (8) and the minimum values of (9) and (10) are negative, other parameters must change to increase the difference by:

1. Increasing L,
2. Increasing f_{SW}, or
3. Selecting an output capacitor with a larger capacitance while keep the ESR almost the same.

SMALL ESR CERAMIC OUTPUT CAPACITORS

Selecting a small ESR capacitor as an output capacitor requires an external RC compensator to form a ramp on FB using R4 and C4, as shown in Figure 10. R9 acts as the noise filter resistance to filter the high frequency noise—usually set around 0Ω-1kΩ. To ensure that the FB ramp is not substantially affected by R9, select R9 to be much smaller than R1//R2.

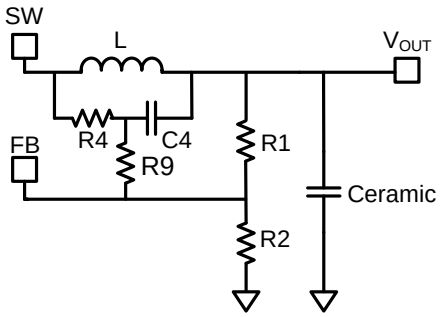

Figure 10: Simplified Circuit in PWM Mode with external components

For stability, R4 and C4 should meet:

$$\frac{1}{R4 \cdot C4} \geq \frac{(\frac{1}{Q \cdot \pi} + \frac{D_{MAX}}{2}) \cdot t_{SW}}{2 \cdot L \cdot C_{OUT}} + \frac{I_{OUT} \cdot 10^{-3}\Omega}{V_{OUT} \cdot t_{SW} \cdot (1 - D_{MAX})} \quad (11)$$

Where I_{OUT} is the full load output current, and Q=[0.7 to 1].

The limitation due to the load and line regulation on R4 and C4 is:

$$\frac{1}{R4 \cdot C4} \leq \frac{R2 \cdot}{k \cdot (R1 + R2) \cdot t_{sw} \cdot (1\text{-}D_{MIN})} \cdot \frac{\Delta V_{OUT\_LOAD}}{V_{OUT}} \quad (12)$$

$$\frac{1}{R4 \cdot C4} \leq \frac{2 \cdot R2 \cdot}{(R1 + R2) \cdot \Delta D \cdot t_{sw}} \cdot \frac{\Delta V_{OUT\_LINE}}{V_{OUT}} \quad (13)$$

Where k is usually set around 0.25, D_{MIN} is the minimum duty cycle during the operation, $\Delta D = D_{MAX}\text{-}D_{MIN}$, $\frac{\Delta V_{OUT\_LOAD}}{V_{OUT}}$ is the acceptable maximum peak-to-peak load line regulation, and $\frac{\Delta V_{OUT\_LINE}}{V_{OUT}}$ is the acceptable maximum peak-to-peak input line regulation.

Choose a minimum value between (12) and (13), then an appropriate range for R4 and·C4 is then defined by (11). Besides meeting the requirements in equations (11)-(13), C4 should also meet the following:

$$\frac{1}{2\pi \times f_{SW} \times C4} < \frac{1}{5} \times \left(\frac{R1 \times R2}{R1 + R2} + R9 \right) \quad (14)$$

Thus allowing C4 and R4 to be selected separately. Once C4 is selected, select R4 from the smaller end of its available range for better stability and smaller jitter, or a larger R4 for better transient, light-load performance, and the load and line regulation.

If the range for R4 and C4 selection is small or even negative, then make flowing changes to improve the range:

1) Increase L or C_{OUT}
2) Increase f_{SW}
3) Reduce R1 and R2 if the actual load regulation is poor for the ultra light load condition drop

DESIGN EXAMPLE

- Typical input voltage: V_{IN} =12V
- Maximum input voltage: V_{IN_MAX}=19V
- Minimum input voltage: V_{IN_MIN}=9V
- Output voltage: V_{OUT} = 5V
- Maximum output current: I_{OUT} = 6A
- Output Capacitors: C_{OUT}=22μF×3/Ceramic
- Inductance: L = 4.7μH
- Switching frequency: f_{SW} = 500kHz
- Duty cycle: D_{MAX}=0.556@ V_{IN} =9V, D_{MIN}=0.263@ V_{IN} =19V
- Reference voltage: V_{REF}=0.815V
- Maximum peak-to-peak Load Regulation: $\frac{\Delta V_{OUT\_LOAD}}{V_{OUT}} = 1.5\%$
- Maximum peak-to-peak Line Regulation: $\frac{\Delta V_{OUT\_LINE}}{V_{OUT}} = 2\%$

1) Selecting R1, R2 and R9

Since this application note only focuses on selecting ramp parameters, refer to relevant datasheets for feedback resistor design and V_{OUT} selection.

The initial calculations usually cannot provide absolute feedback resistor calculations, but the ratio set by the V_{OUT} and V_{REF} is enough to design the external ramp compensation R4 and C4, assuming R1=51.3kΩ, R2=10kΩ, and R9=0.5kΩ.

2) Determining RC Constraints Based on the Stability Requirement

Based on the previous case, V_{IN} ranges from 9V-19V, hence the maximum duty cycle (D_{MAX}) occurs at V_{IN}=9V (according to equation (11)). Set Q=0.7, so that R4 and·C4 satisfies:

$$\frac{1}{R4 \cdot C4} \geq 3.71 \cdot 10^3 (s^{-1})$$

3) RC Constraint Based on the Load Regulation Requirement

From equation (12), the minimum value occurs during the shortest duty cycle, so R4·C4 should meet following requirements at the maximum input voltage.

$$\frac{1}{R4 \cdot C4} \le 6.15 \cdot 10^3 (s^{-1})$$

4) RC Constraint Based on the Input Line Regulation Requirement

R4 and·C4 are constrained by the maximum input line regulation. Based on equation (13), R4 and C4 must meet:

$$\frac{1}{R4 \cdot C4} \le 10.3 \cdot 10^3 (s^{-1})$$

5) Determining the Minimum C4 Value from Equation (14):

$$C4 \ge \frac{5}{2\pi \cdot fsw \cdot (R1//R2 + R9)} = 177pF$$

6) Combined with requirements from step 2) - 5),

R4=739kΩ→1.22MΩ if C4=220pF

R4=492kΩ→816kΩ if C4=330pF

Choose a smaller R4 within the range if the load and line regulation requirements are met.

7) Once the R4 and C4 are selected, refine R1 and R2 based on the related datasheets. Select typical values of V_{IN}=12V,R4=492kΩ,C4=330pF, R2=10kΩ, R9=0.5kΩ for:

$$R1 = \frac{R2}{\frac{V_{FB(AVG)}}{V_{OUT} - V_{FB(AVG)}} - \frac{R2}{R4 + R9}} = 56.2k\Omega$$