Replacing the Si9979 with the MP6532

Application Note

Prepared by Pete Millett

April 2017

ABSTRACT

The MPS MP6532 is a three-phase pre-driver for brushless DC motors. The MP6532 is supplied in a 28-pin QFN or a 28-pin TSSOP package.

The device generates the required gate drive voltages to drive six, external, N-channel MOSFET transistors, arranged as a three half-bridge output. Hall sensor inputs are provided for the self-contained trapezoidal commutation of 3-phase motors.

The MP6532 is very similar functionally to the now end-of-life Vishay Siliconix Si9979 3-phase brushless DC motor controller. In most applications, the MP6532 can replace the Si9979 while providing added features, a smaller footprint, and a compelling price.

This application note explains the differences between and what should be considered when replacing the Si9979 with the MP6532.

Application Circuits

The following are basic application schematics for the Si9979 (see Figure 1) and the MP6532 (see Figure 2). Note that in both cases there may be additional components required in some applications that are not shown in these diagrams. For example, resistors in series with the MOSFET gates may be needed to control the output slew rate.

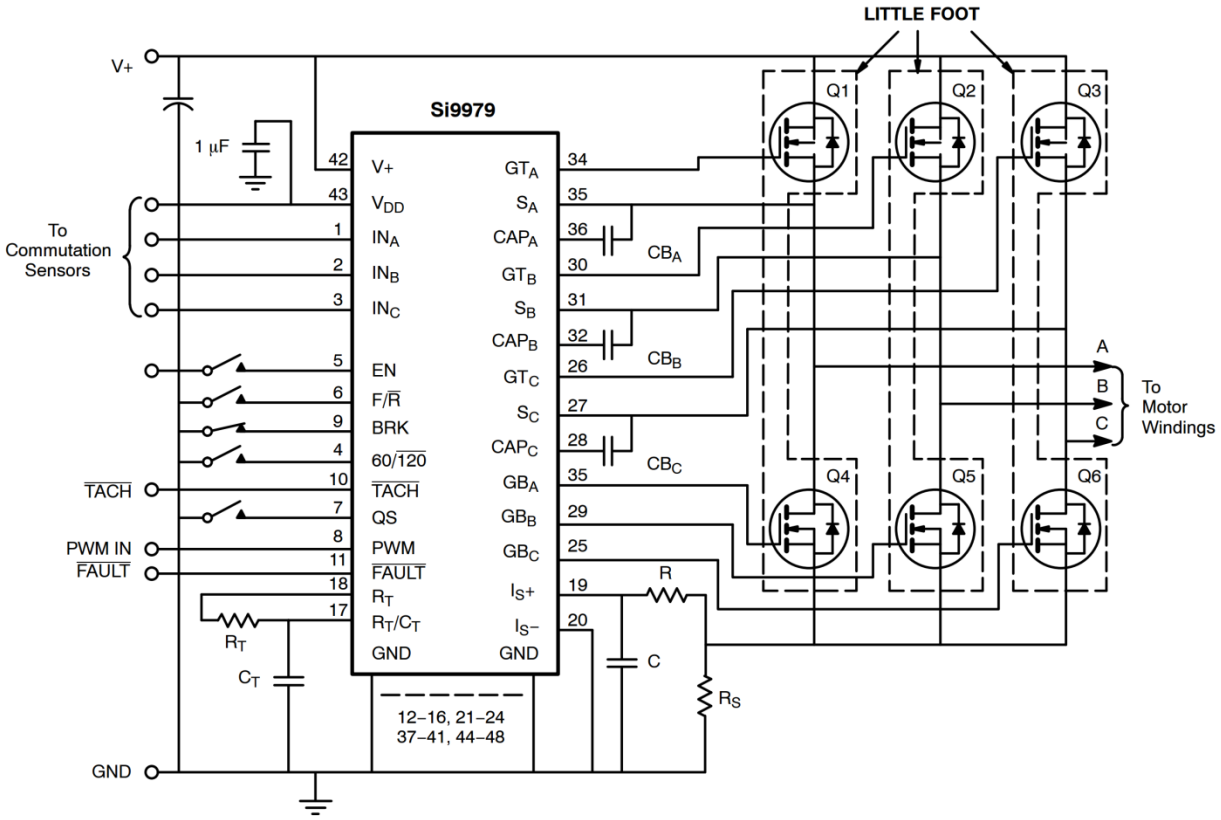

Figure 1: Si9979 Basic Application Circuit

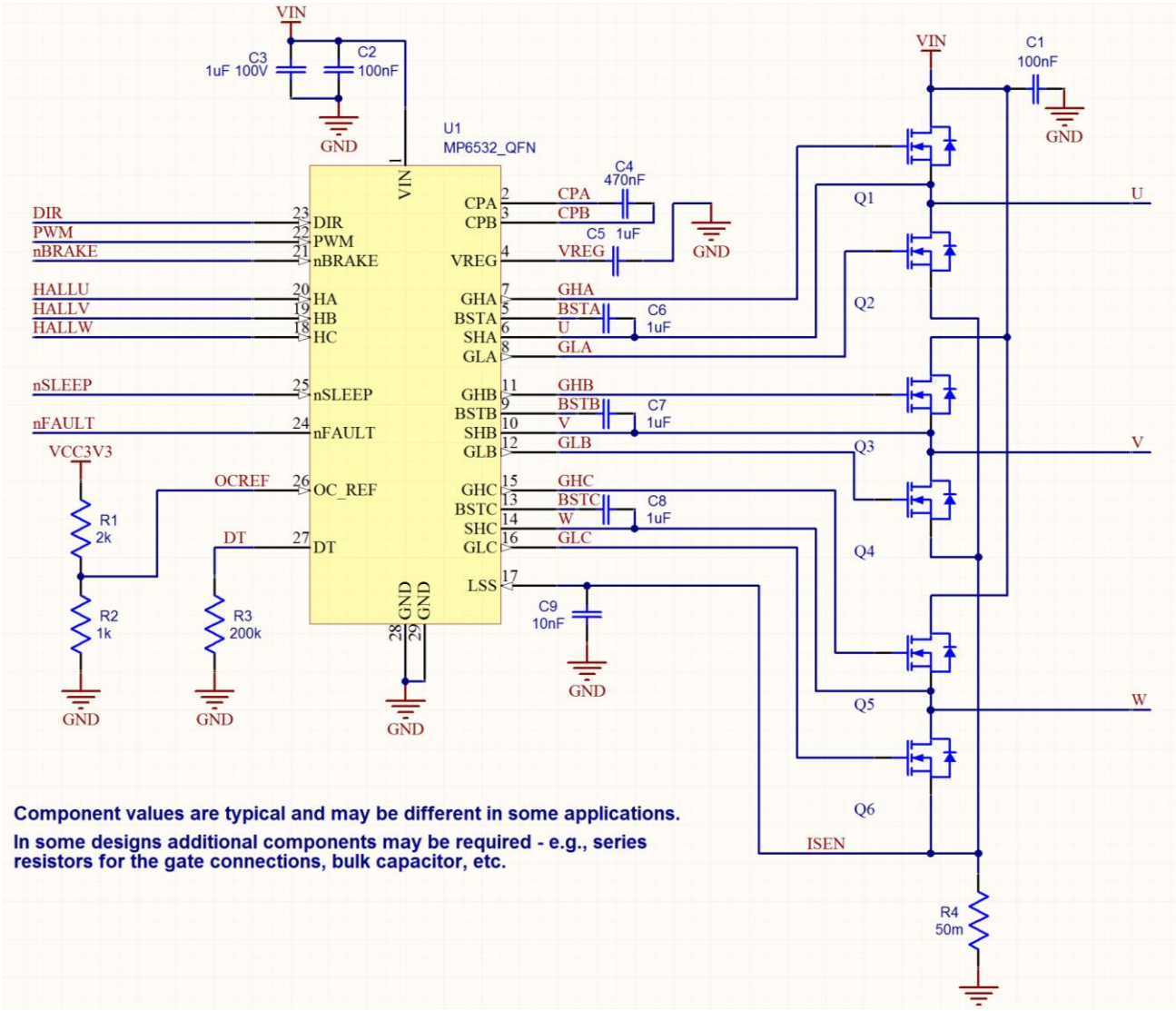

Figure 2: MP6532 Basic Application Circuit

These application circuits show that the parts are very similar and require nearly the same external connections and components.

Table 1 is a summary of the pin connections. Table 2 is a feature comparison of the two parts.

Table 1: Pin Comparison

	Si9979	MP6532
PWM input pin	PWM	PWM
Brake input pin	BRK (active high)	nBRAKE (active low)
Motor direction input pin	F/R	DIR
Hall input pins	INA, INB, INC	HA, HB, HC
Low-side overcurrent sense	IS+	LSS
Low-side gate outputs	GBA, GBB, GBC	GLA, GLB, GLC
High-side gate outputs	GHA, GHB, GHC	GHA, GHB, GHC
Output connection (HS source)	SA, SB, SC	SHA, SHB, SHC
Bootstrap capacitor pin	CAPA, CAPB, CAPC	BSTA, BSTB, BSTC
V+ supply	V+	VIN
Gate drive supply output	VDD	VREG
Enable input pin	EN	nSLEEP
nFAULT output (active low)	FAULT	nFAULT
Hall sensor configuration pin	60/120	Not available (120° only)
Sync/asynchronous configuration pin	QS	Not available (sync only)
Overcurrent retry timing pins	RT, RT/CT	None (fixed retry)
TACH output	TACH	Not available
Dead time programming pin	Not available	DT
VDS sense programming pin	Not available	OC_REF
Charge pump pins	Not available	CP1, CP2
Power input	V+	VIN
Ground	GND, IS-	GND

Table 2: Feature Summary

	Si9979	**MP6532**
Package	SQFP-48 (9mmx9mm)	QFN-28 (4mmx4mm) or TSSOP-28 (9.7mmx4.7mm)
Hall inputs	60° or 120°, 5V only	120° only, 5V or 3V compatible
V+ supply	20 - 40V	5 - 60V
Dead time	Fixed 100/300nS	Adjustable w/ ext resistor 3 - nS - 6µS
Gate drive voltage	Internal, 15 - 17V	Internal, 10 - 12V (even if V+ = 5V)
Under-voltage lockout	12.2V typ.	5.1V max
Current limit comparator	100mV threshold, adjustable retry	500mV threshold, 70µS retry
Sync/async switching	Either, set with QS input	Sync only
TACH output	Yes	No
100% duty cycle support	No (bootstrap only)	Yes (bootstrap + charge pump)
VDS voltage sensing protection (de-sat detection)	No	Yes, with adjustable threshold
Low-power sleep mode	No	Yes (<1mA)

SPECIFIC NOTES AND RECOMMENDATIONS

FET Connections

Connections to the external N-channel MOSFETs are identical between the two devices. Depending on the FET selection and desired slew rate, resistors may be required in series with the gates. In some cases, a diode may be placed in parallel to provide asymmetric turn-on and turn-off.

Dead Time

The Si9979 has an internally fixed dead time of 100nS rising and 300nS falling.

The MP6532 has an adjustable dead time, which has the same rising and falling times. To set the MP6532 dead time to about 300nS, connect an 82kΩ resistor between DT and ground. The dead time can be changed as needed to accommodate different FETs and gate series resistances, if used.

Hall Inputs and Commutation

The Si9979 has hall inputs that can be set to 60° or 120° spacing using the 60/120 programming input pin. The inputs must be 5V signals since the V_{IH} of these pins is 4V.

The MP6532 hall inputs are designed for 120° sensor spacing only and have a low enough V_{IH} threshold that either 5V or 3.3V hall sensors can be used.

Charge Pump and 100% Duty Cycle Operation

The Si9979 generates the high-side gate drive voltage from the bootstrap circuit only. Because of this, the outputs must be driven low periodically to refresh the bootstrap capacitor, which holds the high-side gate drive voltages. In other words, the driver does not support true 100% duty cycle operation. Additionally, the input voltage must be above 20V for the part to operate.

The MP6532 works a bit differently. It has an internal charge pump (using an external capacitor) that generates a quasi-regulated 11V supply used for gate driving, so it can fully enhance the external MOSFETs even if the input supply falls as low as 5.5V. The MP6532 uses a bootstrap circuit to generate the high-side gate drive, but it also has an internal “trickle” charge pump that maintains the charge on the bootstrap capacitors, even when the outputs are held high. The MP6532 can support true 100% duty cycle operation.

Over-Current Protection

Both the Si9979 and MP6532 have a comparator that can be used to monitor the voltage across a low-side sense resistor to detect over-current. The threshold voltage is different for each device: 100mV for the Si9979, and 500mV for the MP6532. The Si9979 will retry (re-enable the outputs) after a period of time that can be adjusted using external R and C components. The MP6532 has a fixed retry time of 70µs.

Additionally, the MP6532 senses the voltage between the source and drain of all external FETs when they are turned on. If this voltage exceeds the voltage applied to OC_REF, a fault is recognized, and the device latches off. This feature is sometimes called de-saturation protection. If this feature is not needed, pull OC_REF up to a voltage that ensures that the circuit will not be triggered falsely (e.g.: 3.3V).

Device Enable and Sleep Mode

The Si9979 has an input pin called ENBL that disables the outputs of the device when set at inactive low.

The MP6532 has an input called nSLEEP, which also disables the device when driven low. Any unnecessary internal circuitry is also shut down to save power. The motor can be enabled and disabled by applying a signal to nSLEEP. When re-enabling the part by driving nSLEEP high, about 1ms of time is needed for the charge pump and internal circuits to stabilize before the outputs become active, so the nSLEEP input cannot be used like the PWM input to control motor speed. When nSLEEP is low, input signals to the Hall inputs, PWM, and DIR pins are ignored.

Synchronous and Asynchronous Operation

The Si9979 has an input pin (QS) that allows users to select either synchronous or asynchronous PWM. In asynchronous mode (QS = 1), the PWM input signal turns the high-side MOSFET on and off only, and the low side MOSFET remains off. In synchronous mode (QS = 0), the low-side MOSFET is turned on when the high-side MOSFET is turned off. The MP6532 only supports synchronous mode.