The Future of Analog IC Technology

MP4033: Application Note for a TRIAC-Dimmable, Offline LED Controller with Primary-Side Control and Active PFC

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April. 18, 2014

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1. INTRODUCTION

The MP4033 is a TRIAC-dimmable, offline LED lighting controller with primary-side control and active PFC. Its adaptive dimmer type detection and phase-cut-based dimming control can achieve good dimmer compatibility and deep dimming range. Besides, the MP4033 can support direct PWM dimming.

The primary-side-control significantly simplifies the LED lighting driving system by eliminating the opto-coupler and the secondary feedback components for an isolated single stage converter. Its proprietary real-current control method can accurately control the LED current from primary-side information.

The MP4033 has a power factor correction (PFC) function that can achieve a high power factor (PF)>0.9. The device also works in boundary conduction mode to reduce switching loss and improve EMI performance.

The MP4033 has an integrated charging circuit at the VCC pin to start-up with a delay of less than 200ms when using a 22μF bulk capacitor. The low-voltage current source outputs a maximum 25mA charging current for VCC capacitor.

With the unique control of the driver pin DIM, the MP4033 supports color temperature and brightness control for warm sunset dimming application.

The MP4033 provides multiple advanced fault protections to enhance the system safety, including over-voltage protection, short–circuit protection, primary-side over-current protection, VCC under-voltage lockout, ZCD pin short protection, programmable thermal fold-back (MSOP10/SOIC14) and thermal shutdown. All protections feature auto-restart.

The MP4033 is available in SOIC8/MSOP10/SOIC14 package, The MSOP10/SOIC14 has NTC pin and DIM pin.

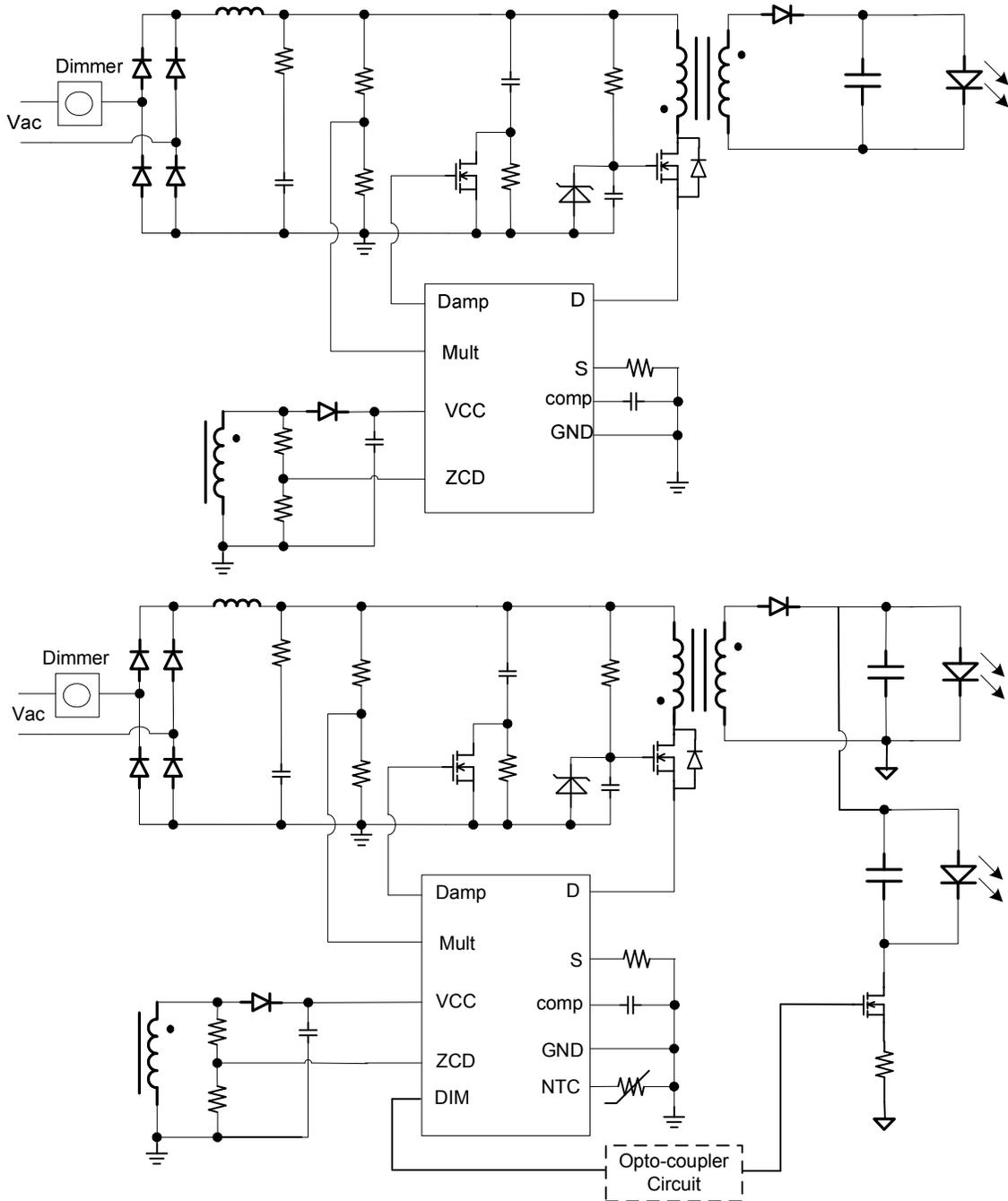Figure 1 shows the typical application circuit. (SO8/MSOP10)

Figure 1: Typical Application

2. PRIMARY-SIDE CONTROL, BOUNDARY-CONDUCTION MODE WITH ACTIVE PFC

Conventional off-line LED drivers use secondary-side control that senses the LED current directly. An error amplifier compares this current level against a reference produced by a device such as a TL431, and the compensated output determines the primary-side duty cycle to regulate the LED current. Although this control method can directly control the LED current and current accuracy under any condition, it requires additional secondary-side components—including a sensing circuit, comparison and compensation circuits, an opto-coupler, and bias power supplies—that significantly increase system complexity and cost.

In addition, the primary-side input stage typically uses a full-wave rectifier bridge with an E-cap filter to generate a DC voltage. The E-cap must be large enough to limit the DC voltage ripple. This means the instantaneous input line voltage is lower than the DC voltage on the E-cap for most of a line half-cycle, and that the rectifier diodes only conduct a small portion of the voltage. This voltage limitation causes the input line current to act like a series of narrow pulses whose amplitudes are about 10x higher than the average DC level. The drawbacks include: a high current peak and RMS current drawn from the line, line-input–current distortion limiting the power factor to about 0.5 to 0.6, and large induced harmonics.

Figure 1 shows that the MP4033 uses primary-side control, which eliminates secondary feedback components to significantly reduce the component count and cost. The MP4033 also works in boundary-conduction mode with active PFC, with a power factor >0.9 for the input, and reduce THD to meet IEC61000-3-2 requirements.
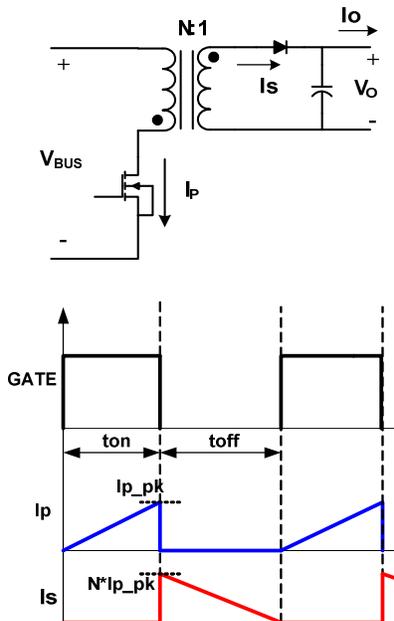
A. PRIMARY-SIDE CONTROL

Figure 2: Transformer Currents Relative to the BCM Flyback Converter

Given that the LED current is the average current of the transformer's secondary side, $I_o = I_{s\_avg}$, as shown in Figure 2, the average secondary-side current in boundary-conduction mode can be calculated as:

$$I_{s\_avg} = \frac{\frac{1}{2} \cdot N \cdot I_{p\_pk} \cdot t_{off}}{t_{on} + t_{off}}$$

Where I_{s_avg} is the average secondary-side current, and I_{p_pk} is the peak primary-side current. The MP4033 samples the primary-side peak current to calculate the average current. Since the average current is proportional to the output current, if the average current is a controlled constant, the output current is also constant, allowing for primary-side control.

B. BOUNDARY-CONDUCTION MODE

The MP4033 works in boundary conduction mode where the transformer functions at the boundary between the continuous and discontinuous mode.

In a conventional fixed-frequency flyback converter working in discontinuous conduction mode (DCM), the primary switch (MOSFET) turns on at a fixed frequency and turns off when the current reaches the desired level. When the MOSFET turns off, the energy stored in the inductor forces the secondary side diode to turn on, and the inductor current decreases linearly from the peak value to zero. When the current drops to zero, the parasitic resonance of the magnetizing inductor and the sum of the parasitic capacitance causes the MOSFET drain-source voltage to oscillate. The MOSFET can turn on at any point during the parasitic resonance, including when the drain voltage is lower than the bus voltage (meaning low switching losses and high efficiency), and when the drain voltage is much higher than the bus voltage (meaning high switching loss). This feature is observable in the efficiency curves of a discontinuous flyback converter with a constant load as input-voltage efficiency fluctuations as the turn-on switching loss changes with the turn-on drain voltage.

In boundary conduction mode, the switch does not have a fixed switching frequency. Instead, the controller always turns on the switch when the drain voltage goes low by detecting the auxiliary winding voltage, V_{ZCD}, the ZCD voltage is a ratio of primary winding and auxiliary winding. Figure 3 shows that by setting the falling-edge detection near zero, the parasitic resonance causes the ZCD voltage to decrease when the secondary side current deceases to zero: Conversely, when V_{ZCD} reaches the detection threshold, the MOSFET turn-on signal triggers. The transformer magnetizing inductance, parasitic capacitance, and ZCD filtering capacitor determine the detection time delay. The feedback loop determines the switch-on time, similar to conventional peak-current–mode control. The energy stored in the magnetizing inductor then transfers to the output.
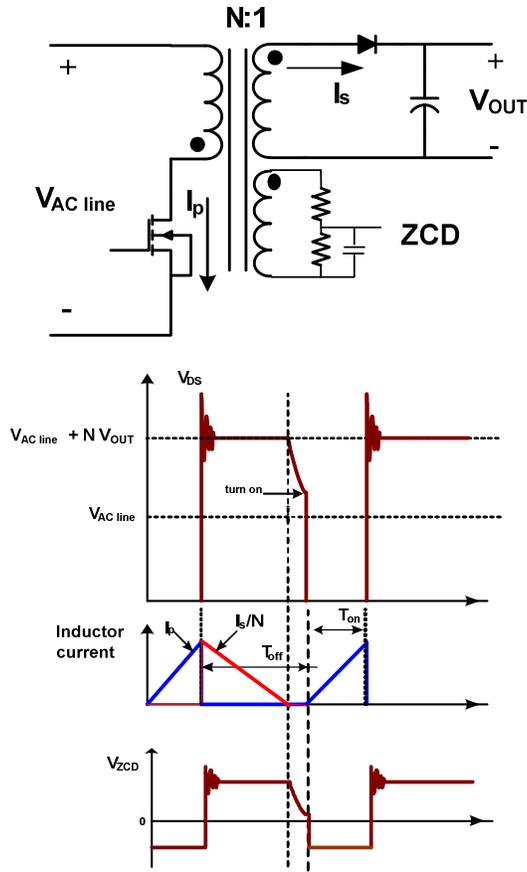
Figure 3: Boundary Conduction Mode

Compared to conventional flyback under continuous conduction mode (CCM) and DCM operation, boundary-conduction mode operation minimizes the turn-on switching loss, thus increasing efficiency and suppressing the MOSFET temperature rise.

C. ACTIVE PFC
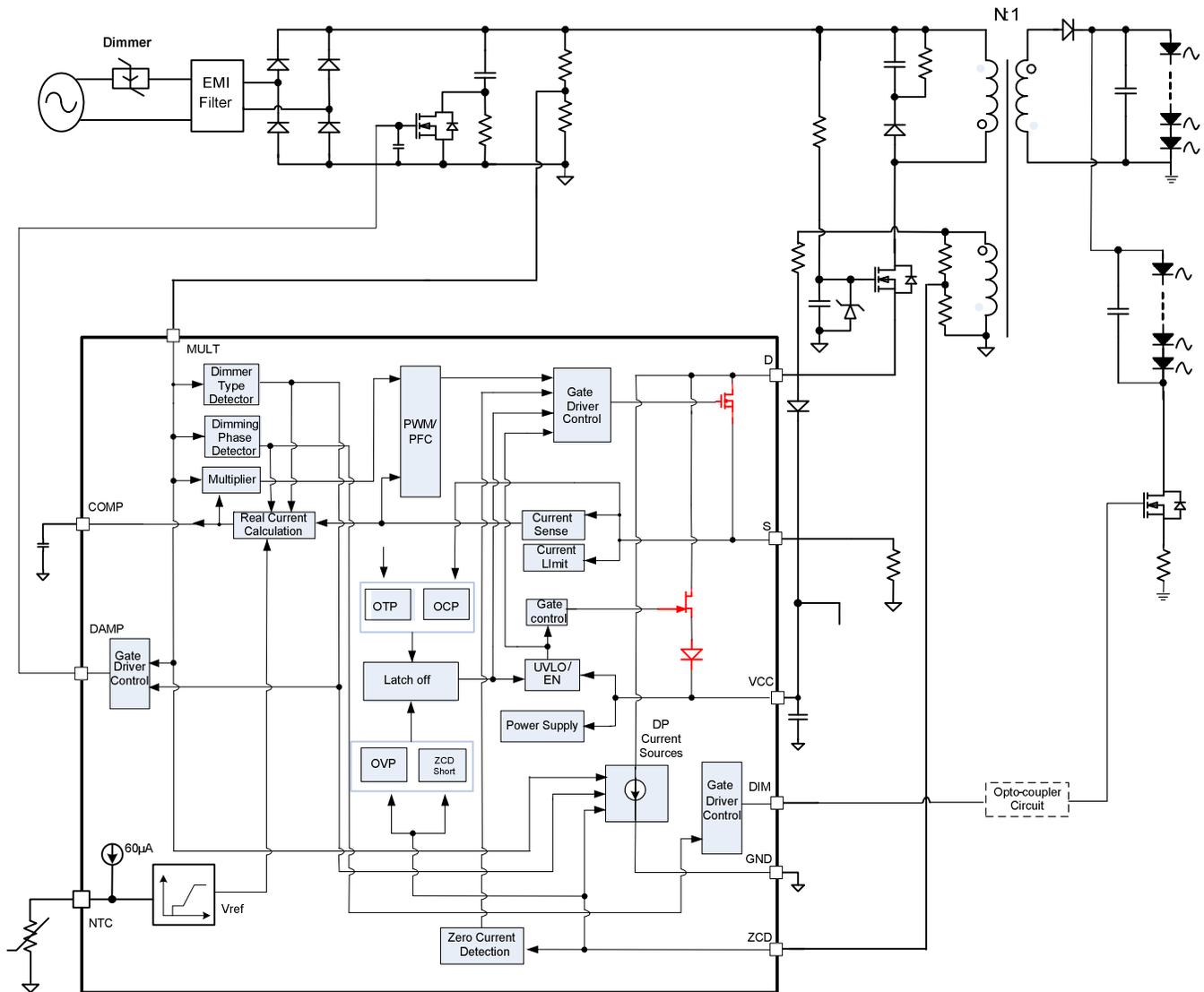
Figure 4: MP4033 Functional Block Diagram and LED Driver

The MP4033 integrates an active PFC function. Figure 4 shows the functional block diagram and the LED converter driver. The converter consists of an EMI filter, a diode bridge rectifier, a flyback circuit using the MP4033. The following description summarizes converter operation with active PFC:

The diode bridge rectifies the AC line voltage, which then goes to the flyback circuit. When the internal main MOSFET turns on, the transformer's primary-side current ramps up from zero. The S pin senses this primary-side current through a sensing resistor, and this signal goes to the real-current calculation block to calculate its average value. The internal error amplifier compares the average value against an internal reference to generate an error signal that is proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (below 20Hz), then the error signal is a DC value for over a line half-cycle and kept constant until the average value equals the reference: This regulates the output LED current to a required constant value.

The error signal goes to the multiplier block with a portion of the rectified mains voltage. The resulting signal is a rectified sinusoid with a peak amplitude that depends on the peak line voltage and the value

of the error signal. The output of the multiplier goes to the negative input of the current comparator to act as a sinusoidal reference for the PWM. When the S-pin voltage equals the value on the negative input of the current comparator, the external MOSFET turns off. The rectified signal envelops the peak primary current. and has the same phase as the main input voltage to implement a good power factor.
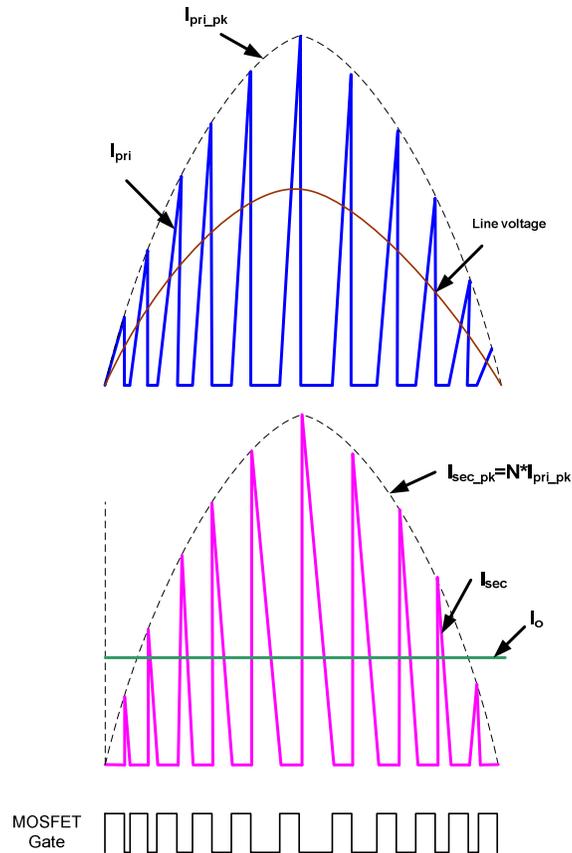
Figure 5: Primary and Secondary Transformer Currents and MOSFET Gate Timing

Figure 5 shows both transformer currents and the gate timing. The operating frequency increases as the instantaneous line voltage decreases; when the line voltage approaches the zero-crossing point, the frequency increases dramatically. The MP4033 has an internally-set 5μs minimum off-time to limit the maximum switching frequency and to improve efficiency and reduce EMI.

3. ADAPTIVE DIMMER TYPE DETECTION AND PHASE-CUT-BASED DIMMING CONTRL

A. ADAPTIVE DIMMER TYPE DETECTION

In TRIAC dimming LED lighting applications, the LED driver will meet different dimmer types, like leading edge dimmers, trailing edge dimmers, or no dimmer connected. The different dimmer conditions require the driver to work with different mode to well compatible with the dimmers. The MP4033 integrates adaptive dimmer type detection to accurately detect what a dimmer is connected at system start up. The dimmer type will be divided into leading edge dimmer, trailing edge dimmer or no dimmer condition. According to the detected dimmer type, the MP4033 works in different mode to best suit the dimmer compatibility and achieve high performance.
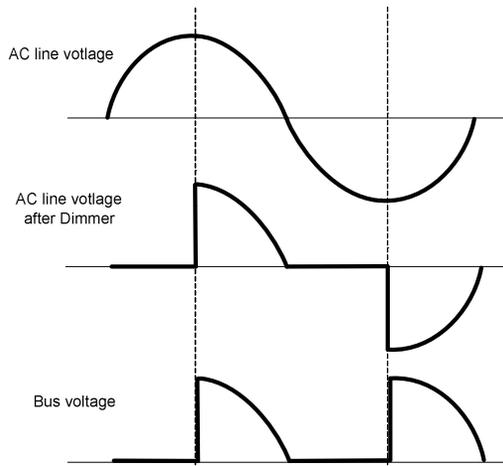

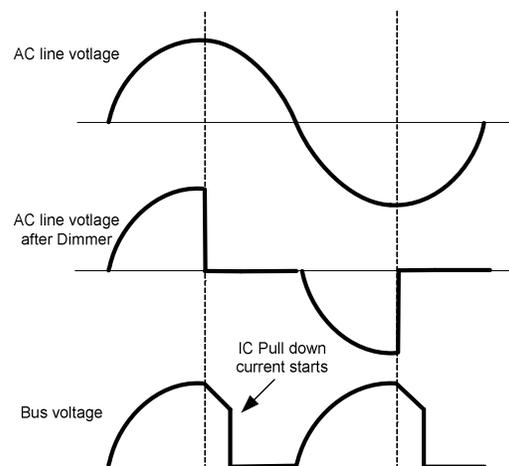**Figure 6: Leading edge dimmer waveforms**   **Figure 7: Trailing edge dimmer waveforms**

The MP4033 will count the bus voltage rising time and falling time to judge what is the dimming condition is. Figurer 6 shows leading edge dimmer waveforms, when dimmer turns on, a sharp leading edge is occurred on bus voltage. If the rising time is shorter than the IC internal comparing threshold value tLEADING, the dimmer will be recognized as leading edge dimmer. Figure 7 shows trailing edge dimmer waveforms, when dimmer turns off, the bus voltage will decrease slowly due to the big capacitance after the diode bride. In order to get a sharp trailing edge, the IC will generate a proper dimming pull down current for trailing edge dimmer to fast pull down the bus voltage. If the bus voltage falling time is shorter than the IC internal comparing threshold value tTRAILING, the dimmer will be recognized as trailing edge dimmer. If there is neither leading edge nor trailing edge, it will be recognized as no dimmer condition.

At system start up, the IC will be forced to work at trailing edge dimming mode first, if leading edge dimmer is detected, the IC will transfer to leading edge dimming mode, if trailing edge dimmer is detected, the IC will keep working in trailing edge dimming mode, if no leading and trailing edge dimmer is detected, the IC will transfer to no dimming mode.

B. PHASE-CUT-BASED DIMMING CONTROL

The MP4033 implements Phase-cut-based dimming control (including leading edge dimmer and trailing edge dimmer). Shown in figure 6 and 7, both for leading edge dimmer and trailing edge dimmer, the input bus voltage is cut off after dimmer turns off in each line cycle. The MP4033 detects the dimming turn-on cycle through the MULT pin, which is fed into the control loop to adjust the internal reference voltage. When the MULT voltage exceeds 0.28V, the IC treats this signal as a dimmer turn-on signal. When the MULT voltage falls below 0.1V, the system treats this as a dimmer turn-off signal. The

MP4033 has a 30% line-cycle–detection blanking time with each line cycle. The real phase detector output adds this time, as shown in figure 8. That means if the turn-on cycle exceeds 70% of the line cycle, the output maintains the same maximum current. It improves the line regulation during the maximum turn-on cycle or without a dimmer.
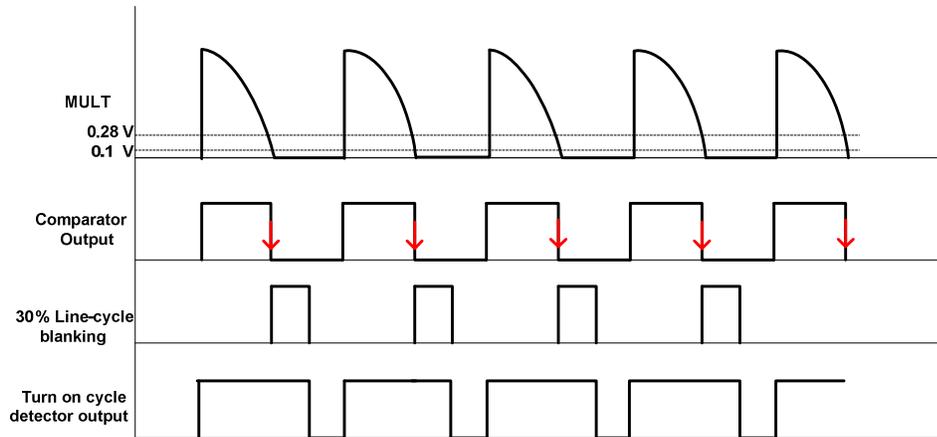
Figure 8: Dimming Turn-On Cycle Detector

If the turn-on cycle decreases to less than 70% of the line cycle, the internal reference voltage decreases as the dimming turn-on phase decreasing, and the output current decreases accordingly to implement dimming. As the dimming turn-on cycle decreases, the COMP voltage also decreases. For leading edge dimmer, once the COMP voltage reaches to 1.9V, it is clamped so that the output current decreases slowly to maintain the TRIAC holding current and avoid random flicker. Figure 9 shows the relationship between the leading edge dimming turn-on phase and output current.
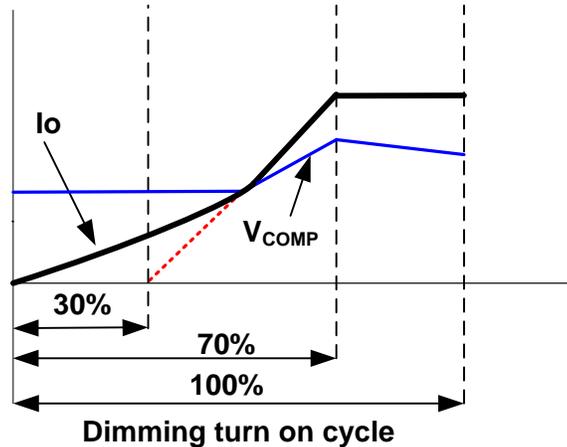
Figure 9: Leading Edge Dimming Curve

For trailing edge dimmer, it does not need to maintain a current to keep the dimmer turn on, so the COMP voltage is clamped at 1.6 to get deeper dimming depth, Figure 10 shows the relationship between the trailing edge dimming turn-on and output current.
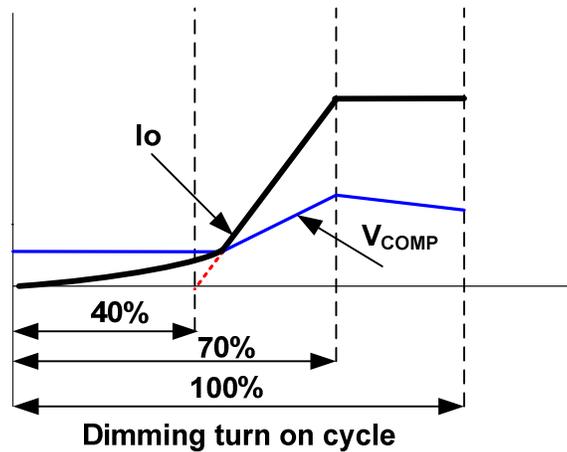
Figure 10: Trailing Edge Dimming Curve

C. DIMMING PULL-DOWN CURRENT SOURCE

There are three dimming pull down current sources inside the chip from D pin to internal GND. The 150mA current source is for trailing edge dimming mode, the other two (weak/strong) current sources are for leading edge dimming mode. The dimming pull down current is used to pull down the rectified line voltage to zero quickly to avoid any mis-detection on the MULT pin. If the leading edge dimmer is detected, the dimming pull-down current source turns on when the MULT decreases to 0.25V and turns off until the MULT increases to 0.35V. If trailing edge dimmer is detected, the dimming pull-down current source turns on when the MULT decreases to 0.45V and turns off until the MULT increases to 0.28V. The weak/strong dimming pull down current source can be selected through different resistance on the ZCD pin (for the detailed selection equation, please refer to the PIN function of ZCD). In real application design, the weak/strong dimming pull down current selection is related to the detailed application SPEC. Usually, it is recommended to use strong dimming pull down current in high line (220/230VAC) input or power larger than 10W low line input (100/120VAC) application.

Below table are the dimming mode operation summaries.

	No Dimming Mode	Leading edge dimming	Trailing edge dimming
MP4033 Operation	1. Damp signal keeps high 2. DP current stops	1. Damp works 2. DP current 40mA/10mA optional 3. COMP low clamp: 1.9V 4. Dimming Range: max 70% to min 30% (dimming phase cycle)	1. Damp works 2. DP current 150mA 3. COMP low clamp: 1.6V 4. Dimming Range: max 70% to min 45% (dimming phase cycle)

4. PIN FUNCTION AND OPERATION INFORMATION

A. PIN INTRODUCTION (HERE USING MSOP10 FOR EXAMPLE, SO8/SOIC14 CAN REFER TO IT)

Pin1 (MULT)

Figure 11 shows the MULT pin circuit. The MULT pin provides one of the inputs to the internal multiplier. Connect this pin to the tap of the resistor divider from the rectified instantaneous line voltage, which will produce a sinusoidal multiplier output. This output signal provides the reference for the current comparator, which shapes the primary peak current into a sinusoid that is in-phase, with the input line voltage. The MULT pin also provides for dimming phase detector, dimming type detector, DP current source on/off threshold and DAMP gate turn on/off threshold.
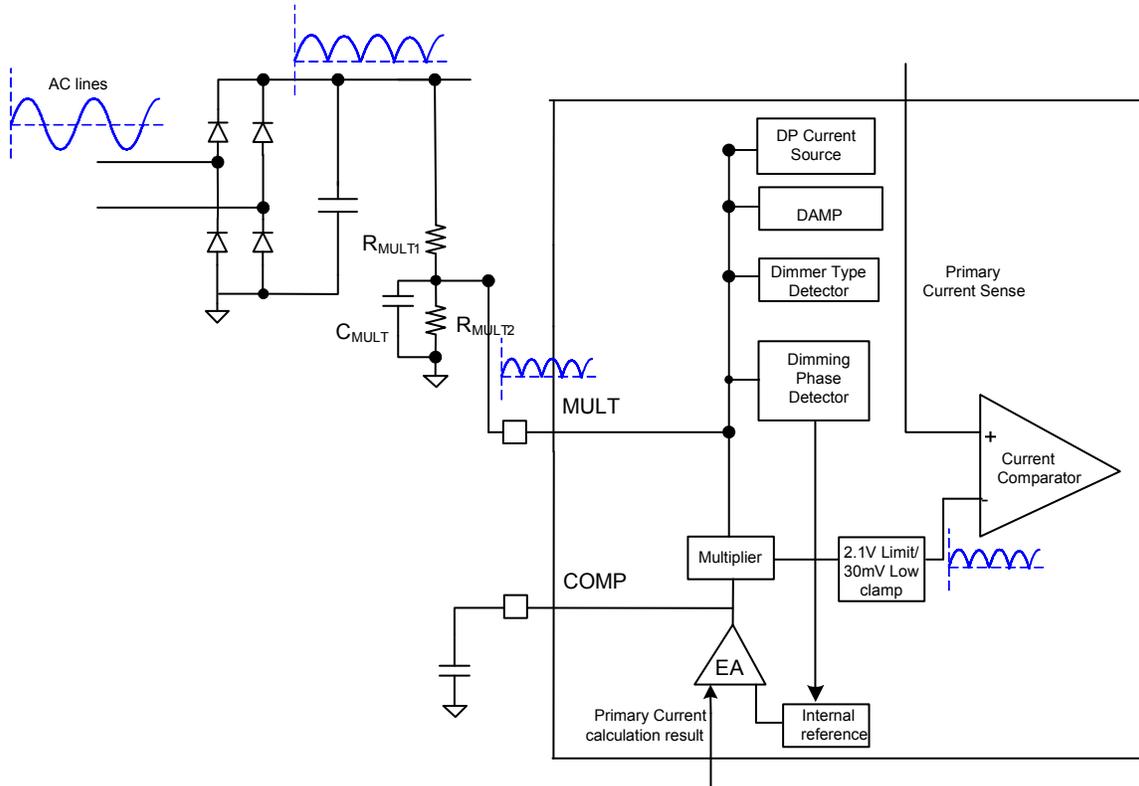
Figure 11: MULT Pin Circuit

The multiplier output is given by:

$$V_{multiplier\_out} = k \cdot V_{MULT} \cdot (V_{COMP} - 1.5)$$

Where k is the gain of the multiplier.

The MULT voltage determines the COMP voltage level for the system control loop. A low MULT voltage leads a high COMP voltage; a high MULT voltage means a low COMP voltage. In dimming conditions, the COMP voltage directly influences the dimming curve (see figure 9 and 10). High COMP voltage is benefit to dim deeper, low comp voltage is benefit to avoid leading edge dimmer prematurely turns off which may cause the LED flicker. In real applications, the COMP voltage is recommended to be set from 2.1 to 2.3V without dimmer connected at typical input voltage. Besides, the MULT voltage also determines the DP current turn on point, if DP current source turns on too earlier, the power loss of external MOSFET will significantly increase, especially at trailing edge dimming condition where the dimmer has not turned off. So, setting the MULT voltage value is very important. With lots of

experimental results, the MULT voltage is strongly recommended to be set at about 1-1.2V at typical input voltage.

The multiplier output has two clamps: The 2.3V high clamp is for primary cycle-by-cycle current limiting, the 30mV low clamp is to ensure a high gate output when bus voltage goes to zero crossing and reducing 130us auto start gate signals.

Pin2 (ZCD)

Figure 12: ZCD Pin Circuit

Figure 12 shows the ZCD pin circuitry. The ZCD pin connects to the auxiliary winding through a resistor divider (R_{zcd1}, R_{zcd2}). The ZCD pin integrates four functions: One detects the secondary-side–current zero-crossing condition by monitoring the auxiliary winding voltage for BCM; the second function is to implement the output over voltage protection by comparing the ZCD voltage to the internal 5.36V reference; the third function is to select the weak or strong DP current for leading edge dimming, the fourth function is the ZCD pin short circuit protection.

The internal gate turn-on signal triggers when the ZCD pin voltage falling-edge from the resistor divider goes below 0.3V, with a 0.6V hysteresis. The MP4033 switching frequency varies instantaneously with the input line voltage. To limit the maximum frequency and improve EMI and efficiency performance, the MP4033 employs an internal minimum OFF-time limiter of 5μs, as shown in 13. When the input line voltage crosses the zero point, the primary current is very small and cannot turn the secondary diode on, so the ZCD does not receive the turn-on signal for the next duty cycle. To avoid unnecessary IC shutdown, the MP4033 integrates an auto starter that starts timing when the MOSFET turns off. If the ZCD fails to send out another turn-on signal after 130μs, the starter will automatically send out a turn-on signal.
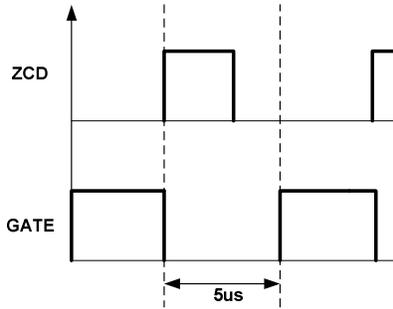
Figure 13: Minimum Off Time

Output over-voltage protection (OVP) works by detecting the auxiliary-winding voltage's positive plateau, which is proportional to the output voltage. Once the ZCD pin voltage exceeds 5.36V, the OVP signal triggers and latches, the gate driver turns off, and the VCC voltage decreases. When the VCC drops below 7V, the IC resets and restarts. The following equation estimates the output OVP set point:

$$V_{out\_OVP} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{zcd2}}{R_{zcd1} + R_{zcd2}} = 5.36$$

Where V_{out_OVP} is the output OVP setting voltage, N_{aux} is the turns of transformer auxiliary windings, and N_{sec} is the turns of secondary windings. Consider that the ZCD falling-edge detection delay time (when coupled with the ceramic bypass capacitor C_{ZCD}) increases with larger resistor values, reducing the output LED current: limit the delay time to <1.5µs. To avoid OVP mis-triggers caused by switch-off oscillation spikes, the MP4033 integrates an internal τ_{OVPS} blanking time for the OVP detection— typically 2.2µs (see 14).
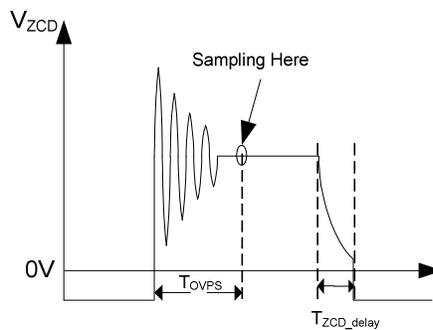

Figure 14: ZCD Voltage with Blanking Time

The weak or strong DP current for leading edge dimming is selected in ZCD pin at system start up. When VCC is charged to 10V, IC is enabled, an internal 200uA current source $I_{DP\_DET\_LD}$ will flow out ZCD to external resistance and generate a voltage on ZCD pin. If the voltage is higher than 1.2V over 200us, the strong DP current is selected, otherwise, the weak DP current is selected. Once the strong DP is selected, the 200uA current source will cut off, or the current source will cut off until COMP rise to 1.5V. So, if want to use strong DP current, the external resistance RZCD1//RZCD2 should meet the following condition:.

$$I_{DP\_DET\_LD} \cdot (R_{ZCD1} // R_{ZCD2}) > 1.2$$

Selecting for R_{ZCD1} and R_{ZCD2} also need take the ABS voltage and ZCD current into consideration. The ZCD pin's negative ABS voltage of ZCD pin is internally clamped at –7V and its source current is 5mA. Turning the primary MOSFET on applies a large negative voltage to the auxiliary winding, and may cause the ZCD pin to reach its negative voltage limit, so a diode is hired to clamp the negative voltage to -0.7V, and the R_{ZCD1} and R_{ZCD2} values must be large enough to limit the ZCD pin source current to below 5mA

The ZCD pin short circuit protection is used to protect the components over voltage damage when output is open load and ZCD is just short. If protection occurs if ZCD pin voltage is less than 0.1V over 33ms. The MP4033 shuts down the switching and latched until VCC dropping below UVLO and restarts.
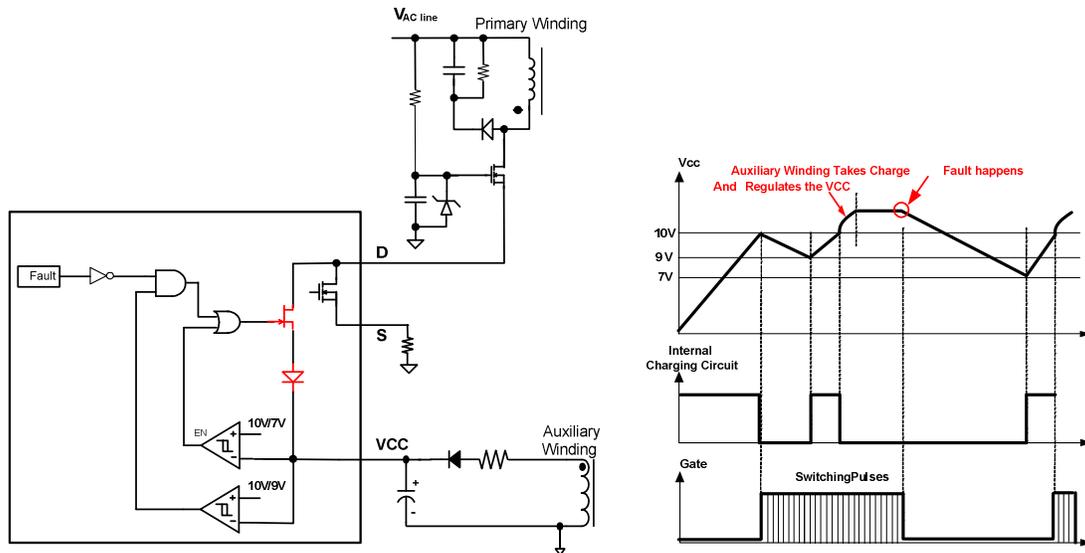
Pin3 (VCC)

Figure 15: VCC Circuit and Power Supply Flow-Chart

VCC powers both the internal logic circuit and the gate driver signal. Figure 15 shows the VCC circuit and the power supply flow-chart. The gate of high-side MOSFET charges quickly in the presence of an AC power supply, then VCC is charged through the internal charging circuit from the AC line. When VCC reaches 10V, the internal charging ceases, then the control logic and the internal main MOSFET begin to function. Then the auxiliary winding provides power.

The initial auxiliary-winding positive voltage is low and so the VCC level drops. Once VCC drops below a 9V threshold, the internal charging circuit triggers and to charge VCC to 10V again until the auxiliary winding can take over. If any fault occurs, the switching and the internal charging circuit will stop and latch, and VCC will drop. When the VCC drops to 7V, the internal charging circuit recharges to restart the device. A bulk capacitor connected to VCC determines the system start-up time and the VCC fall time under fault and TRIAC-dimming conditions. A large bulk capacitor results a long start up time but slows the VCC voltage drop under deep TRIAC-dimming conditions. Most applications call for a 22μF electrolytic capacitor.
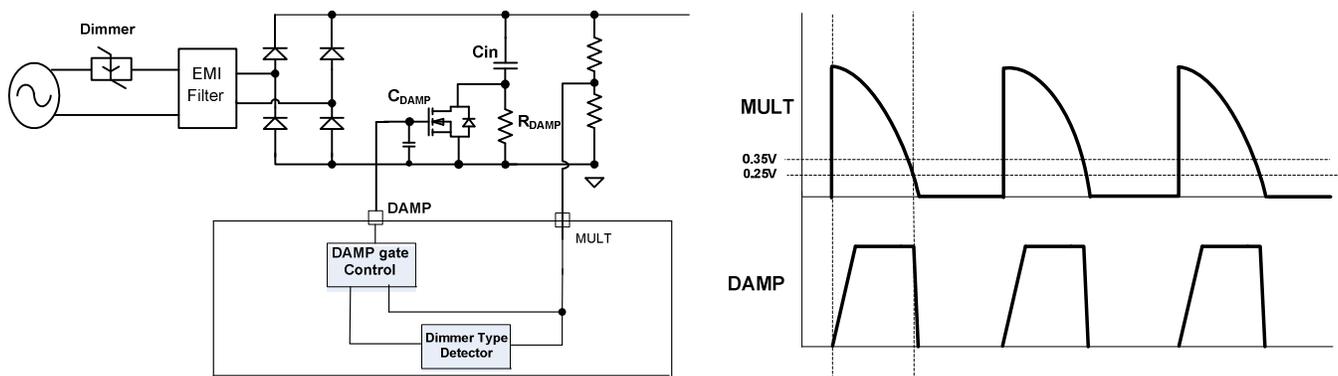
Pin4 (DAMP)

Figure 16: DAMP Pin Circuit and Gate Driver Logic

In phase-cut dimming application, when dimmer turns on, a significantly input current ring may occur due to the input current charging the input capacitance, if the current rings below the holding current, the dimmer may turn off prematurely and cause flicker. Since the input capacitor Cin is the dominant factor of the whole input capacitance, an active damping circuit is used to limit the Cin current ring. Shown in figure 16, the damping circuit consists of a damping resistor R_{DAMP}, a damping MOSFET and a switching speed adjusting capacitor C_{DAMP}.

The DAMP pin is the gate control of the damping MOSFET. If a leading edge dimmer or trailing edge dimmer is detected, the damping circuit is enabled to limit the inrush current when dimmer is turned on. If no dimmer is detected, the damping circuit is disabled by pulling up the damp pin voltage. The DAMP begins to be pull down when V_{MULT} decreases lower than 0.25V so that the damping resistor can be conducted when dimmer turns on at next cycle, when V_{MULT} increases to higher than 0.35V. the DAMP begins to be pull up and the damping resistor will be short by external MOSFET so that damping resistor only conducts for a short time at each cycle, this can be help reduce the damping resistor conduction power loss. The max pull up current source is 100µA while the max pull down current source is 400µA. The capacitor C_{DAMP} is used to adjust the damping MOSFET on/off speed. The cap value should be large enough to ensure the current ring has been effectively limited before the MOSFET is turned on, however, too large cap will cause the damping resistor conduct a long time which may bring unnecessary power loss. To be a trade off, the recommended value is 10nF.
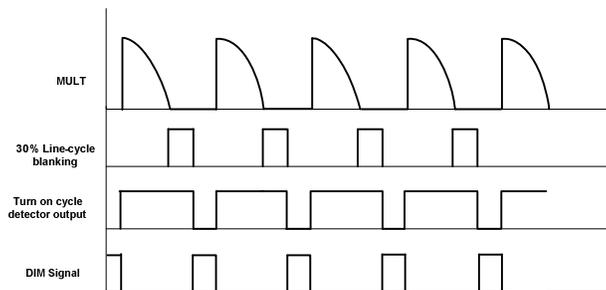
Pin5 (DIM)

Figure 17: DIM Signal Logic

The DIM pin outputs a driving signal for external MOSFET. The DIM signal is the reversal signal of the dimming turn on cycle detector output, shown in figure 17. It means the bigger dimmer turn on cycle, the smaller DIM turn on cycle, the smaller dimmer turn on cycle, the bigger DIM turn on cycle. With this logic, the DIM pin can easily support color temperature and brightness control for warm sunset dimming. The control circuit is shown in figure 18.
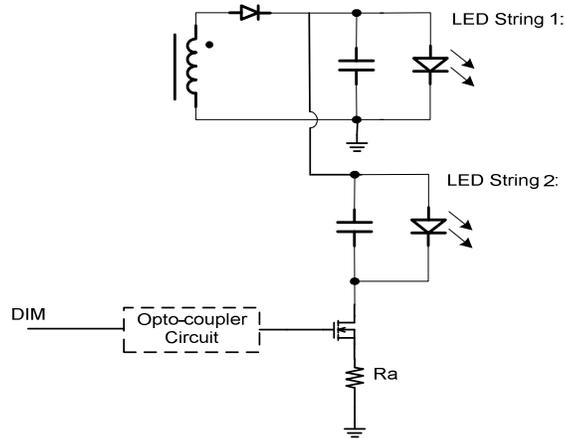
Figure 18: Color Temperature and Brightness Control Circuit

When the dimming turn on cycle detector detects the dimming duty is bigger than 70%, the DIM keeps constant low, the output current totally flows through the LED string 1, when output current begins to reduce after dimming, DIM outputs turn on cycle, the LED string 2 begins to distribute part of the output current, as the dimming cycle decrease, the LED string 2 will distribute more current which can achieve color temperature and brightness control, the accurate LED string 2 distribution current can be adjusted by changing the resistance of Ra.
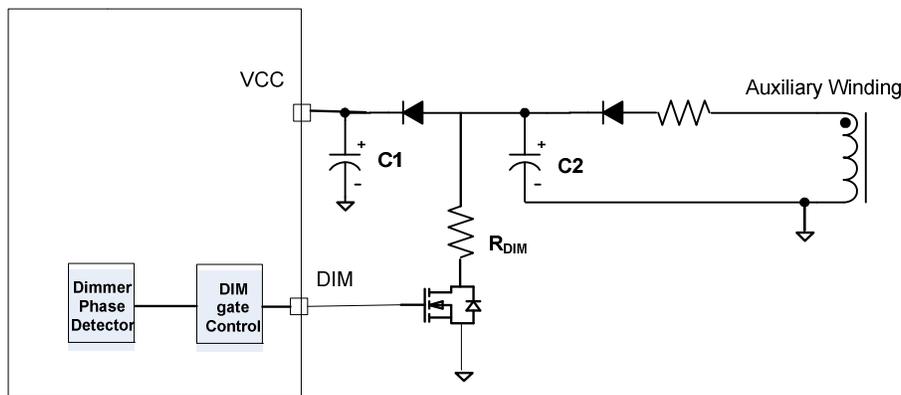

Figure 19: DIM Pin Circuit

Shown in figure 19, connecting a MOSFET to the rectified auxiliary winding output through a resistor R_{DIM} and E-cap C2 can form a dummy load to help distribute the output current, so the dimming depth can be enlarged. When dimmer turn on cycle goes small, the dummy load will distribute much current, so the output LED current will become smaller and the dimming depth is enlarged. The resistor RDIM determines the distribution current in the dummy load, a smaller RDIM can distribute more current and make deeper dimming depth, but also, it will significantly increase the power loss of RDIM, so, the value of RDIM is a trade off, 500 -1k Ω is recommended which can reduce the minimum output current about 20-10mA.

In real applications, if the dimming depth can meet the requirement and no need to do the warm sunset dimming, the DIM pin can be disconnected and leave as floating.

Pin6 (D)

Figure 20 shows the D-pin circuit. The D pin is the drain of the internal, main, low-side MOSFET. This pin also connects the internal VCC charging path to the source of the external high-side MOSFET. The dimming pull down current source is also connected from this pin to GND. Under normal conditions, the

internal, main, low-side MOSFET has a break-down voltage of 30V. When the MOSFET is OFF, the D voltage is the ratio of the high-side MOSFET and the low-side MOSFET voltages. The D voltage may exceed the break-down voltage and damage the device: Adding a diode from the D-pin to the high-side MOSFET gate helps to absorb the D-pin spike voltage.
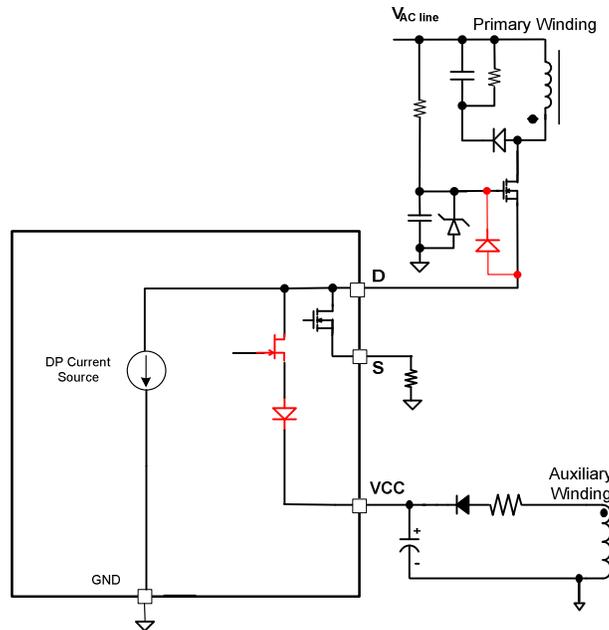
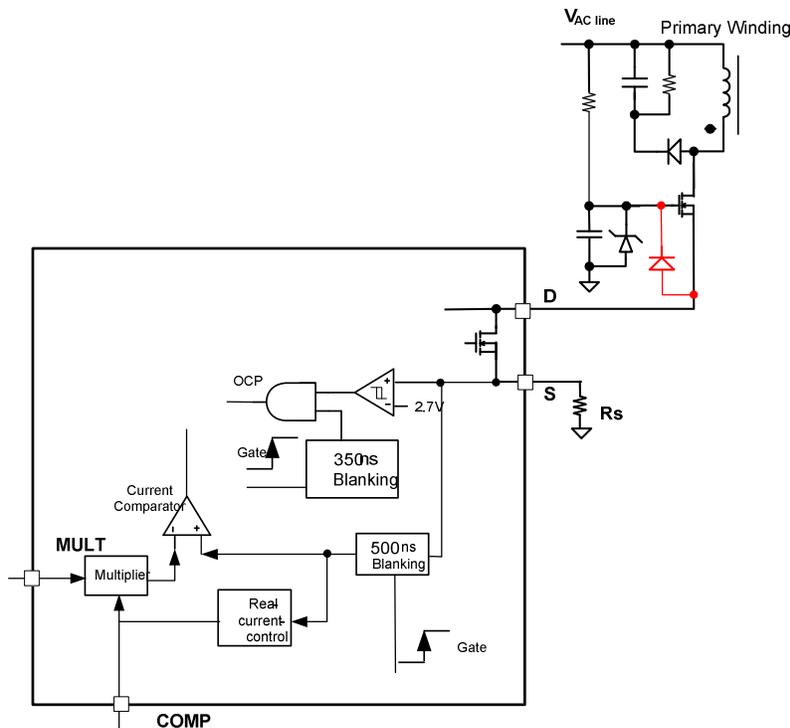**Figure 20: D Pin Circuit**

Pin7 (S)

Figure 21: S Pin Circuit

The S pin circuit is shown in figure 21. The S pin senses the primary-side current through a sensing resistor. The resulting voltage goes to the current comparator with the multiplier output to determine the MOSFET turn-off time, and the average-current calculation block to calculate the average primary-current value. A stable system loop produces a primary average value, $I_{p\_avg} \times R_S$, equal to the internal reference, V_{ref}. Combined with the equation on page 7, the output LED mean current can approximated as:

$$I_o = \frac{N \cdot V_{ref}}{2 \cdot R_s}$$

Where N is the turn ratio of the primary and secondary windings, V_{ref} is the internal reference voltage (typically 0.4V), and R_s is the sensing resistor connected between the main MOSFET source and GND.

An internal leading-edge blanking (LEB) unit between the S pin and the internal feedback avoids premature switching-pulse termination due to the parasitic capacitance discharging during turn-on. The internally-fed path is blocked during the blanking time. Figure 22 demonstrates the leading-edge blanking time.
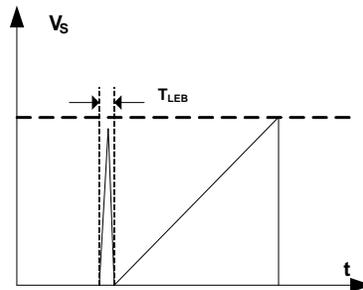

Figure 22`: Leading-Edge Blanking

The primary-side over-current protection is achieved by detecting the S peak voltage at gate turn on. If the S pin voltage rising to 2.5V at gate turn on interval, the primary-side over-current protection signal will be triggered and latched, the gate driver will be turned off and the VCC voltage dropped below the UVLO which will make the IC shut down, and the system restarts again. The primary-side over-current protection prevents device damage caused by extremely excessive current, like primary winding short. To avoid mis-trigger by the parasitic capacitances discharging when the MOSFET turns on, a LEB time is needed, this LEB time is relatively smaller than current regulation sensing LEB time, typical 350ns.

Pin8 (NTC)

The NTC pin provides tow functions. One is LED programmable thermal fold-back; the other is PWM dimming. The NTC pin block is shown as Figure 23.
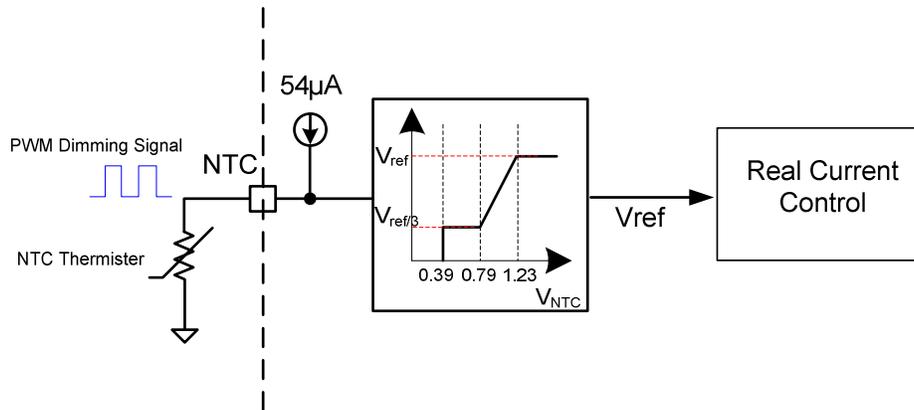
Figure 23: NTC Block

For the LED programmable thermal fold-back, a NTC thermistor for monitoring the ambient temperature can be directly connected from NTC pin to GND. The internal pull up current flows through the thermistor and generates a corresponding voltage on NTC pin. The NTC voltage controls the output LED reference. The relation is the curve shown in figure 23. When the NTC voltage is higher than 1.23V, the reference is maximum, when the NTC voltage drops from 1.23V to 0.79V, the reference changes from maximum to 1/3, when the NTC voltage changes from 0.879 to 0.39V, the reference is kept same, when the NTC drops below 0.39V, the reference will set to zero, the LED current outputs minimum.

For PWM dimming, applying the PWM dimming signal on NTC pin. The PWM signal high level need be higher than 1.23V, the low level should be lower than 0.39V, the frequency is recommended to be 10 times higher than the system loop bandwidth for a steady output. Normally, the frequency should be >200Hz. The output current will linearly change with the dimming duty from maximum to minimum. The minimum output current is caused by the IC minimum on time (equals LEB time), influenced by the input voltage, MOSFET turn off delay and the transformer inductance. etc. The higher input voltage, the bigger minimum current; the longer MOS turn off delay the bigger minimum current, so a small Q_G MOSFET is better for deep dimming.

Pin9 (GND)

The Ground (GND) pin provides the current return for both the control and the power signals. Connect the power and analog GNDs at this pin only for PCB layout. The power GND (PGND) provides the reference for the power switches, and the analog GND (AGND) for the control signals.

Pin10 (COMP)

Loop compensation pin. Connect a compensation capacitor from this pin to AGND. Use a low-ESR ceramic capacitor, such as X7R. The COMP pin is the output of the internal error amplifier. To limit the loop bandwidth <20Hz for good PFC performance, select a capacitor value between 2.2μF and 10μF. A larger capacitor results in a smaller COMP voltage ripple for better thermal, EMI, steady-state performance, but also means a longer soft-start time.

5. DESIGN EXAMPLE: 230VAC, DIMMABLE, HIGH-PERFORMANCE, 10W A19 LED LUMINAIRE DRIVER

A. SPECIFICATIONS

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage	V_{IN}	2 Wire	198	230	265	VAC
AC Line Frequency	f_{LINE}			50		Hz
Output Voltage	V_{OUT}	8 LEDs in series		24		V
LED Current	$I_{LED(MAX)}$	Without connecting dimmer		420		mA
Continuous Output Power	P_{OUT}			10.08		W
Efficiency	η	Full load, with out connecting dimmer	84%			
Power Factor				0.88		
Conducted EMI			Meets EN55015			
Harmonics			Meets IEC61000-3-2 Class C Limitation			
Surge			Meets IEC61547 surge requirement			

B. SCHEMATIC
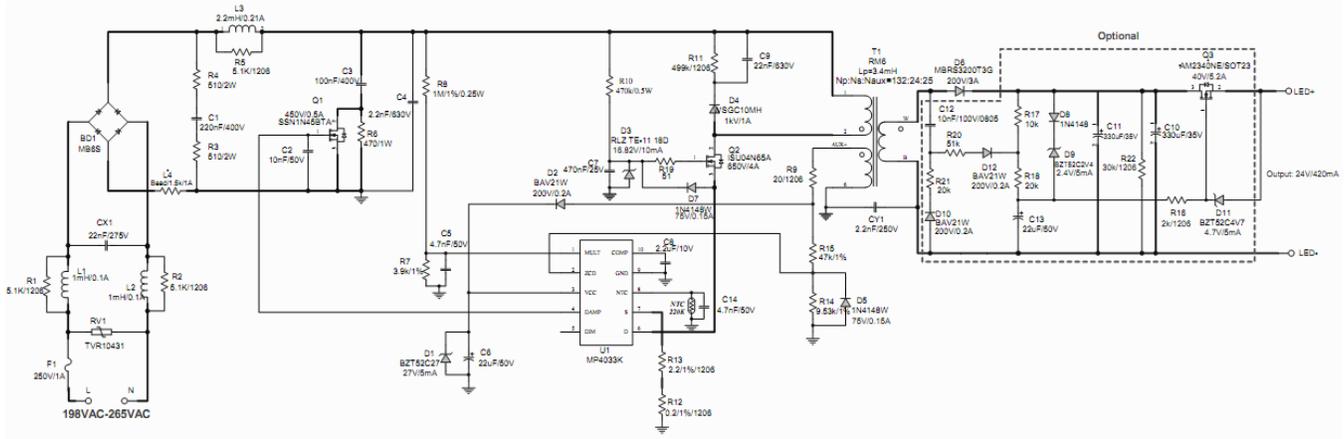
Figure 24: Example Application Schematic—10W A19 Luminaire Driver

C. TURN RATIO (N), PRIMARY MOSFET, AND SECONDARY-RECTIFIER–DIODE VOLTAGE RATING SELECTION

The following provides a design example given the following conditions:

- V_{ac_min}=198V

- V_{ac_max}=265V

- $V_{in\_max}= \sqrt{2} \cdot V_{ac\_max}$

- $V_{in}(V_{ac}, t) = \left| \sqrt{2} \cdot V_{ac} \cdot \sin(2 \cdot \pi \cdot f_{line} \cdot t) \right|$

Figure 25 shows a typical drain-source voltage waveform for the primary high-side MOSFET and he secondary rectifier diode. From the waveform, the maximum primary high side MOSFET Drain-Source

voltage rating $V_{\text{P-MOS\_max}}$ is

$$V_{P-MOS\_max} = V_{in\_max} + N \cdot V_o + 100 \tag{1}$$

Where 150V is the assumed maximum spike voltage, and is related to the RCD snubber.

The maximum secondary rectifier diode voltage rating, $V_{\text{DIODE\_max}}$, is

$$V_{DIODE\_max} = \frac{V_{in\_max}}{N} + V_o + 40 \tag{2}$$

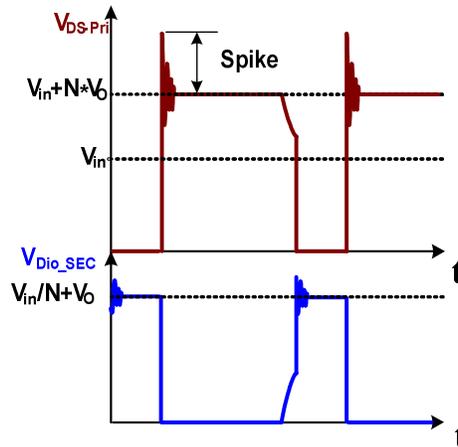Assuming the maximum voltage spike is 40V.

Figure 25: Drain-Source Voltage of the Primary MOSFET and the Secondary Rectifier Diode

Figure 26 shows the voltage rating curves of the primary MOSFET and secondary rectifier diode versus the turn ratio, N, based on equations (1) and (2). N can be determined by the required MOSFET and rectifier diode voltage ratings.

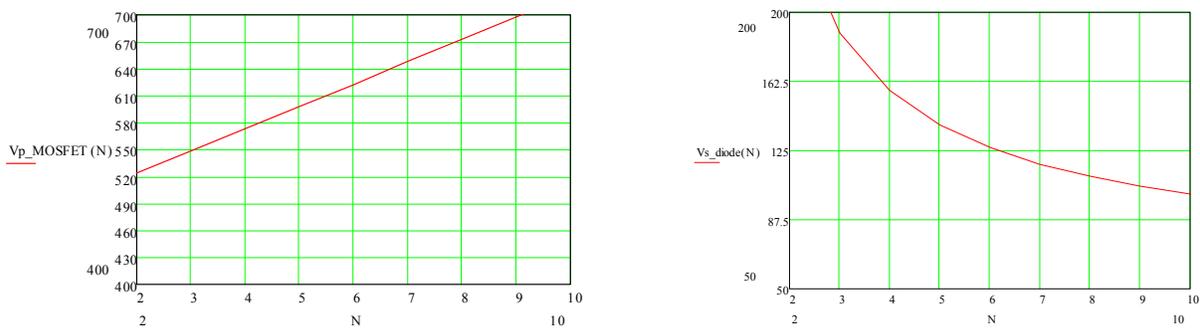**Figure 26: Voltage Ratings for the Primary MOSFET and the Secondary Rectifier Diode as a function of Turn Ration, N**

Some applications allow for N to be selected from within a range, which then requires the following considerations:

- A small N means a smaller τ_{on}/τ_{off} ratio, as per equation (5), which leads to a poor THD
- A large N leads to a large primary inductance and a physically larger transformer.

- According to the equation (33), a small N means a smaller current sensing resistor, which is better for fast pulling down the bus voltage when dimmer is off since the internal multiplier has a minimum clamp value, this is good for dimming performance.

Based on the stated conditions and the input voltage is 230VAC, the internal dimming pull down current will be selected with 40mA to confirm the bus voltage can be fast pulled down. Besides, for 230VAC input applications, the THD is relatively worse than 120VAC case, so a relatively bigger turn ration is selected, here choose N=5.5, so a 650V or 700V MOSFET and a 200V Schottky or fast-recovery diode suffices for this particular design example

D. TRANSFORMER DESIGN

Primary Inductance, L_P

It is possible to demonstrate that the MP4033 produces a constant ON-time over each line half-cycle, given:

- $V_S = R_s \cdot V_{in} \cdot \dfrac{\tau_{on}}{L_p}$, and

- $V_{Multipier} = K_1 \cdot K_2 \cdot V_{in} \cdot (V_{COMP} - 1.5)$, since

- $V_{CS} = V_{Multiplier}$,

- then $\tau_{on} = \dfrac{L_p \cdot K_1 \cdot K_2 \cdot (V_{COMP} - 1)}{R_s}$

Where L_p is the primary inductance, R_s is the current sensing resistor, K_1 is the multiplier gain, K_2 is the ratio of the MULT pin voltage vs. the line voltage, and V_{COMP} can a constant DC value when decoupled with a large COMP capacitor. The turn-off time varies with the instantaneous line voltage.

$$\tau_{on} = \frac{L_p \cdot I_p}{V_{in}(V_{ac}, t)} \tag{3}$$

$$\tau_{off} = \frac{L_p \cdot I_p}{N \cdot V_o} \tag{4}$$

for

$$\tau_{off}(\tau_{on}, V_{ac}, t) = \frac{V_{in}(V_{ac}, t) \cdot \tau_{on}}{N \cdot V_o} \tag{5}$$

Considering the τ_{off} limit within MP4033, the τ_{off} equation should be modified as:

$$\tau_{OFF}(\tau_{ON}, V_{ac}, t) = \left\| \begin{matrix} \dfrac{V_{in}(V_{ac}, t) \cdot \tau_{ON}}{N \cdot V_o} & \text{if } \dfrac{V_{in}(V_{ac}, t) \cdot \tau_{ON}}{N \cdot V_o} > 5\mu s \\ 5\mu s, \text{otherwise} \end{matrix} \right. \tag{6}$$

Figure 27 shows that the output LED current equals the average value of the secondary winding current during a half-line cycle. Equation (7) shows that the output current is the sum of the secondary current in each cycle to produce an average value.

$$I_o(a,b,T_{on},V_{ac},L_p) = \left\| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left\| sum \leftarrow sum + \frac{1}{2} \cdot \left\{ \left[\frac{V_{in}(V_{ac},t1+\tau_{on}) \cdot \tau_{on}}{L_p} \right] \cdot N \right\} \cdot \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on}) \right. \\ \left. t1 \leftarrow t1 + \tau_{on} + \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on}) \right. \\ \frac{sum}{b-a} \end{array} \right.$$
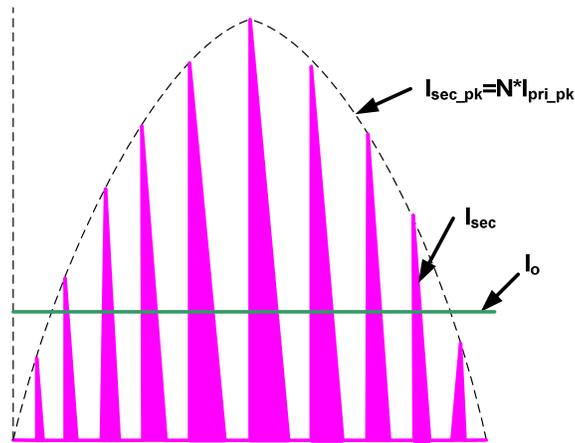(7)

Figure 67: Secondary-Side Current

Usually, the system will define a minimum frequency, f_{s_min}, at $V_{in} = \sqrt{2} \cdot V_{ac\_min} \sin(\frac{\pi}{2})$, and sets the minimum switching frequency, f_{s_min}=66kHz.

$$I_o(0, 0.01, \tau_{ON\_198V}, 198, L_p) = 0.42A$$
(8)

$$f_{s\_min} = \frac{1}{\tau_{ON\_198V} + \tau_{OFF}(\tau_{ON\_198V}, 198, 0.005)} = 66kHz$$
(9)

Combining (8) and (9) gets L_P=3,4 mH, τ_{ON_198}=4.7μs.

The maximum primary-peak current is:

$$I_{pk\_max} = \tau_{ON\_198V} \cdot \frac{V_{in}(198, 0.005)}{L_p} = 0.387A$$
(10)

When estimating L_P, the maximum operation frequency occurs when V_{in} approaches the zero crossing at 265VAC.

$$f_{s\_max} = \frac{1}{\tau_{ON\_265V} + \tau_{OFF}(\tau_{ON\_265V}, 265, 0)} = 115kHz$$
(11)

The Primary-Winding RMS Current:

$$I_{pri\_rms}(a,b,T_{on},V_{ac},L_p) = \begin{Vmatrix} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \begin{Vmatrix} sum \leftarrow sum + \left\{ \dfrac{1}{\tau_{on} + \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on})} \int_0^{\tau_{on}} (\dfrac{V_{in}(V_{ac},t1+\tau_{on}) \cdot t}{L_p})^2 \cdot dt \right\} \cdot \\ \left[\tau_{on} + \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on})\right] \\ t1 \leftarrow t1 + \tau_{on} + \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on}) \end{Vmatrix} \\ \\ \sqrt{\dfrac{sum}{b-a}} \end{Vmatrix}$$

(12)

The maximum primary RMS current is then:

$$I_{pri\_rms\_max} = I_{pri\_rms}(0,0.01,\tau_{ON\_198V},198,3.4 \cdot 10^{-3}) = 0.096\,\text{A} \tag{13}$$

The secondary winding RMS current:

$$I_{sec\_rms}(a,b,T_{on},V_{ac},L_p) = \begin{Vmatrix} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \begin{Vmatrix} sum \leftarrow sum + \left\{ \dfrac{N^4 \cdot V_o^2 / L_p^2}{\tau_{on} + \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on})} \int_0^{\tau_{off}(\tau_{on},V_{ac},t1+\tau_{on})} (\dfrac{V_{in}(V_{ac},t1+\tau_{on}) \cdot \tau_{on}}{N \cdot V_o} - t)^2 \cdot dt \right\} \cdot \\ \left[\tau_{on} + \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on})\right] \\ t1 \leftarrow t1 + \tau_{on} + \tau_{off}(\tau_{on},V_{ac},t1+\tau_{on}) \end{Vmatrix} \\ \\ \sqrt{\dfrac{sum}{b-a}} \end{Vmatrix}$$

(14)

The maximum secondary winding RMS current is:

$$I_{sec\_rms\_max} = I_{sec\_rms}(0,0.01,\tau_{ON\_198V},198,3.4 \cdot 10^{-3}) = 0.7\,\text{A} \tag{15}$$

The Transformer Core Selection

Select the transformer core based on output power for the entire operating frequency. Ferrite is common in flyback transformers. The core area product ($A_E \cdot A_W$)—which is the core magnetic cross-section area multiplied by the available window area for winding—typically provides an initial core-size estimate for a given application. The following provides a rough estimate of the required area product:

$$A_E \cdot A_W = \left(\frac{L_p \cdot I_{Pk\_max} \cdot I_{rms\_max}}{B_{max} \cdot K_u \cdot K_j} \right) cm^4 \qquad (16)$$

Where:

- K_u is winding factor which is usually 0.2 to 0.3 for an off-line transformer,

- K_j is the current-density coefficient (typically 0.06 A/m^2 for ferrite core),

- I_{Pk_max} and I_{rms_max} are the maximum peak current and RMS current of the primary inductor, and

- B_{max} is the maximum-allowed flux density under normal operation—which is usually preset to the saturation flux density of the core material (0.25T to 0.3T).

So the estimated minimum core area product is 0.039 cm^4.

Refer to the manufacture's datasheet to select an appropriate core with sufficient margins. Also, select a core shape to best meet the layout dimensions and audible noise limits. For this example, choosing an RM6 core provides better mechanical construction for suppressing audible noise compared to EE or EFD cores such that:

- A_E = 0.36 cm^2, A_W = 0.26 cm^2, $A_E \times A_W$ = 0.095 cm^4.

- The core magnetic path length: l_c = 2.86 cm

- The relative permeability of the core material: $\mu_\gamma = 2400$

Primary and Secondary Winding Turns

The transformer's primary size requires a minimum number of turns to avoid saturating a given core size. The normal saturation specification is E-t, or the volt-second rating. The E-t rating is the maximum voltage, E, applied over t seconds (The E-t rating is identical to the product of inductance, L, and the peak current). Equation (17) estimates the minimum value of N_P to avoid the core saturation:

$$N_P = \frac{L_p \cdot I_{pk\_max}}{B_{max} \cdot A_E} \times 10^4 \qquad (17)$$

Where:

L_p = the primary inductance of the transformer (H)

B_{max} = the maximum allowable flux density (T)

A_E = the effective cross sectional core area (cm^2)

I_{pk_max} = the maximum primary peak current (A)

Select B_{max} to be smaller than the saturation flux density, B_{sat}. B_{max} selection also requires taking the transformer's high-temperature characteristics into account because B_{sat} decreases as the temperature increases. B_{max} also influences the transformer's audible noise: a small B_{max} can reduce audible noise given a narrow window area. For PC40 material, the B_{max} is set to 0.27 to get N_P=132.

The number secondary windings is a function of the turn ratio, N, and primary turn count, N_P:

$$N_s = \frac{N_p}{N} = 24 \qquad (18)$$

Wire Size

Once the number of windings have been determined, select the wire size to minimize the winding conduction loss and the leakage inductance. The winding loss depends on the RMS current value, and the wire length and cross section.

Determine the wire size from the winding's RMS current:

$$S_{pri} = \frac{I_{pri\_rms\_max}}{J} = 1.59 \cdot 10^{-2} (mm^2) \tag{19}$$

$$S_{sec} = \frac{I_{sec\_rms\_max}}{J} = 1 \cdot 16^{-1} (mm^2) \tag{20}$$

Where J is the current density of the wire, which is typically 6A/mm^2.

Due to the skin effect and proximity effect of the conductor, select a wire diameter less than 2×Δd (where Δd is the skin-effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_{s\_min} \cdot \mu \cdot \sigma}} = 0.3 (mm) \tag{21}$$

Where μ is the conductor's magnetic permeability, which is usually equal to the permeability of a vacuum for most conductors (i.e. $4\pi \times 10^{-7}$ H/m). σ is the wire's conductivity (typically 6×10^7 S/m at 0° for copper, which increases with temperature).

If the requires wire diameter exceeds 2×Δd, use multiple strands of thinner wire or Litz wire to minimize the AC resistance. Select enough strands such that the effective cross sectional area meets the current density requirement.

In offline isolated applications, the whole system needs to pass the Hipot test, which requires taking the primary to secondary isolation distance into consideration. Small power systems typically use triple-insulated wire (TIW) as the secondary winding wire to enhance the isolation distance. Using TIW negates the need for a retaining wall and conserves the transformer window area.

This example uses 0.15mm×1 wire for the primary winding, 0.35mm×1 T.I.W for the secondary winding, so the wire area for the primary winding is S$_1$=1.77×10^{-2} mm^2, and for the secondary winding it is S$_2$=0.97×10^{-1} mm^2.

Auxiliary Winding Wire Size

The auxiliary winding's current requirement is relatively small because it primarily provides power to VCC and detects the current zero crossing for boundary-mode operation. The auxiliary winding's output DC voltage is proportion to the output LED voltage with a turn ratio of N$_{aux}$/N$_s$. VCC requires high stability so that the IC can continue to function even when dimming function goes very low. Most applications VCC to go as high as 25V. Given an LED output voltage of 24V, select N$_{aux}$ as N$_{aux}$=25/24×N$_s$, so N$_{aux}$=25 for a 0.15mm wire.

Window-Area Fill-Factor Calculation

After selecting appropriate wire sizes, check whether the core window area can accommodate the windings. Calculate each winding's required window area, respectively, then add the areas together—be sure to take the interwinding insulation and spaces into consideration. The fill factor—the winding area relative to the whole core window area—should be well below 1 due to these interwinding insulation and spaces between turns. Select a fill factor no greater than 20%.

$$\frac{N_p \cdot S_1 + N_s \cdot S_2 + N_{aux} \cdot S_3}{A_{W\_RM6}} = 0.196 < 0.2 \tag{22}$$

If the required window area exceeds the selected one, reduce either the wire size or use a larger core. However, reducing the wire size increases the transformer copper loss.

Air Gap

With a selected core and winding turns, the core air gap is approximately:

$$G = \mu_0 \cdot A_E \cdot \frac{N_P^{\,2}}{L_p} - \frac{l_c}{\mu_r} = 0.23\,(mm) \tag{23}$$

Where A_E is the cross sectional area of the selected core, μ_0 is the permeability of vacuum which equals $4\pi \times 10^{-7}$ H/m., L_p and N_P is the primary winding inductance and turns respectively, l_c is the core magnetic path length and μ_r is the relative magnetic permeability of the core material.

Instructions for Transformer Manufacturing

The coupling between the transformer primary side and the secondary side must be as tight as possible to minimize leakage inductance. This can be accomplished be interleaving the primary and secondary windings during transformer manufacture, as shown in Figure 28. Start with the winding connected to the drain of the high-side MOSFET first, followed by the auxiliary winding, and then the secondary winding to isolate the secondary wind from the drain to reduce parasitic capacitance and to improve the CM EMI. To meet the safety requirements, separate the transformer's primary side and secondary side and keep a safe creepage distance of at least 6mm. Do not directly connect the auxiliary winding pin (AUX+) and the two secondary winding pins (W and B) to the transformer pins. Instead, use jumpers and connect externally, as per Figure29.
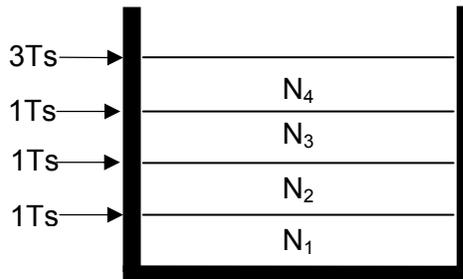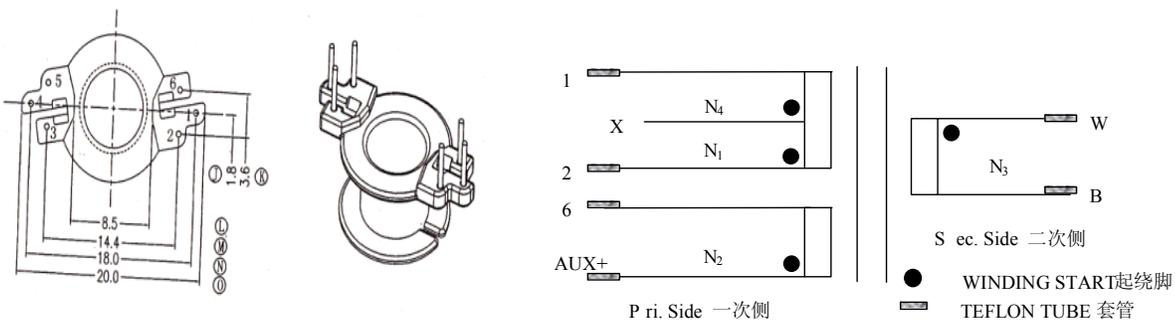

Figure 28: Transformer Winding Diagram

Figure 29: Transformer Pin Out and the Connection Diagram

E. INPUT EMI FILTER (L1, L2, L3, CX1, CY1, C3, C4)

The input EMI filter is comprised of L1, L2, L3, CX1, with the Y-class capacitor, CY1, and input film capacitor, C4. The EMI filter has two stages with –80dB attenuation for the DM noise. Soldering the L2 and L3 inductors to the L and N lines, respective, also acts as a CM noise filter. Select component values to pass EMI test standards, as well as to account for the power factor and dimming performance. The input capacitance plays the primary role: a small input capacitance increase the power factor, decreases the inrush current for leading edge dimming and better for pulling down the bus voltage at trailing edge dimmer off, so select a relatively small X capacitor. The capacitor C4 is used to help improve the high frequency EMI performance, like CDN test.

F. INPUT BRIDGE (BD1)

The input bridge can use standard, slow-recovery, low-cost diodes. When selecting diodes, take into account these three items: the maximum input RMS current; the maximum input-line voltage; and thermal performance. The maximum input-line voltage occurs during surge conditions, where the surge voltage across the line may exceed 600V. This example uses MB6S as the BD, with a 600V, 0.5A rating.

G. INPUT CAPACITOR (C3)

The input capacitor, C3, mainly provides the transformer's switching frequency magnetizing current. The maximum current occurs at the peak of the input voltage. Limit the capacitor's maximum high-frequency voltage ripple to 10%, or the voltage ripple can cause the primary peak current to spike and worsen both the power loss and the EMI performance.

$$C3 > \frac{I_{pk\_max} - \sqrt{2}I_{pri\_rms\_max}}{2 \cdot \pi \cdot f_{s\_min} \cdot V_{ac\_min} \cdot 0.1} = 30nF \qquad (24)$$

Input capacitor selection requires taking into account the EMI filter, the power factor, and the surge current at the dimming turn-on time. A large capacitor improves EMI, but limits the power factor and increases the inrush current. This example uses a 100nF, 400V, film capacitor.

H. PASSIVE BLEEDER (C1, R3, R4) AND ACTIVE DAMPER (Q1, C2, R6)

Since the LED lamp impedance is relatively large, significant ringing occurrs at leading edge TRIAC dimmer turn on due to a inrush current charging the input capacitance (shown in Figure 30). The ringing may cause the TRIAC current fall below the holding current and turn off the TRIAC, which can cause flickering.
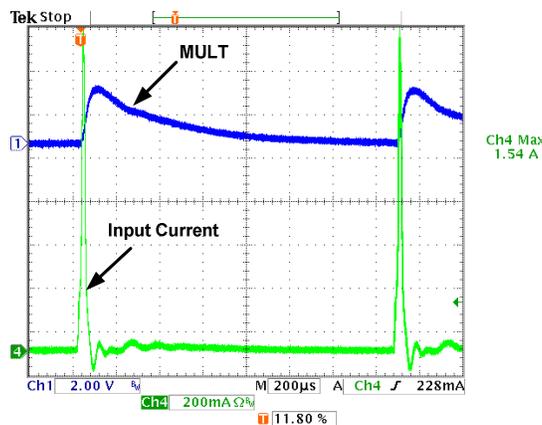

Figure 30: Input Current Ringing at the TRIAC's Leading-Edge Turn-On Period

This example incorporates both a passive bleeder and an active damper circuit to address this issue. The passive bleeder consists of an RC circuit (C1, R3, and R4) installed across the input line right after the bridge rectifier. Select a bleeder capacitance larger than the input capacitor,,C3, and X capacitor, CX1, to limit the bleeder current-ringing frequency below the C3 and CX1 current ringing, as shown in; Figure 31, the current through the TRIAC rises when the TRIAC turns on. However, increasing the capacitance increases the power dissipation and therefore decrease efficiency. Use the minimum acceptable value.

The bleeder resistor limits the bleeder current and damps the input current. The resistance requires fine-tuning: large resistors limit bleeder functionality, while small resistors limit damping and can lead to high-amplitude bleeder-current ringing. This examples uses 220nF, a total of 1.02kΩ, and a power rating of 2W.
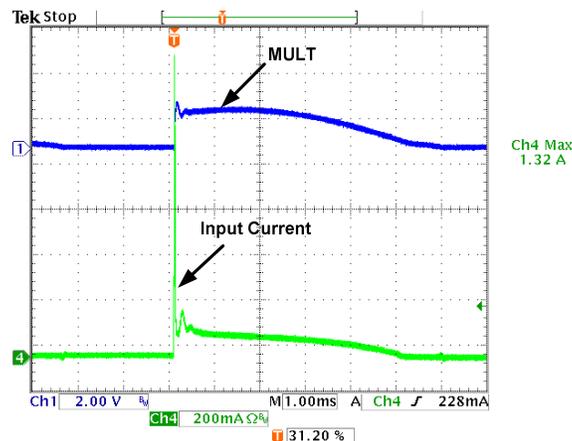

Figure 31: Input Ringing with Passive Bleeder

However, Only the passive bleeder is not enough to maintain conduction in the TRIAC for many kinds of different TRIACs, then a damper is needed. The purpose of the damper is to limit the inrush current that charges the input capacitance at TRIAC turning on. There are tow kinds of dampers, passive and active. Passive damper is simple, only need hire a resistor in series with the AC input line, limited by the power dissipation, values can not be large, the values are typically from 10 to 100Ω.The passive damper may suit for power less than 5W and the effective is strongly limited by the efficiency requirement. For higher power or higher efficiency design, an active damper is required. The MP4033 integrates the damping control circuit, only need 3 external components Q1, C2, R6. Since the input capacitor C3 has the biggest capacitance, the damping circuit is connected to C3. Resistor R6 is used for limiting the inrush current and the value can be much higher than the passive case. The capacitor C2 is used to adjust the damping operation time and determine when the MOSFET turns on and short R6. Increasing the damping operation time by increasing the value of capacitor C2 can improve the damping result, but cause more power dissipation. Here choosing a 10nF capacitance for C2, the MOSFET Q1 should select a higher voltage rating than V_{in_max} and current conduction capability bigger than $2*I_{pri\_RMS\_MAX}$.

I. OUTPUT CAPACITOR (C10, C11)

The output voltage ripple has two components: the switching-frequency ripple associated with the flyback converter, and the low-frequency ripple associated with the input-line voltage (100Hz). Selecting the output bulk capacitor depends on the output current, the allowable overvoltage, the desired voltage ripple, and with an LED load the LED current ripple. This example has a load of 8 LEDs in series, a 420mA output current, and a current ripple set within 40% without dimming. Since the LED impedance is not resistive, the output voltage ripple refers to the LED V-I characteristics as provided by the LED manufacturer to design the output voltage ripple within 2.5%.

The maximum RMS current of the output capacitor is:

$$I_{out\_cap\_rms\_max} = \sqrt{I_{sec\_rms\_max}{}^2 - I_{o\_rms}{}^2} \qquad (25)$$

Where I_{o_rms} is the output RMS current and $I_{sec\_rms\_max}$ is the maximum secondary RMS current from equation (15). Design the maximum RMS current to be smaller than the capacitor's RMS current specification.

The maximum switching voltage ripple occurs at the peak of the minimum-rated input line voltage, and the ripple (peak-to-peak) can be estimated by:

$$\Delta V_{o\_swtiching} = \frac{I_{o\_\max} \cdot \tau_{off}(\tau_{on\_198V}, 198, 0.005)}{C_{out}} + (I_{sec\_pk\_\max} - I_{o\_\max}) \cdot R_{ESR} \qquad (26)$$

Where I_{o_max} is the maximum instantaneous output LED current with a mean value of 420mA plus a 20% peak ripple; $\tau_{off}(\tau_{on\_198V}, 198, 0.005)$ is the turn-off time at the peak of the minimum-rated input line, R_{ESR} is the ESR of output capacitor (typically 0.03Ω per capacitor), and $I_{sec\_pk\_max}$ is the maximum peak current of the secondary winding.

Estimate the maximum low-frequency ripple (2x the line frequency, 100Hz) from the capacitor impedance and the peak capacitor current (I_{o_max}).

$$\Delta V_{o\_line} = I_{o\_\max} \sqrt{\frac{1}{(2\pi \cdot 2f_{line} \cdot C_{out})^2} + R_{ESR}{}^2} \qquad (27)$$

Based on this equation, the 100Hz low-frequency ripper dominates the output voltage ripple. Set $\Delta V_{o\_line} = 0.6V$ for C_{out}=668µF. Selecting 330µF/35V bulk capacitors in parallel minimizes the ESR and distributes the capacitor RMS value. Add a 30kΩ pre-load resistor to discharge the output voltage under open-load conditions.

J. RCD Snubber (R11, C9, D4)

The peak voltage across the high-side MOSFET at turn-off includes the instantaneous input line voltage, the voltage reflected from the secondary side, and the voltage spike due to leakage inductance. The RCD snbber (shown in Figure 32) protects the MOSFET from over-voltage damage by absorbing the leakage inductance energy and clamping the drain voltage. The values of C9 and R11 depend on the leakage inductance energy dissipated by the RC network during each cycle. Figure 33 shows the primary high-side MOSFET output voltage ripple and the snubber capacitor at point A during the turn-off interval.
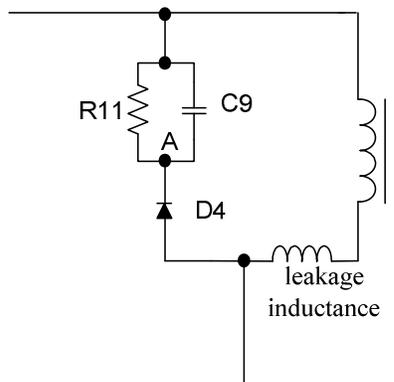

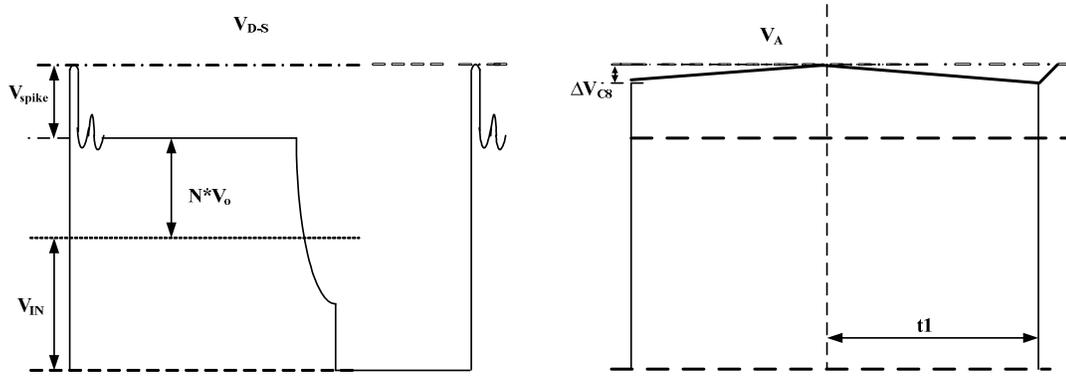**Figure32: Primary-Side RCD Snubber**

Figure 33: A Point Voltage with a High-Side MOSFET Drain Voltage and Snubber Capacitor

Estimate the energy stored in the leakage inductor at the maximum input voltage as:

$$E_{Lk\_max} = \frac{1}{2} \cdot L_{leakage} \cdot I_{pk\_V_{in\_max}}{}^2 \tag{28}$$

Where $I_{pk\_Vin\_max}$ is the peak current for the primary side at the maximum input voltage. Assume all the leakage inductance energy transfers to the snubber capacitor. The secondary relationship is:

$$E_{Lk\_max} = \frac{1}{2} \cdot C9 \cdot \left[(V_{in\_max} + N \cdot V_o + V_{spike})^2 - (V_{in\_max} + N \cdot V_o + V_{spike} - \Delta V_{C9})^2 \right] \tag{29}$$

Where V_{spike} is the spike voltage clamped by the RCD snubber, ΔV_{C9} is the snubber capacitor's voltage change caused by the leakage inductance.

Assuming ΔV_{C9} << V_{spike}, and the $\frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C9} < \tau_{Vin\_max}$,

$$\Delta V_{C9} = V_{spkie} \cdot (1 - e^{-\frac{t1}{R11 \cdot C9}}) \tag{30}$$

Where t1 is the time $\tau_{Vin\_max} - \frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C9}$, and τ_{Vin_max} is the switching period at V_{in_max}.

To select R11, take into account the secondary-side reflecting voltage because it contributes to the snubber resistance after the MOSFET turns off. Select R11 to be large enough to reduce the reflecting voltage loss, but avoid contributing to a clamping voltage that exceeds the selected MOSFET based on equation (1).

Based on equations (6), (7), and (10), $I_{pk\_Vin\_max}$=0.35A, τ_{on_265V}=3.16μs, and τ_{vin_max}=12.8μs. The leakage inductance is estimated as 1% of the primary inductance, 34μH. Select the snubber parameters: C9=22nF, R11=499kΩ for V_{SPIKE}=100V and $\Delta VC1$=0.11V.

Select a snubber capacitor with a higher voltage rating than the spike voltage, and a diode voltage rating higher than V_{in_max} + V_{spike}—use a normal-recovery diode, such as a WSGC10MH, which has better EMI performance than a fast-recovery diode. Given the difficulty in theoretically calculating the power dissipation of the snubber resistor R11, monitor the resistor's thermal performance during testing to determine the final appropriate value.

K. HIGH-SIDE MOSFET GATE DRIVER (R10, R19, C7, D3, D7)

The rectified line voltage initially charges the high-side MOSFET gate through R10. C7 To stabilizes the gate voltage when line voltage goes low; typically 470nF suffices for most dimming conditions. Zener diode, D3, clamps the gate voltage to avoid damaging the MOSFET. Select a clamping voltage that exceeds 16V to ensure the VCC voltage can charge to 10V through point D. R10 and C7 introduces a delay; reducing R10 reduces the delay, but increases power dissipation. For C7 = 470nF, select R5 in the 499kΩ-to-1MΩ range for a delay time of less than 40ms— much shorter than the system start-up time. The gate driving resistor R19 is used to limit the driving speed to improve the radiation EMI. 20-100Ω is the typical range, if the EMI performance can pass, the value should be as small as possible to reduce the MOSFET switching loss, here choose 51Ω.

The diode D7 connects the internal low side MOSFET drain to high side MOSFET gate. So the oscillation spike voltage in D pin can be clamped at 16.8 V when internal MOSFET is switching off and help maintain the gate driver voltage by feedback the oscillation energy in deep dimming duty.

L. VCC POWER SUPPLY (R9, C6, D1, D2)

Page 17 shows the detailed VCC operation timing sequence. After system starts up, the auxiliary winding takes over the VCC power supply through a rectifying diode (D2) with a current-limiting resistor (R9). The bulk capacitor (C6) stabilizes the VCC voltage to limit the ripple—most applications use 22µF. Since the VCC maximum voltage is 30V, use a Zener diode (D10) to protect the VCC pin under open-load conditions, and to minimize the power dissipation. Set the clamping voltage as high as 27V. Use a relatively small current-limit resistor (R9) because of the limited power dissipation. Use the following equation to determine the D2 voltage rating:

$$V_{D5} > VCC_{max} + \frac{N_{aux}}{N_p} \cdot V_{in\_max} + V_{aux\_negtive\_spike} \tag{31}$$

Where VCC_{max} is the maximum VCC voltage, in this case, VCC_{max}= 27V, N_{aux} and N_p are the auxiliary winding and primary winding turns, $V_{aux\_negtive\_spike}$ is the maximum negative spike on auxiliary winding, in this case, $V_{aux\_negtive\_spike}$= 40V, so D2 need a voltage rating higher than 100V.

M. ZCD AND OVP DETECTOR (R14, R15, D5)

Refer to information starting on page 1515 for additional information.

The resistor divider, R14 and R15, sets the OVP threshold:

$$V_{o\_ovp} \cdot \frac{N_{aux}}{N_s} \cdot \frac{R_{14}}{R_{14} + R_{15}} = 5.36V \tag{32}$$

Where V_{o_ovp} is the output OVP voltage, N_{aux} is the number of transformer auxiliary winding turns, and N_s is the number of transformer secondary winding turns. Given N_{aux}=25, N_s=24, set V_{o_ovp}=30V for R14/R15=4.83. Consider the leading edge DP current source select 40mA, R14//R15 should be > 6kΩ, select R14=9.53kΩ, R15=47kΩ. Add a diode D5 in parallel with R14 to clamp the ZCD minus voltage to -0.7V since the ZCD pin minimum minus voltage is just -7V.

N. MULT PIN RESISTOR DIVIDER (R7, R8, C5)

The MULT pin resistor divider needs to be carefully tuned because the MULT voltage determines the COMP voltage level and influence the dimmer type detection result which directly influence the dimming performance. Test the estimated divider values with different types of dimmers to determine accurate resistor values: this example uses R8=1MΩ and R7=3.9kΩ for a COMP level of 2.2V at 230VAC input. The C5 is absorbs the switching frequency ripple on the ZCD voltage for accurate dimming-phase and dimmer type detection. Increasing the capacitance can further smooth the ZCD voltage, but increase the input-line voltage phase shift and cause diminish the power factor. Here, C5 is tuned to 4.7nF.

O. CURRENT SENSING RESISTOR (R12, R13)

As described on page 21, approximate the current sensing resistor with the following equation:

$$R_s \approx \frac{V_{ref} \cdot N}{2 \cdot I_o}$$

(33)

Where N is the turn ratio of primary winding to secondary winding, V_{ref} is the feedback reference voltage (typically 0.414V), and R_s is the sense resistor between the S pin and GND.

Equation (33) describes R_S under BCM, but the device may enter DCM during a line cycle due to the minimum off-time limitation and a missing ZCD turn-on signal. The DCM influences and other factors also influence the output current through primary-side control, such as the IC's internal logic delay, the transformer inductance, and the ZCD detection delay. These factors make estimating the output current difficult, and why designing the current sensing resistor last provides allows for better fine-tuning for the required output current.

In this case, the sensing resistor is tuned to 2.4Ω, using 2.2Ω/0.25W resistor in series with 0.2Ω/0.25W.

P. NTC SET (NTC, C14)

The NTC thermistor should be selected to meet the required resistance with the temperature variation, this can be refer to the thermistor manufacture's datasheet. The MP4033 NTC function voltage is started from 1.2V, the internal pull up current source is 60uA. So corresponding resistance is

$$1.2V / 60uA = 20k\Omega$$

(34)

Here choose MURATA thermistor NCP18WM224E03R8, 25℃ typical resistance is 220kΩ. with 80℃ reducing to 20kΩ.

Q. SECONDARY SIDE RIPPLE SUPPRESSOR CIRCUIT

For dimming LED lighting application, a single stage PFC converter needs large output capacitor to reduce the current ripple whose frequency is double of the AC lines. And in deep dimming condition, the LED would shimmer caused by the dimming on duty which is not all the same in every line cycle. What's more, the Grid has noise or inrush which would bring out shimmer even flicker. Figure 34 shows a ripple suppressor circuit, which can shrink the LED current ripple obviously and avoid shimmer happening.
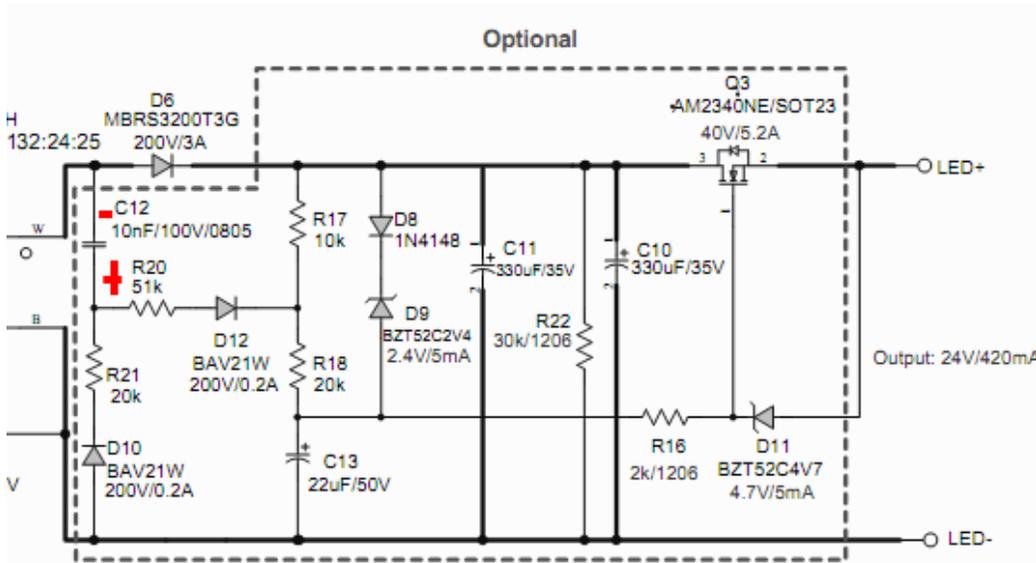
Figure 34: LED Current Ripple Suppressor Circuit

The current ripple suppressor circuit consists of C12, C13, D8, D9, D10, D11, D12, Q3, R16, R17, R18, R20, R21. Regardless of R20, D12, the capacitor C13 will be charged by D6, R17, R18 and gets a mean value equals to output voltage Co to drive the MOSFET Q3, the Q3 works in variable resistance area, if C13 is large enough to get a steady voltage, the output voltage is also steady, so the LED current will be smooth. But this will lead a big power loss for Q3 since it keeps working in variable resistance area. Considering the shimmer always happens in small dimming on duty, it can let the Q3 firstly work in fully switching status in big dimming on phase. This can be achieved by adding a bias voltage on C13. The C12 voltage can be used, when primary side MOSFET turns on, the C12 is charged by D10 and R21, so the C12 also gets a mean value with the reversal direction of C13, then connects C12 to C13 with R20 and D12, when primary MOSFET turns off, C12 also can charge C13 and let C13 get a bias voltage. The C12 mean voltage is related to the dimming on duty, when dimming on duty goes small, the mean voltage will also become small. By adjusting the R20 resistance to tune the bias voltage on C13, make the bias voltage Vbias higher than the Q3's Vth in big dimming on duty so that the Q3 can work in fully switching mode to reduce power loss, when dimming on duty goes small, make the bias voltage lower than Vth so that the Q3 works in variable resistance area to suppress the current ripple. The D8, D9 is used to fast charge up C13 to avoid overshot at start up, the R16, D11 is used to clamp the gate voltage of Q3 to a safe level when output is short. Figure 35 shows the LED current in different dimming on duty with current suppressor circuit.
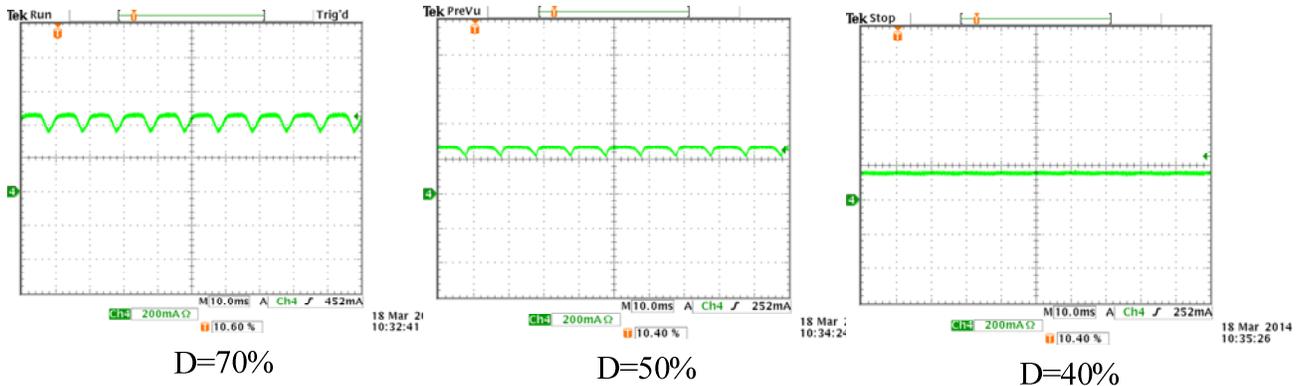

Figure 35: LED Current with Ripple Suppressor Circuit

R. LAYOUT GUIDELINE

- Design the main power flow path as short as possible using wide wires. Design the sense resistor GND return to directly connect to the input capacitor, C4. Use the largest-possible cooper pour for the power devices for good thermal performance.

- Separate the power GND and the analog GND, and connect them together only at an IC GND pin.

- Placed the IC pin components as close as possible to the corresponding pins, especially the MULT pin components.

- Isolate the primary side and the secondary side by at least 4mm to meet safety requirements and the Hipot test. Tune the transformer installation position to keep the primary side far away from secondary side.

- In order to pass the surge test, separate the input high voltage wire from other components and GND. Better to connect R10 and R8 to the rectified input line for the DIP package.

- On the secondary side, place the rectifying diode as close as possible to the output filter capacitor, and use a short trace from the transformer output return pin to the return point of the output filter capacitor.

S. BOM

Item	Qty	RefDes	Value	Description	Package	Manufacturer	Manufactuer_P/N
1	1	BD1	MB6S	BRIDGE, 600V, 0.5A	SOIC-4	Taiwan Semiconductor	MB6S
2	1	C1	220nF/450V	CBB,450V	DIP	Fala	C222S224K31C000
3	1	C2	10nF/50V	Ceramic Cap,X7R,50V	0603	muRata	GRM188R71H103KA01D
4	1	C3	100nF/400V	104/400v	DIP	Panasonic	ECQE4104KF
5	1	C4	2.2nF/630V	Ceramic Cap, 630V，X7R	1206	muRata	GRM31BR72J222KW01L
6	1	C5	4.7nF/50V	Ceramic Cap,X7R,50V	0603	muRata	GRM188R71H472KA01D
7	1	C6	22uF/50V	Electrolytic Capacitor;50V;Electrolytic	DIP	Jianghai	CD281L-50V22
8	1	C7	470nF/50V	Ceramic Cap,X7R,50V	0603	muRata	GRM188R71E474KA12D
9	1	C8	2.2uF/10V	Ceramic Cap,10V,X7R	0603	muRata	GRM188R71A225KE15D
10	1	C9	22nF/630V	Ceramic Cap, 630V，X7R	1206	TDK	C3216X7R2J223K
11	2	C10,C11	330uF/50V	Electrolytic Capacitor, 50V, Electrolytic	DIP	JiangHai	CD263-50V330
12	1	C14	4.7nF/50V	Ceramic Cap,50V,X7R	0603	muRata	GRM188R71H472KA01D
13	1	CX1	22nF/275V	X Capacitor,275V	DIP	Kaili	PX223K3IB19L270D9R
14	1	CY1	2.2nF/4000V	Y Capacitor,4000V	DIP	Hongke	JNK12E222MY02N
15	1	D1	BZT52C27	Zener Diode, 27V, 2mA	SOD-123	Diodes	BZT52C27
16	1	D2	BAV21W	Diode;200V;0.2A;	SOD-123	Diodes	BAV21W-7-F
17	1	D3	RLZ TE-11 18D	Zener DIODES/16.82V, 10mA	SOD-123	ROHM	RLZ TE-11 18D
18	1	D4	WSGC10MH	Diodes,1000V,1A	SOD-123	ZOWIE	WSGC10MH
19	2	D5,D7	1N4148WS	Diode;75V;0.15A;	SOD-323	Diodes	1N4148WS-7-F
20	1	D6	MBRS320T3G	Diode;200V;3A	SMB	Qianlongxin	MBRS320T3G
21	1	F1	250V/1A	Fuse	DIP	any	
22	2	L1,L2	Inductor,1mH	Inductor,1mH/0.1A	DIP	Bangdayuan	CKL0410-102
23	1	L3	Inductor,2.2mH	Inductor,2.2mH/0.21A	DIP	Wurth	744741222
24	1	L4	BEAD	Magnetic Bead 1.5k/1A	0805	Wurth	742792097
25	1	NTC	220kΩ	Thermistor	0603	muRata	MCP13WM224E03R8
26	1	Q1	SSN1N45BTA	N-Channel Mosfet450V;4250/10V;8.5	TO-92	Fairchild	SSN1N45BTA
27	1	Q2	ISU04N65A	N-Channel MOSFET, 650V, 4A	TO-251	IPS	ISU04N65A
28	3	R1,R2,R5	5.1kΩ	Film Resistor;1%;1/4W	1206	Yageo	RC1206FR-075K1L
29	2	R3,R4	510Ω	DIP,2W RESISTOR	DIP	any	510Ω/2W
30	1	R6	470Ω	DIP,1W RESISTOR	DIP	any	470Ω/1W
31	1	R7	3.9kΩ	Film RES, 1%	0603	Yageo	RC0603FR-073K9L
32	1	R8	1MΩ	DIP,0.25W RESISTOR	DIP	any	1MΩ/0.25W
33	1	R9	20Ω	Film RES;1%	1206	Yageo	RC1206FR-0720RL
34	1	R10	470kΩ/0.5W	Resistor;5%;0.5W	DIP	any	470kΩ/0.5W
35	1	R11	499kΩ	Film RES, 1%	1206	Yageo	RC1206FR-07499KL
36	1	R12	200mΩ	Film RES, 1%	1206	Yageo	RC1206FR-070R2L
37	1	R13	2.2Ω	Film RES, 1%	1206	Royalohm	1206TF2R20
38	1	R14	9.53kΩ	Film RES, 1%	0603	Yageo	RC0603FR-079K53L
39	1	R15	47kΩ	Film RES, 1%	0603	Yageo	RC0603FR-0747kL
40	1	R19	51Ω	Film RES, 1%	0603	Yageo	RC0603FR-0751RL
41	1	R22	30kΩ	Resistor;1%	1206	Yageo	RC1206FR-0730kL
42	1	RV1	TVR10431KSY	430V/2500A	DIP	TKS	TVR10431KSY
43	1	T1	RM6	RM6, Np:Ns:Naux=132:24:25, Lp=3.4mH	RM6	any	
44	1	U1	MP4033GK	MP4033GK	MSOP10	MPS	MP4033GK R2

Optional

Item	Qty	RefDes	Value	Description	Package	Manufacturer	Manufactuer_P/N
1	1	C12	10nF/250V	Ceramic Cap,X7R,250V	0805	TDK	C2012X7R2E103K
2	1	C13	22uF/50V	Electrolytic Capacitor;50V;Electrolytic	DIP	Jianghai	CD281L-50V22
3	2	D10,D12	BAV21W	Diode;200V;0.2A;	SOD-123	Diodes	BAV21W-7-F
4	1	D11	BZT52C4V7	Zener Diode, 4.7V, 5mA	SOD-123	Diodes	BZT52C4V7
5	1	D9	BZT52C2V4	Zener Diode, 2.4V, 5mA	SOD-123	Diodes	BZT52C2V4
6	1	D8	1N4148WS	Diode;75V;0.15A;	SOD-323	Diodes	1N4148WS-7-F
7	1	Q3	AM2340NE	N-channel MOSFET, 40V,5.2A	SOT23	Analog Power	AM2340NE
8	1	R16	2kΩ	Film RES;1%	1206	Yageo	RC1206FR-072KL
9	1	R17	10kΩ	Film RES;1%	0603	Yageo	RC0603FR-0710KL
10	2	R18,R21	20kΩ	Film RES;1%	0603	Yageo	RC0603FR-0720KL
11	1	R20	51kΩ	Film RES;1%	0603	Yageo	RC0603FR-0751KL

5. EXPERIMENTAL RESULT

All measurements performed at room temperature

5.1 PERFORMANCE DATA

VIN(VAC)	Io(A)	Vo(V)	Pin(W)	PF	THD	Efficiency
198	0.421	24.03	12.02	0.945	16.5%	84.16%
230	0.423	24.05	12.15	0.913	19.5%	83.73%
265	0.425	24.01	12.28	0.87	23.8%	83.10%

5.2 STEADY STATE

I_O, 200mA/div

V_{CC}, 10V/div

V_{COMP}, 1V/div

V_D, 10V/div
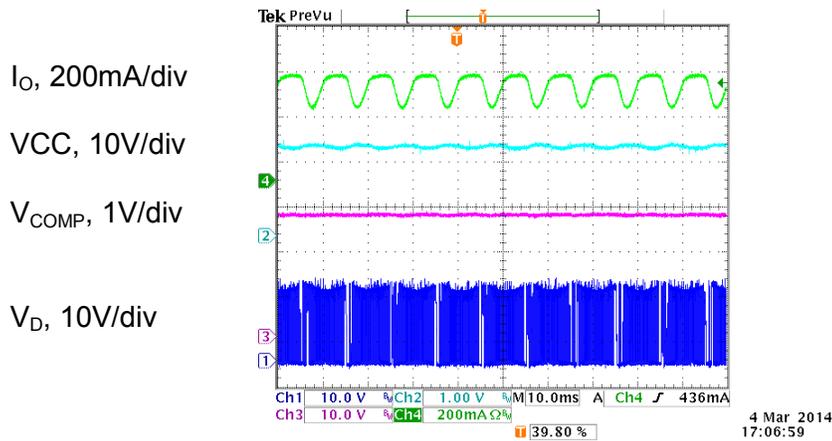
Figure 28: 230VAC, Full Load, 10ms/div

5.3 INPUT VOLTAGE AND CURRENT

I_{IN}, 50mA/div

V_{MULT}, 500mV/div
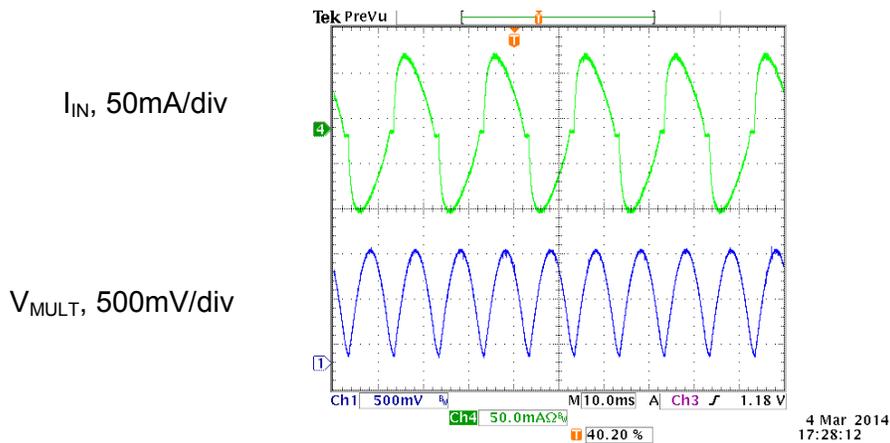
Figure 29: 230VAC, Full Load, 10ms/div

5.4 BOUNDARY CONDUCTION OPERATION

V_S, 1V/div

V_{ZCD}, 2V/div

V_D, 10V/div
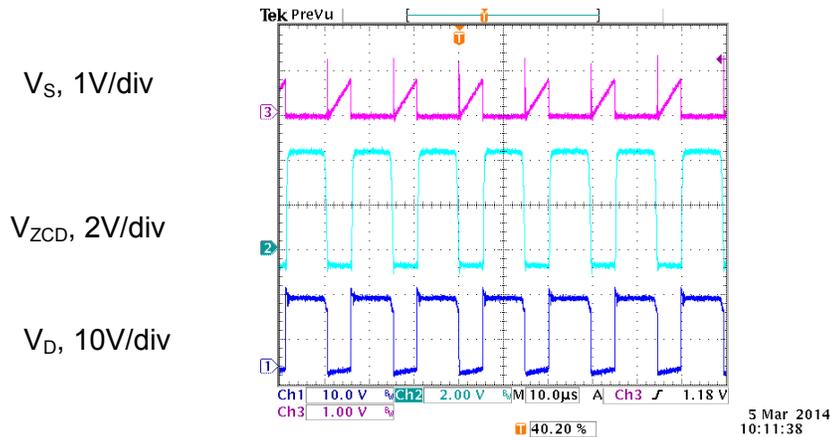
Figure 30: 230VAC, Full Load, 10μs/div

5.5 START UP AT NO DIMMING CONDITION

I_O, 200mA/div

VCC, 10V/div

V_{COMP}, 1V /div

V_D, 10V/div
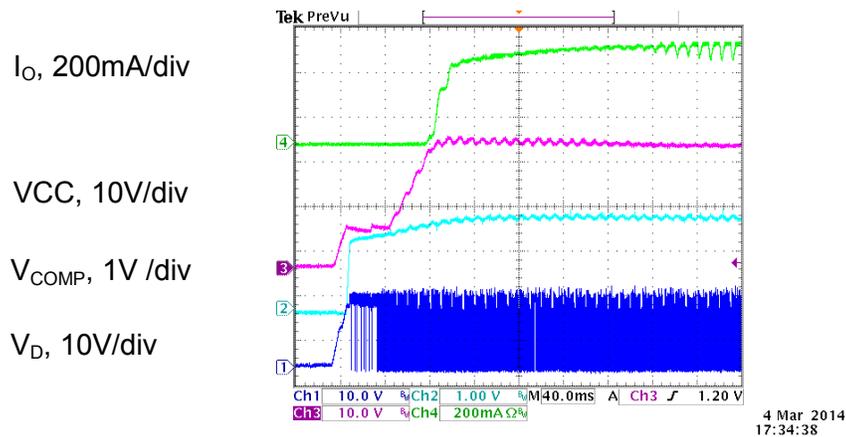
Figure 31: 230VAC, Full Load, 40ms/div

5.6 OVP (OPEN LOAD AT NORMAL OPERATION)

VCC, 20V/div

V_{COMP}, 2V /div

V_{ZCD}, 2V/div

I_O, 500mA/div
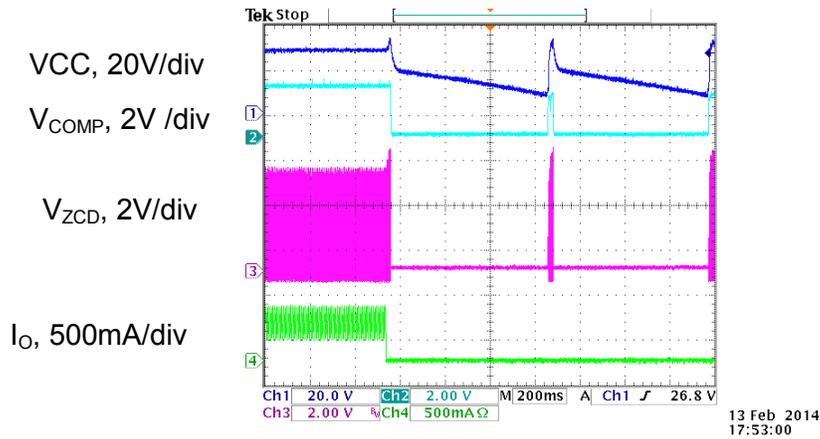
Figure 32: 230VAC, 200ms/div

V_O, 10V/div

I_O, 500mA/div
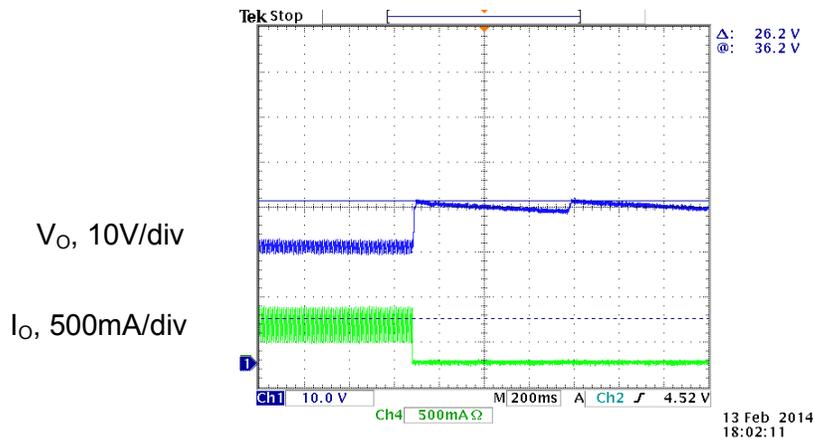
Figure 33: 230VAC, 200ms/div

5.7 SCP (SHORT LED+ TO LED– AT START UP)

VCC, 5V/div

V_{COMP}, 1V /div

I_{SHORT}, 500mA/div
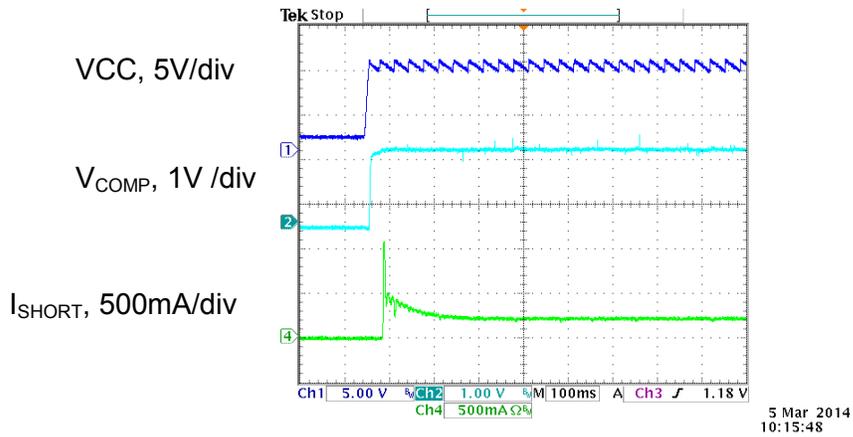
Figure 34: 230V, 100ms/div

5.8 PRIMARY WINDING SHORT AT START UP

V_{COMP}, 1V /div

V_{CC}, 5V /div
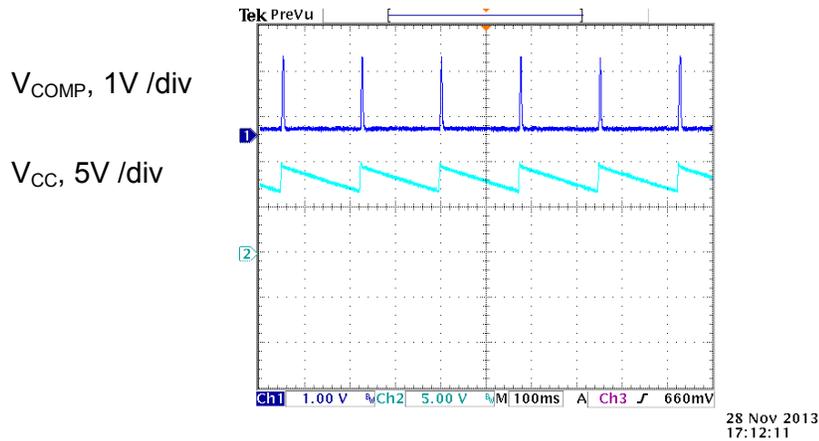
Figure 35: 230VAC, 100ms/div

5.9 LEADING EDGE DIMMING

I_O, 200mA/div

V_{COMP}, 1V /div

I_{IN}, 500mA/div

V_{MULT}, 1V/div
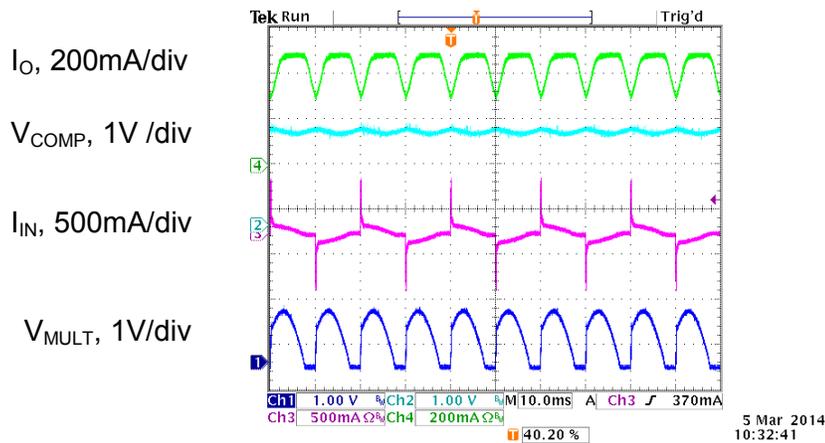
Figure 36: 230VAC, D=70%, 10ms/div

I_O, 200mA/div

V_{COMP}, 1V /div

I_{IN}, 500mA/div

V_{MULT}, 1V/div
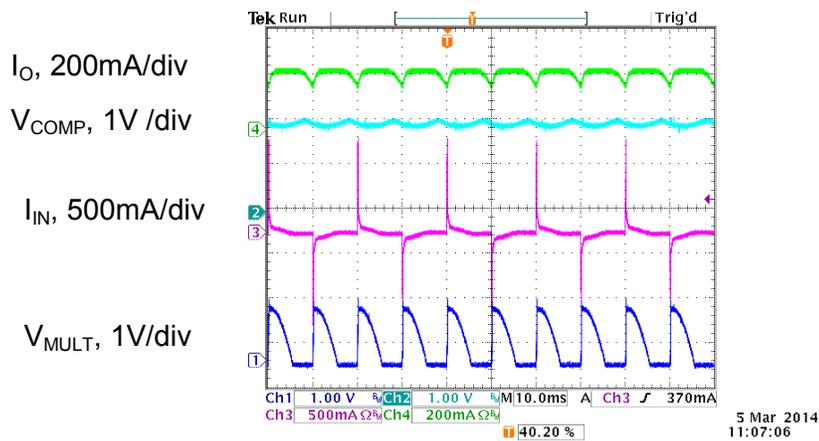
Figure 37: 230VAC, D=50%, 10ms/div

I_O, 50mA/div

V_{COMP}, 1V /div

I_{IN}, 500mA/div

V_{MULT}, 1V/div
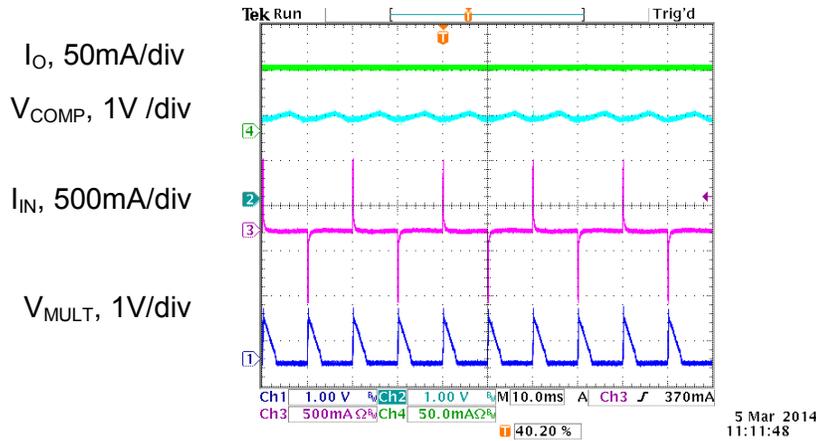
Figure 38: 230VAC, D=30%, 10ms/div

5.10 TRAILING EDGE DIMMING

I_O, 200mA/div

V_{COMP}, 1V /div

I_{IN}, 100mA/div

V_{MULT}, 1V/div
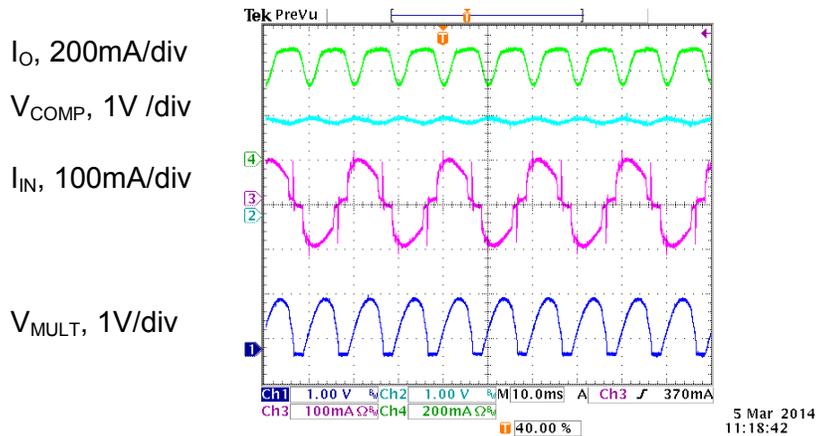
Figure 39: 230VAC, D=70%, 10ms/div

I_O, 50mA/div

V_{COMP}, 1V /div

I_{IN}, 100mA/div

V_{MULT}, 1V/div
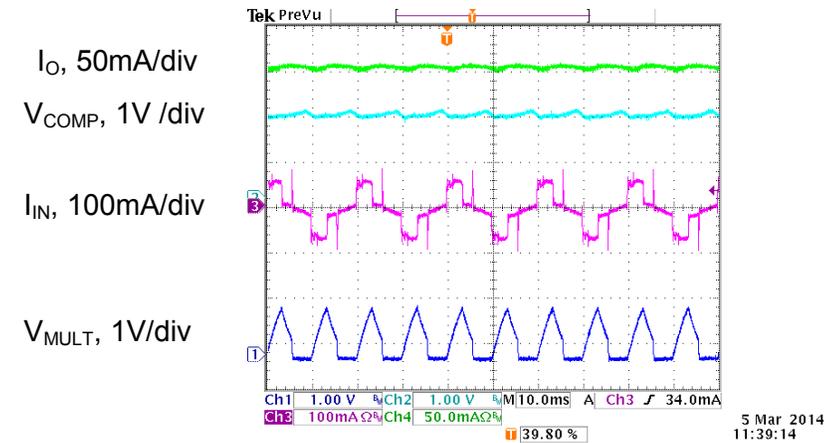
Figure 40: 230VAC, D=50%, 10ms/div

I_O, 20mA/div
V_{COMP}, 1V /div

I_{IN}, 100mA/div

V_{MULT}, 1V/div
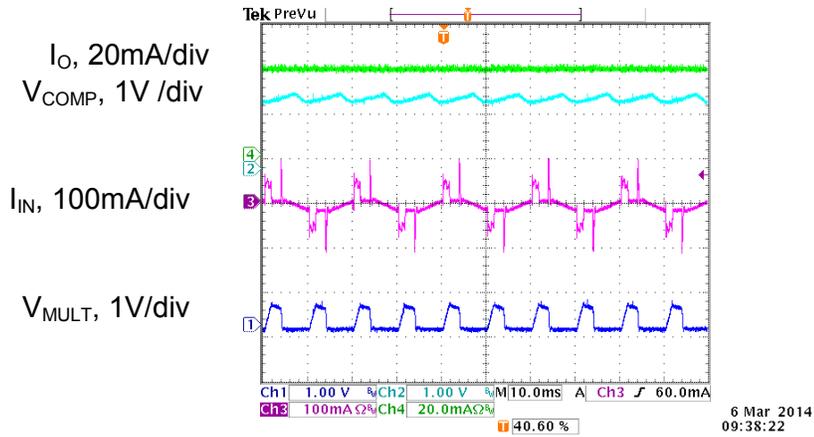
Figure 41: 230VAC, D=30%, 10ms/div

5.11 DIMMING CURVE
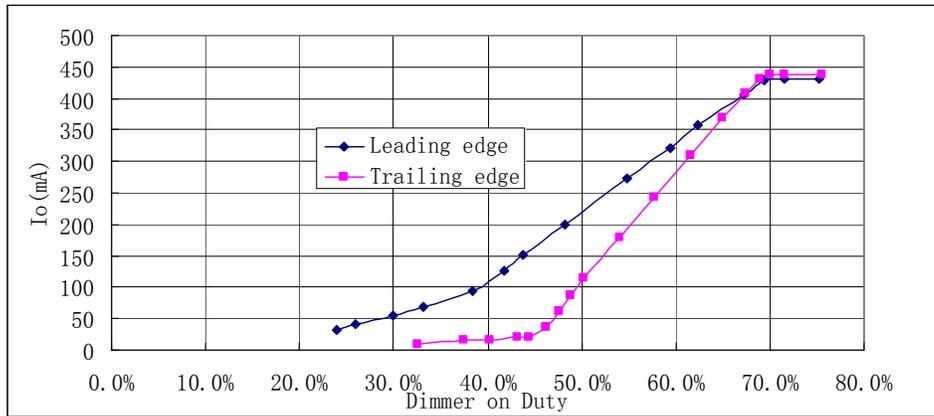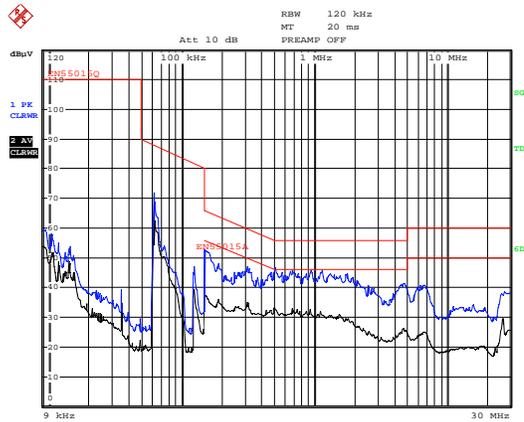

Figure 42: 230VAC, Dimming Curve

5.12 CONDUCTION EMI

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Figure 43: Conduction EMI