

MP6902
Synchronous Rectification Controller
Application Note

Prepared by Lei Miao

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AN077

MP6902

Synchronous Rectification Controller

ABSTRACT

This document will explain the operation principle and present the design procedure of MP6902 in detail.

INDEX

MP6902 Introduction.....	4
Driving Method and Operation Logic.....	4
Turn On Phase (t_1).....	4
Conduction Phase ($t_1 - t_4$)	4
Turn Off Phase ($t_4 - t_5$)	4
Power Saving Mode at Light Load	5
COMPONENTS SELECTION AND DESIGN GUIDE	6
Components Design Procedure	6
SR Driver Design Guide during System Transient	7
RC Snubber Design Guide	9
a. Choose proper C_S	9
b. Choose proper R_S	11
c. How to determine C_P and L_S	12
d. Design Example for an optimized RC snubber network	13
SR Design Guide in CCM Flyback Application.....	15
CCM Flyback SR Design Example with MP6902	20
LAYOUT CONSIDERATIONS	23
Sensing for V_D/V_{SS}	23
V_{DD} Decoupling Capacitor	24
Gate Driver Loop	24
Layout Example.....	24

MP6902 INTRODUCTION

MP6902 is a synchronous rectification controller designed for Flyback converters. By driving N-Channel MOSFET on the secondary side of an isolate/non-isolate Flyback converter, higher efficiency is achieved compared with traditional schottky diode rectification. This IC regulates the forward voltage drop of the MOSFET at $\sim 70\text{mV}$ and switches it off as soon as the drain-source voltage of the rectifier becomes negative. At no/light load condition, the IC turns off the driver signal to save the driving loss.

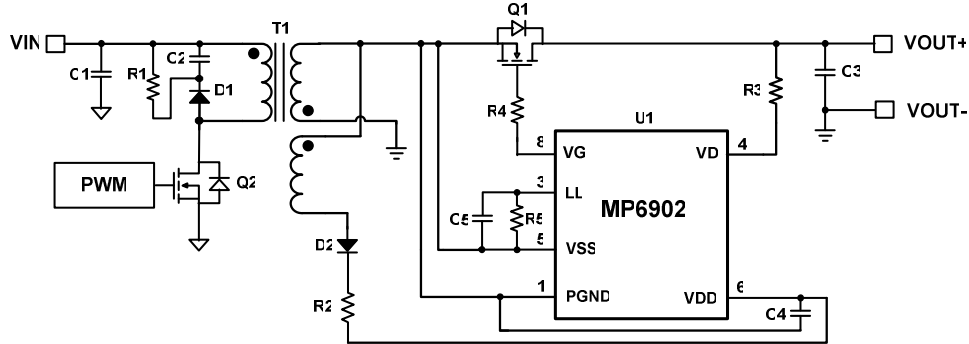


Figure 1 – Typical Application for MP6902 in Flyback Converter

DRIVING METHOD AND OPERATION LOGIC

Figure 1 shows the typical application circuit of a Flyback converter with MP6902. The IC senses the drain-source voltage of the rectifier and compares it with internal turn-on threshold (-70mV) and turn-off threshold (-30mV) to determine the on/off timing for the SR (Synchronous Rectification) FET, see figure 2:

Turn On Phase (t_1)

When the switching current initiates in the SR FET, body-diode conducts which generates a voltage drop much higher than the turn-on threshold (-70mV) of the IC, this will trigger the driver turns on the MOSFET.

At the beginning of SR FET's turn-on, switching current will transfer through the $R_{ds(ON)}$ and lead to the drain-source voltage drop rises, during which some oscillation will occur on V_{DS} lead by the parasitic parameters (after t_1), in order to prevent the V_{DS} ringing from triggering the driver turns off the SR FET, a turn on blanking time ($\sim 1.6\mu\text{s}$) is applied in MP6902, during which the turn-off threshold of the driver will be increased to a fairly high level so that the voltage ringing on V_{DS} won't trigger it

Conduction Phase ($t_1 - t_4$)

As the drain-source voltage V_{DS} ($I_{DS} \times R_{ds(ON)}$) change with the switching current, when the switching current drops to the level which makes V_{DS} above -70mV (turn-on threshold) at t_3 , the IC stops pulling up the gate driver which makes the driver voltage V_{GS} of the SR FET drops, hence the $R_{ds(ON)}$ of SR FET increases and the voltage drop V_{DS} is adjusted at $\sim -70\text{mV}$.

Turn Off Phase ($t_4 - t_5$)

When switching current keeps dropping to the level which make V_{DS} trigger the turn-off threshold (-30mV), gate driver is turned off by the internal fast turn-off comparator. Once the SR FET is turned off, the switching current will flow through the body diode and lead to V_{DS} trigger the turn-on threshold (-70mV) again, in order to avoid the gate driver re-turn on, a turn off blanking time is applied and force the gate driver's off state lasts for at least $\sim 200\text{ns}$.

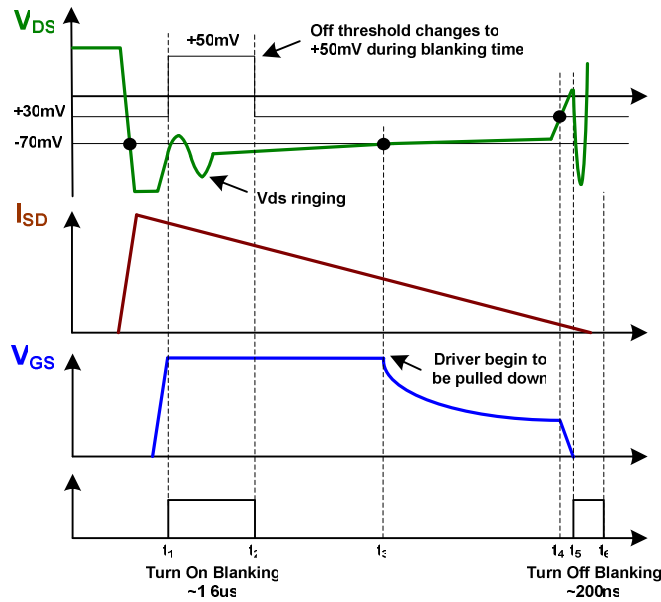


Figure 2 — Operation for MP6902 in Flyback Converter

In figure 2, from t_1 to t_2 is the turn on blanking time which to prevent the V_{DS} ringing affect; from t_3 to t_4 , gate voltage stops be pulled up by the driver, which begins to drop when V_{DS} rises higher than $-70mV$; at t_4 V_{DS} triggers $-30mV$ turn off threshold, gate driver is fast pulled down; from t_5 to t_6 , turn off blanking time forces gate driver remains turn off.

Power Saving Mode at Light Load

When the system is running with light load, rectifier conduction loss no longer dominates the secondary-side power loss, in which condition it is preferred the SR FET keeps off to save the driver loss.

MP6902 senses the secondary rectifier conduction duration t_{ON} each cycle, when t_{ON} keeps smaller than the internal light load timing t_{LL} (typical $2.2\mu s$, programmable on LL pin) for more than $\sim 100\mu s$, the IC will shutdown the gate driver and keeps it off until t_{ON} has increased to $t_{LL} + t_{LL,H}$ ($t_{LL,H}$ is the light load timing hysteresis, typical $0.2\mu s$). Figure 3 and figure 4 show the procedure of MP6902 enter/exit light load mode.

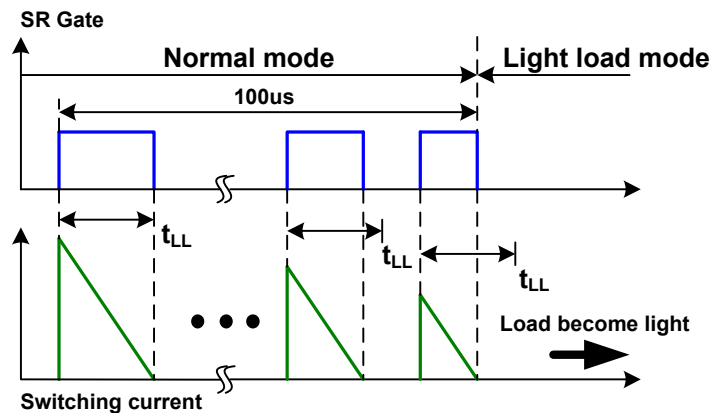
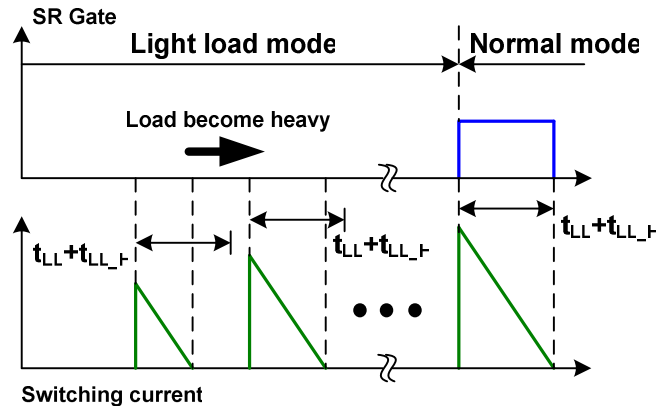


Figure 3 — MP6902 Enters Light Load Mode


Figure 4 — MP6902 Exits Light Load Mode

COMPONENTS SELECTION AND DESIGN GUIDE

Components Design Procedure

From figure 1, the external components recommended for MP6902 in Flyback converter are:

- R3, series resistor in VD sensing line, typical 1kΩ to protect VD pin from excessive current flows into it when pin voltage goes below -0.7V (SR FET's body diode conduction). Too large value of this resistor may delay the turn-on/off timing of the driver due to the parasitic capacitance on VD pin.
- R4, gate driver resistor for SR FET. An anti-parallel diode may be required when fast turn off speed of the gate is preferred.
- R5 and C5, LL pin resistor and capacitor used to program the light load timing t_{LL} , C5 is typically 1nF used to decouple the noise, R5 is selected from 30kΩ to 300kΩ to set the light load timing t_{LL} as following:

$$t_{LL} = \frac{R5(k\Omega)}{100k\Omega} \cdot 2.2\mu s \quad (1)$$

- C4, decouple capacitor for IC's power supply, typical no smaller than 1μF
- EN pin of the IC is internal pulled up by the regulator from V_{DD} with a ~15μA current source. Leave this pin open if unused. When use external signal to control EN, it is highly recommended the pull down current be larger than 15uA to make sure the EN pin can be pulled to low.
- R2 and D2, series resistor and diode from auxiliary winding which used as the power supply of IC. The VDD power voltage can be derived from:

$$V_{DD} = \frac{N_{au}}{N_s} \cdot V_{OUT} \quad (2)$$

Where N_s and N_{au} are the turn counts for secondary and auxiliary winding, V_{OUT} is the system output voltage.

When secondary rectifier is put on low-side, the power supply of MP6902 can be derived directly from output voltage.

Figure 5 shows another non-auxiliary winding power solution for MP6902, R2, R6, D3, Q3 forms an external LDO circuit, in which D3 provides the output clamp of the LDO, R6 (typical <1kΩ) limits the LDO current, while R2 provides the turn on signal for Q3, which can be selected as several tens kΩ. The D2 can also be connect to system output voltage (VOUT+) instead of transformer winding, when the LDO output is not high enough to power the VDD.

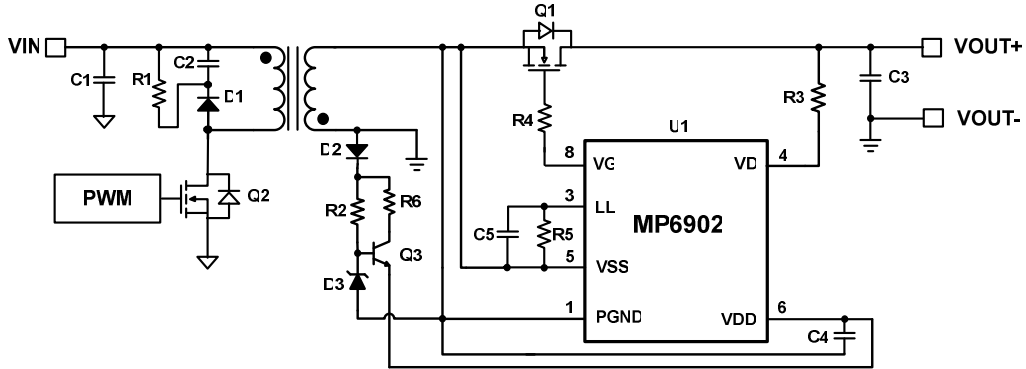


Figure 5 — Non-auxiliary Winding Power Solution for MP6902

SR Driver Design Guide during System Transient

When the Flyback system is working during start-up, shutdown and OCP/Short, the SR driver IC may be turned off due to insufficient power supply lead by the system output drop out. In this case, the switching current will flow through the body diode of the SR FET, if the reverse recovery time of the body-diode is not as short as a Schottky, fairly large reverse current and voltage spike may be observed on the SR FET, especially in CCM condition.

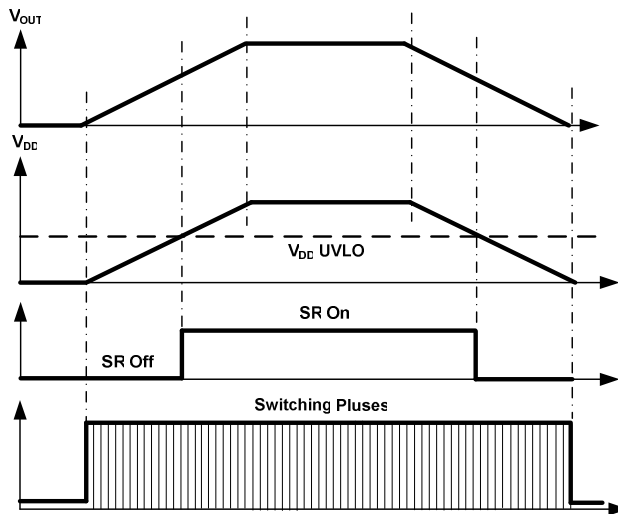


Figure 6 — SR Driver V_{DD} Power Supply During System Transient

Figure 6 shows an example of SR driver power supply during system transient, although the system is switching as soon as the output voltage (V_{OUT}) is set up, the SR driver won't start to work until the power supply (V_{DD}) has crossed above the V_{DD} UVLO, before which the switching current will flow through the SR FET's body diode.

In order to avoid reverse current and voltage spike lead by the output voltage drop out, we can:

- Parallel a small schottky diode on the SR FET. When the SR driver is turned off due to the system output drop out, the switching current will flow through the external schottky diode which has lower forward voltage drop and reverse recovery time compared with SR FET's body diode.
- Make the V_{DD} UVLO of the driver IC be crossed when system output is still fairly low. For example, design the V_{DD} of the SR driver IC be ~20V at steady state, so that the driver won't be shut down until the output voltage had dropped to ~30% according to (2) (the V_{DD} UVLO of the SR driver is ~6V). This could help to extend the SR driver's active state during system start-up or shutdown.

See figure 7 which SR driver startup earlier than in figure 6.

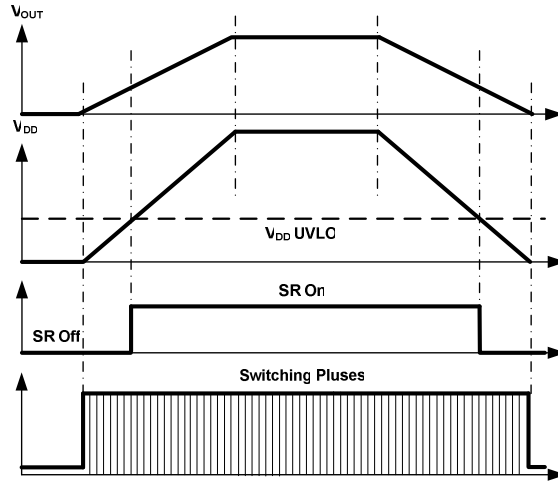


Figure 7 — Extend the SR Driver’s Active Duration

- Design the V_{DD} power supply derived from secondary transformer winding as figure 5 shows. This will make the V_{DD} power supply capacitor charged as soon as the system is switching, which means the V_{DD} power supply voltage level rises much faster.

Figure 8 shows the simulation of the SR driver’s V_{DD} power supply charge speed during system startup. In which V_{DD1} is the SR driver’s power supply derived from transformer winding; V_{DD2} is the power supply derived from auxiliary winding. From the comparison results, V_{DD1} is charged as soon as the Flyback converter is switching (V_D is the secondary side winding voltage), while V_{DD2} follows the output voltage (V_{OUT}) charge speed, which is much slower.

Figure 9 is the experimental results of the SR driver start when system is during start-up or SCP, from which the simulation results in figure 8 is verified.

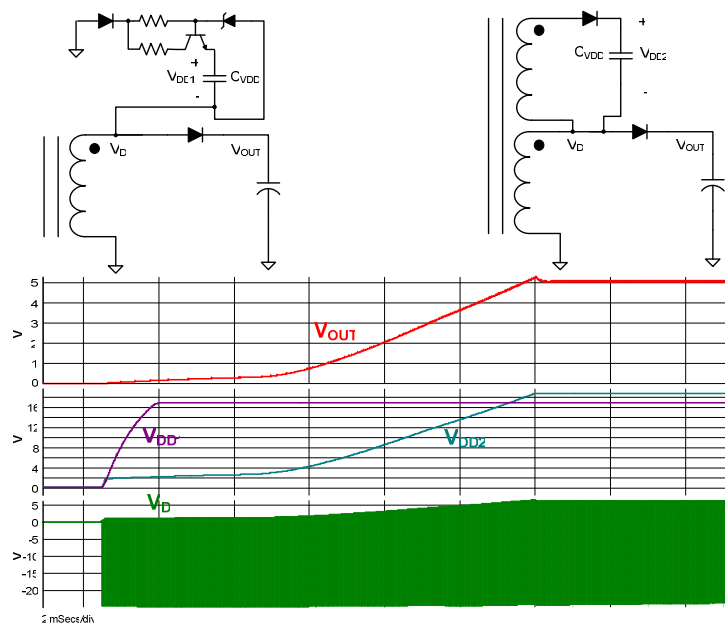


Figure 8 — SR Driver Power Supply Charge Speed Comparison at Startup

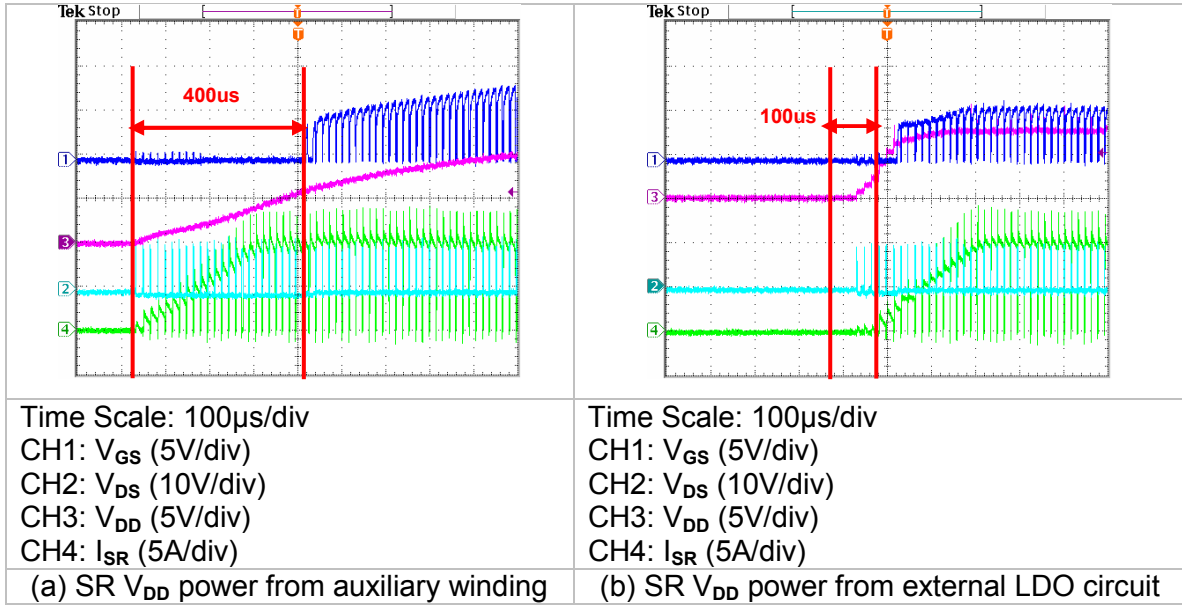


Figure 9 —SR Driver Power Charge during System Start-up & SCP Recovery

RC Snubber Design Guide

Generally, we need a simple RC snubber network putting in parallel to the drain-source of the SR FET, which is responsible for damping the voltage overshoot lead by reverse current through the SR FET, see figure 10.

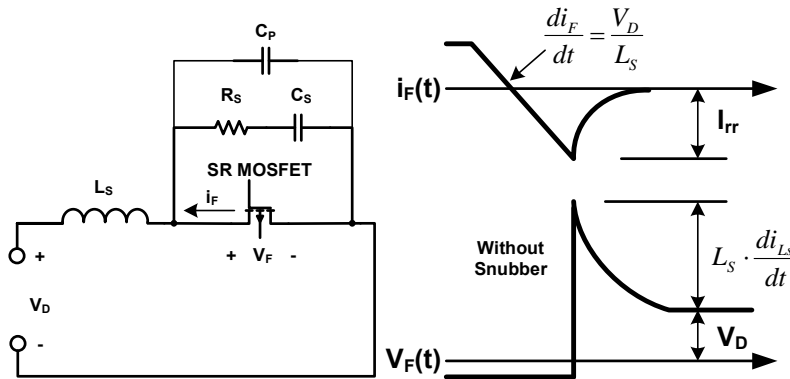


Figure 10 — RC Snubber on SR MOSFET of Flyback Secondary Side

Figure 10 shows the equivalent model of the Flyback secondary side circuit with an RC snubber on SR FET, where V_D implies the secondary side voltage derived in equation (3), V_F is the drain-source voltage on SR FET, R_S and C_S forms the RC snubber network while L_S is the leakage inductance of the transformer secondary winding, C_P implies the stray capacitance of the secondary side circuit.

$$V_D = V_{OUT} + V_{IN_DC} / n \tag{3}$$

Where V_{OUT} is the output voltage; V_{IN_DC} is the input DC voltage and n is the Flyback transformer turn-ratio.

a. Choose proper C_S

In order to simplify the analysis model of C_S impact on $V_F(t)$, consider R_S as a constant 0, we can get figure 11 and equation (4) as following, where C_K implies “ C_S+C_P ” in figure 10.

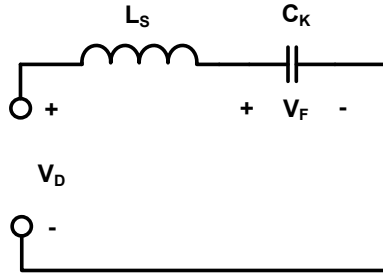


Figure 11 — Simplified Equivalent Circuit for RC Snubber Network ($R_S=0$)

$$\frac{d^2V_F(t)}{dt^2} + \frac{V_F(t)}{L_S \cdot C_K} = \frac{V_D}{L_S \cdot C_K} \tag{4-a}$$

$$V_F(0^+) = 0; \frac{dV_F(0^+)}{dt} = i_f(0^+) = I_{rr} \tag{4-b}$$

Where I_{rr} is the peak reverse current through the SR MOSFET, which can be also find in figure 10. From (4), the drain-source voltage through the SR MOSFET V_F is as follows:

$$V_F(t) = V_D - V_D \cdot \cos(\omega_0 \cdot t) + V_D \cdot \sqrt{\frac{C_B}{C_K}} \cdot \sin(\omega_0 \cdot t) \tag{5-a}$$

$$\omega_0 = \frac{1}{\sqrt{L_S \cdot C_K}}; C_B = L_S \left(\frac{I_{rr}}{V_D}\right)^2 \tag{5-b}$$

When $\cos(\omega_0 t)$ equals to 0, the $V_F(t)$ gets to its maximum which implies the peak voltage spike on SR FET:

$$V_{F_MAX} = V_D \cdot \left(1 + \sqrt{\frac{C_B}{C_K}}\right) \tag{6}$$

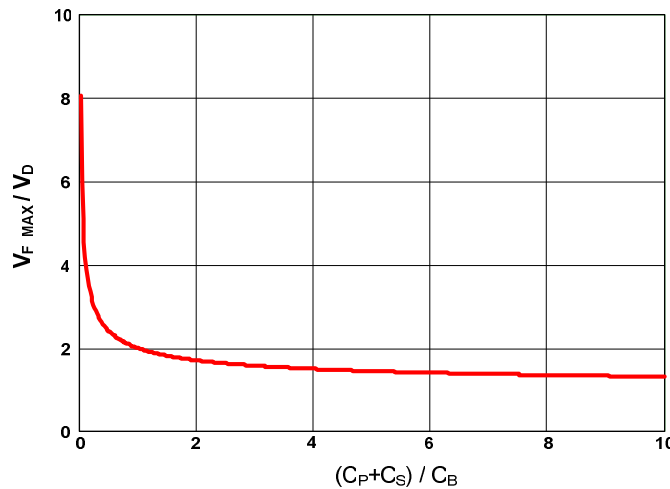


Figure 12 — C_S Value Effect on the SR FET Voltage Spike

From (6) and figure 12, we can know by designing C_S larger, the damping effect on SR FET voltage spike will be better. But in real application, considering the power loss on RC snubber in (7), C_S is not recommended to be set too large. Generally we choose C_S as 2~3 times of C_P for a fairly well damping effect.

$$P_{Snubber} = \frac{1}{2} \cdot V_D^2 \cdot C_S \cdot f_s \tag{7}$$

b. Choose proper R_S

The analysis model of R_S impact on $V_F(t)$ is much more complicated than C_S , due to the C_S value is always selected much larger than C_P , figure 13 and (8) shows an simplified model for R_S which neglects the C_P impact.

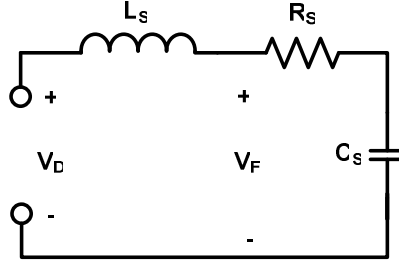


Figure 13 — Simplified Equivalent Circuit for RC Snubber Network ($C_P=0$)

$$L_S \cdot C_S \frac{d^2V_F(t)}{dt^2} + R_S \cdot C_S \cdot \frac{dV_F(t)}{dt} + V_F(t) = V_D \tag{8-a}$$

$$V_F(0^+) = I_{rr} \cdot R_S; \frac{dV_F(0^+)}{dt} = \frac{I_{rr}}{C_S} + \frac{R_S \cdot V_D}{L_S} - \frac{I_{rr} \cdot R_S^2}{L_S} \tag{8-b}$$

From (8), the drain-source voltage through the SR MOSFET V_F is derived as follows:

$$V_F(t) = V_D - (V_D - R_S \cdot I_{rr}) \cdot \left[\cos(\omega \cdot t) - \frac{\alpha}{\omega} \sin(\omega \cdot t) \right] \cdot e^{-\alpha t} + \frac{I_{rr}}{C_S \cdot \omega} \cdot \sin(\omega \cdot t) \cdot e^{-\alpha t} \tag{9-a}$$

$$\omega = \sqrt{\omega_0^2 - \alpha^2}; \omega_0 = \frac{1}{\sqrt{L_S \cdot C_S}}; \alpha = \frac{R_S}{2 \cdot L_S} \tag{9-b}$$

According to (9), by setting $dV_F(t)/dt=0$, the drain-source voltage spike across the SR FET will reach to its maximum when:

$$t = t_M = \frac{1}{\omega} \cdot \tan^{-1} \left[\frac{(V_D - R_S \cdot I_{rr}) \cdot 2\alpha + \frac{I_{rr}}{C_S}}{(V_D - R_S \cdot I_{rr}) \frac{\omega^2 - \alpha^2}{\omega} - \frac{I_{rr} \cdot \alpha}{C_S \cdot \omega}} \right] \tag{10}$$

Put (10) into (9), we can get the peak voltage spike on the SR FET with RC snubber is:

$$V_{F_MAX} = V_D + e^{-\alpha \cdot t_M} \cdot \sqrt{(V_D - R_S \cdot I_{rr})^2 + \frac{2\alpha \cdot (V_D - I_{rr} \cdot R_S)}{\omega_0^2} \cdot \frac{I_{rr}}{C_S} \cdot \frac{I_{rr}^2}{\omega_0^2 \cdot C_S^2}} \tag{11}$$

But V_{F_MAX} in (11) is so complicated which can't tell how R_S affect this value, so we need further simplify (11) as follows:

$$V_{F_MAX} = V_D + V_D \cdot e^{\left\{ \frac{-x}{\sqrt{1-x^2}} \tan^{-1}[f(x,y)] \right\}} \cdot \sqrt{1-2xy+y^2} \tag{12-a}$$

$$f(x,y) = -\frac{(2x - 4x^2y + y) \cdot \sqrt{1-x^2}}{1-3xy-2x^2+4x^3y} \tag{12-b}$$

$$x = \frac{R_S}{2\sqrt{L_S/C_S}}; y = \frac{I_{rr}}{V_D} \cdot \sqrt{\frac{L_S}{C_S}} \tag{12-c}$$

Once C_S is selected, y in (12) becomes a constant which makes V_{F_MAX} a function of x . Figure 14 shows the drain-source peak voltage spike as function of x and y , from which we can see with different y value, x that implies R_S selection always has an optimized value which makes the drain-source peak voltage

spike (V_{F_MAX}) minimum. With smaller y , the optimized x value will be closer to 1; while with y value becomes larger, x needs to be selected smaller, which means smaller R_S value needed.

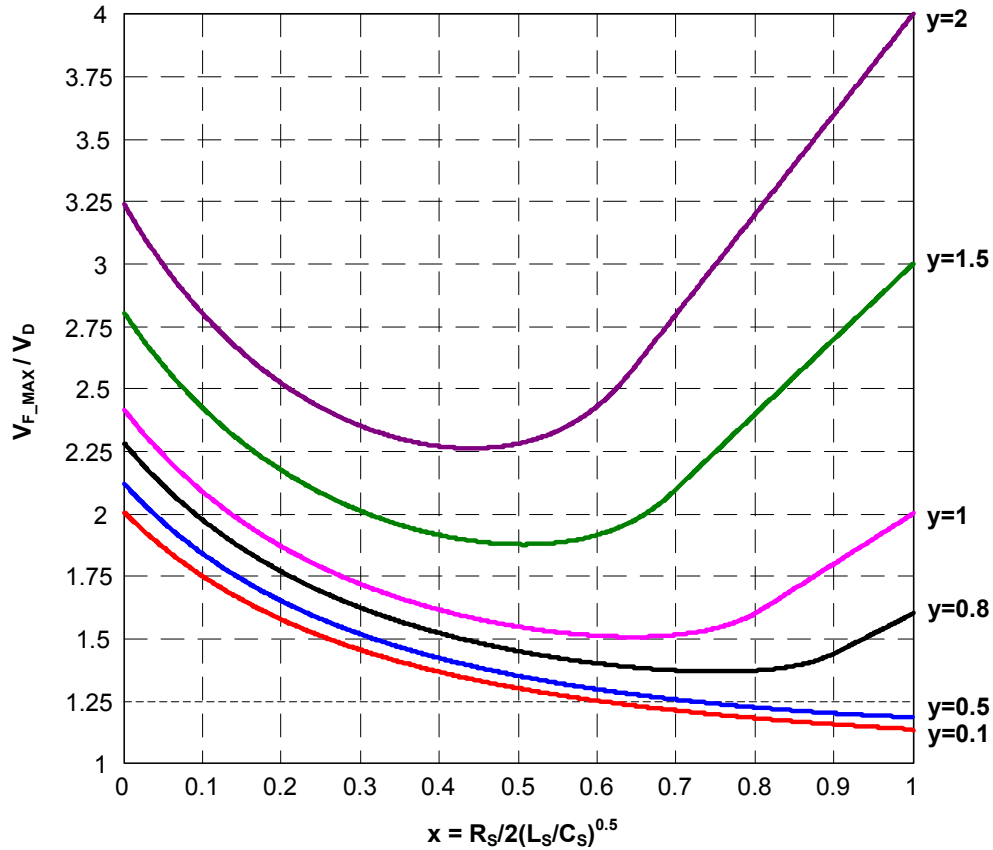


Figure 14 — R_S Value Effect on the SR FET Voltage Spike

c. How to determine C_P and L_S

The analysis above implies how to select R_S and C_S to make the RC snubber network best fit the system according to different stray capacitance (C_P) and inductance (L_S). So before the RC snubber design started, we need to determine the C_P and L_S of the system which may be derived by the following simple method:

- i. Keep RC snubber unconnected, parallel a capacitor C_1 on SR MOSFET and capture the drain-source voltage V_{DS} oscillation frequency f_{sw1} by oscillograph.
- ii. Keep RC snubber unconnected, parallel a capacitor C_2 on SR MOSFET and capture the drain-source voltage V_{DS} oscillation frequency f_{sw2} by oscillograph.
- iii. Calculate the C_P and L_S by the following equation:

$$f_{sw1} = \frac{1}{2\pi \cdot \sqrt{L_S \cdot (C_P + C_1)}} \tag{13-a}$$

$$f_{sw2} = \frac{1}{2\pi \cdot \sqrt{L_S \cdot (C_P + C_2)}} \tag{13-b}$$

Following is an example to determine C_P and L_S for a 20W universal input adapter application with CCM Flyback:

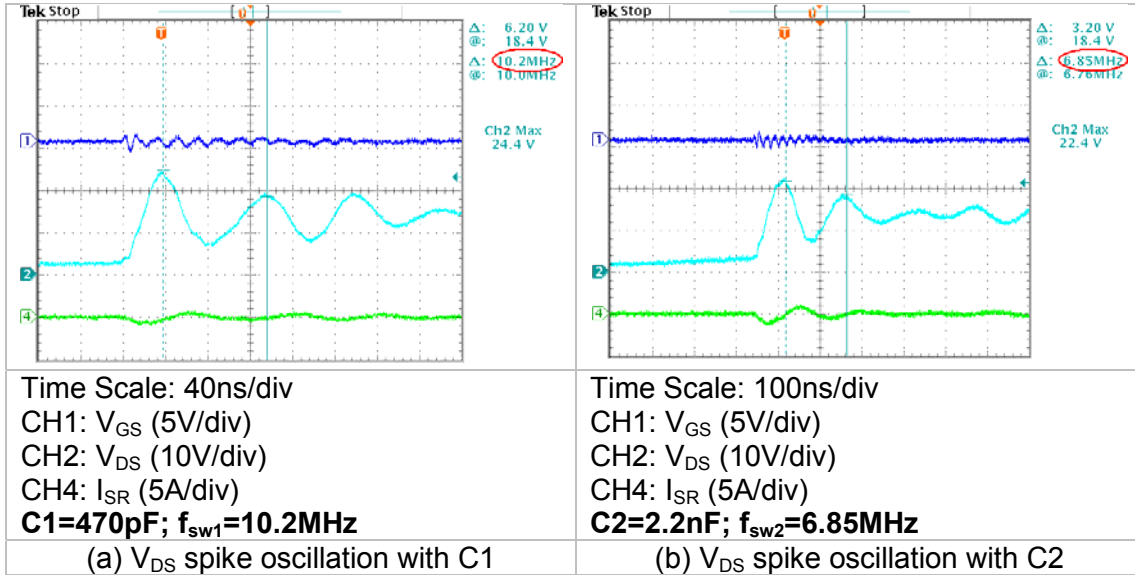


Figure 15 — Drain-Source Voltage Spike Oscillation

According to (13) and bench test results in figure 15, C_P and L_S can be calculated as $\sim 940\text{pF}$ and $\sim 0.2\mu\text{H}$.

d. Design Example for an optimized RC snubber network

A design example of RC snubber network for a 20W universal input adapter with CCM Flyback is as follows:

- Input AC voltage: $90V_{ac} \sim 265V_{ac}$ (V_{IN_DC} : $120V \sim 380V$)
- Output DC voltage V_{OUT} : 5V
- Transformer turn ratio n: 15 (From primary to secondary)
- Secondary stray capacitance and inductance: $C_P=940\text{pF}$, $L_S=0.2\mu\text{H}$, which is already got from (13) and figure 15.

The RC snubber network needs to be optimized based on the condition when drain-source voltage spike has its maximum value. For a universal input Flyback converter, the drain-source voltage spike will reach its maximum during system start-up with high line input, in which condition both CCM switching current and V_D level is the highest.

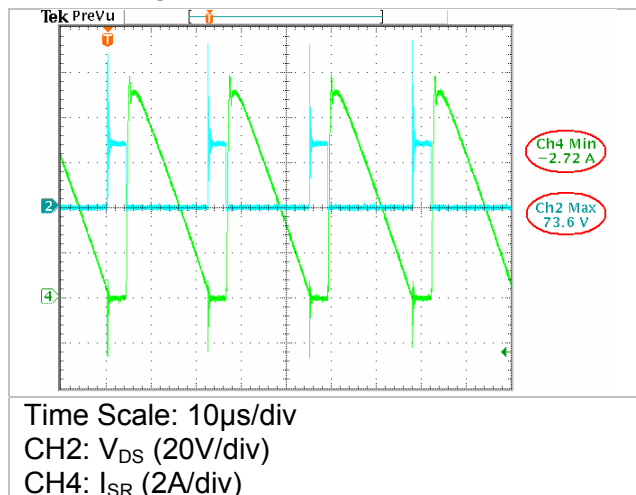


Figure 16 — Maximum Voltage Spike during Start-Up at High Line Input

Figure 16 shows the bench test result of the maximum voltage spike and reverse current (I_{rr}) during system start up at high-line input without RC snubber applied. Also based on the specification of this 20W Flyback converter, we can get:

$$I_{rr} \approx 2.8A$$

$$V_D = V_{OUT} + V_{IN_DC} / n \approx 30V$$

$$C_p \approx 940pF; L_s \approx 0.2\mu H$$

According to the analysis above, we choose C_s as 2~3 times of C_p , in this design example, C_s is selected as 2.2nF:

$$C_s = 2.2nF$$

So, from (12), now y can be derived as:

$$y = \frac{I_{rr}}{V_D} \cdot \sqrt{\frac{L_s}{C_s}} = 0.89$$

With $y \approx 0.9$, we can get the optimized RC snubber design is to make x be ~ 0.7 according to figure 14:

$$x = \frac{R_s}{2 \cdot \sqrt{L_s / C_s}} \approx 0.7 \tag{14}$$

From (14), R_s can be calculated which is $\sim 13.3\Omega$. So connect the RC snubber network as $C_s=2.2nF$ & $R_s=13.3\Omega$, the maximum voltage spike on SR FET during system start-up at high line input is showed in figure 17, we can find over 30V voltage spike is damped by the RC snubber compared with in figure 16.

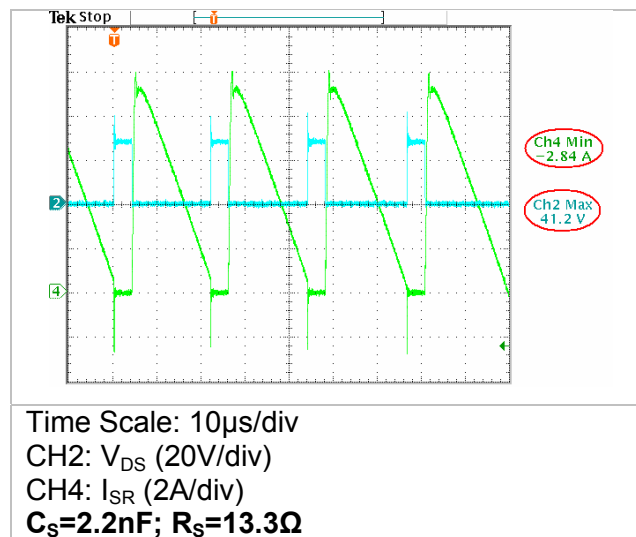


Figure 17 — Maximum Voltage Spike during Start-Up at High Line Input with RC Snubber

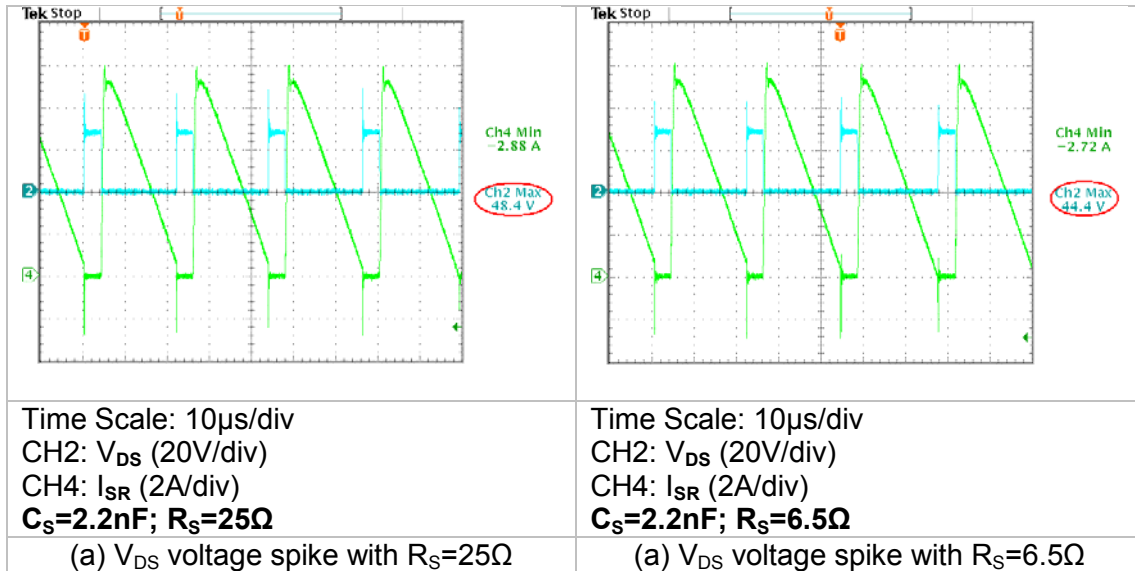


Figure 18 — Maximum Voltage Spike with different R_S Value

Figure 18 shows the maximum voltage spike with the same C_S but different R_S value. We can find by choosing R_S larger or smaller than the optimized value (13.3Ω), the maximum voltage spike will be larger.

SR Design Guide in CCM Flyback Application

It is required to pay more attention on the turn-off timing of the SR driver in CCM Flyback application. Figure 19 shows the operation of MP6902 in CCM Flyback system, when CCM turn-off of switching current I_{SD} occurs at t₁, the sensed drain-source voltage V_{DS} on MP6902 will have a rapid increase which is lead by the voltage drop (V_{LK}) on the parasitic inductance of the SR FET’s package:

$$V_{DS} = -I_{SD} \cdot r_{ds(ON)} + V_{LK} \tag{15}$$

$$V_{LK} = L_S \cdot \frac{dI}{dt} \tag{16}$$

Where the L_S is the parasitic inductance of the SR FET’s package, dI/dt is the switching current slew rate when CCM turn-off occurs. Due to the negative slew rate of dI/dt, V_{LK} is reverse polarity compared with the voltage drop on SR FET’s on resistance (r_{ds(ON)}).

For L_S, figure 20 shows the typical L_S value of a traditional TO220-3 package MOSFET simulated by Ansoft. For some SMD packages, such like SO8 and TO252, the L_S is a bit smaller, which is in figure 21. The trace on the PCB layout will also bring in some leakage inductance, which is ~1nH/mm.

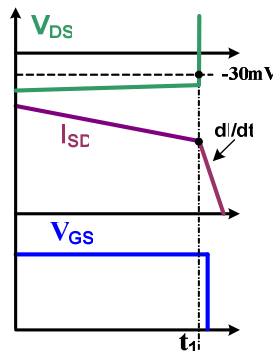


Figure 19 — Operation of MP6902 in CCM Flyback System

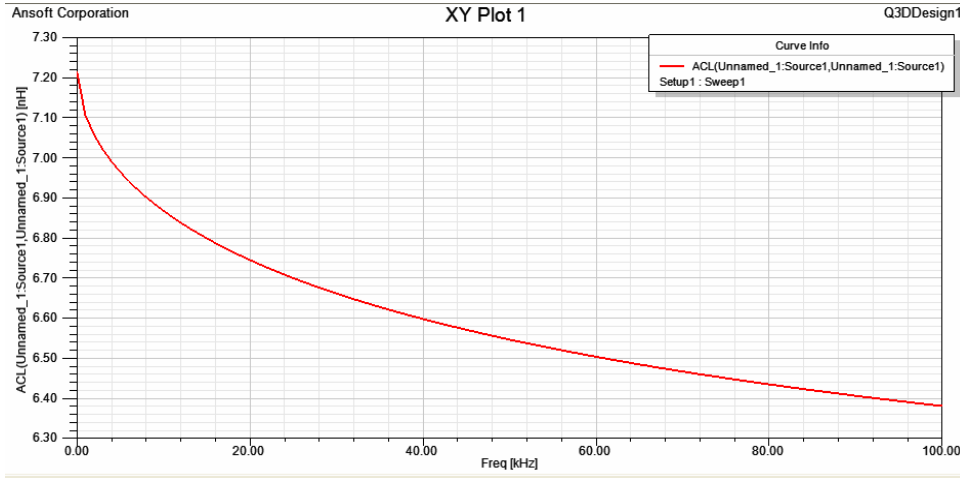


Figure 20 — TO220-3 Package Inductance vs. Switching Frequency Simulate by Ansoft

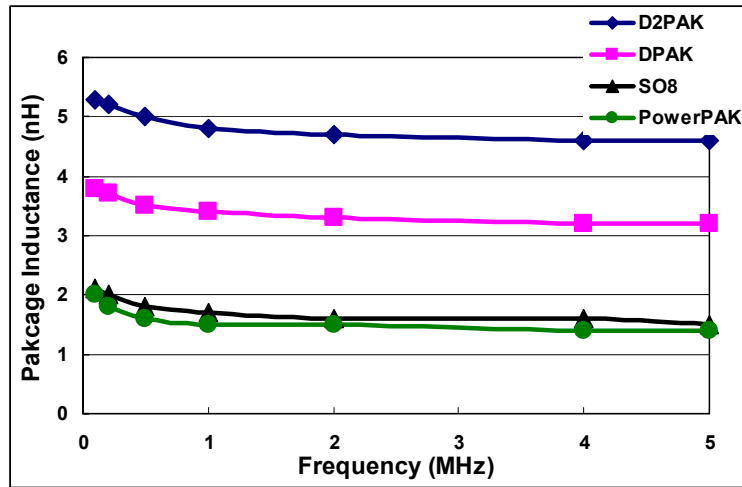


Figure 21 — Surface Mount Packages Inductance vs. Frequency

For the CCM switch current turn-off slew rate di/dt , it can be derived as:

$$\frac{di}{dt} = \frac{V_D}{L_S} \tag{17}$$

$$V_D = V_{OUT} + V_{IN_DC} / n \tag{18}$$

Where V_D is the Flyback secondary side voltage, V_{IN_DC} is the input DC voltage, n is the transformer turn ratio from primary to secondary, L_S is the leakage inductance of the secondary transformer winding, which can be estimated as ~2%-3% of the secondary winding inductance.

Following is an example for a 20W universal input adapter application with CCM Flyback:

- Input AC voltage: $90V_{ac} \sim 265V_{ac}$ (V_{IN_DC} : 120V~380V)
- Output DC voltage V_{OUT} : 5V
- Primary winding inductance L_m : 1.8mH (leakage inductance: ~2%-3% of L_m)
- Transformer turn ratio : 15 (From primary to secondary)
- Switching Frequency : ~60kHz

Derived from (17) and (18), the secondary CCM turn-off di/dt for this case is around $60A/\mu s \sim 150A/\mu s$ due to the different input. With a TO220 package SR FET ($\sim 6.5nH$ package inductance at $60kHz$ from figure 20), the voltage drop on package inductance V_{LK} will be $400mV \sim 900mV$ according to (16). This voltage drop is much larger compared with the voltage drop on $r_{ds(ON)}$ and dominate the V_{DS} in (15) trigger $-30mV$ turn-off threshold of the IC affirmatively.

Figure 22 shows the test verification results for this 20W Flyback converter at low-line input, the drain-source voltage across SR FET rises to above $500mV$ as soon as the CCM current turn-off occurs, the CCM di/dt is $\sim 60A/\mu s$.

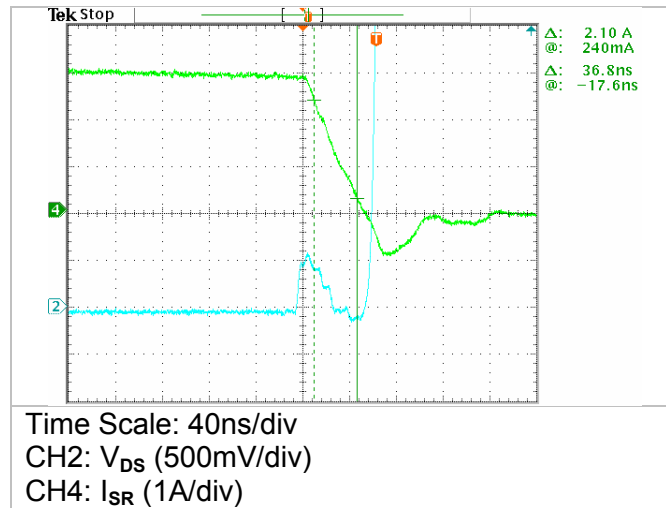


Figure 22 — Drain-Source Voltage Bounce at CCM Current Turn-Off Falling Edge

From above analysis, in CCM Flyback application, the MP6902’s turn off threshold is always tend to be triggered when the secondary CCM current turn-off falling edge occurs (t_1 in figure 19).

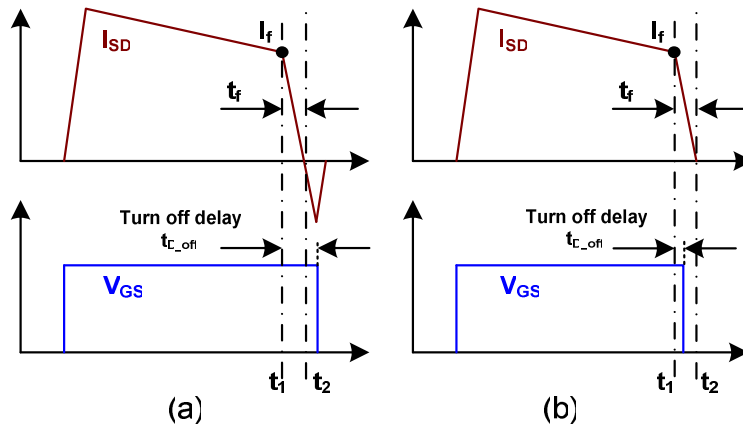


Figure 23 — CCM Turn Off of MP6902 in Flyback Converter

Figure 23 shows the different turn-off timing of the SR FET gate driver which affect the switching current (I_{SD}).

In figure 23(a), reverse current (shoot through) occurs due to the gate driver V_{GS} is turned off after switching current I_{SD} crosses zero (at t_2).

Although the IC's turn off threshold (-30mV) is triggered when switching current CCM turn-off occurs at t_1 , there is always a time delay between t_1 and gate driver's turn-off, which is so-called turn off delay (t_{D_off}), the t_{D_off} mainly include:

- Internal Logic Delay: the SR driver IC's response time, which is internal fixed.
- Gate Driver Falling Time: the time for the driver IC to pull down the SR FET's gate, depend on the dynamic characteristics of the MOSFET (Q_g etc.).

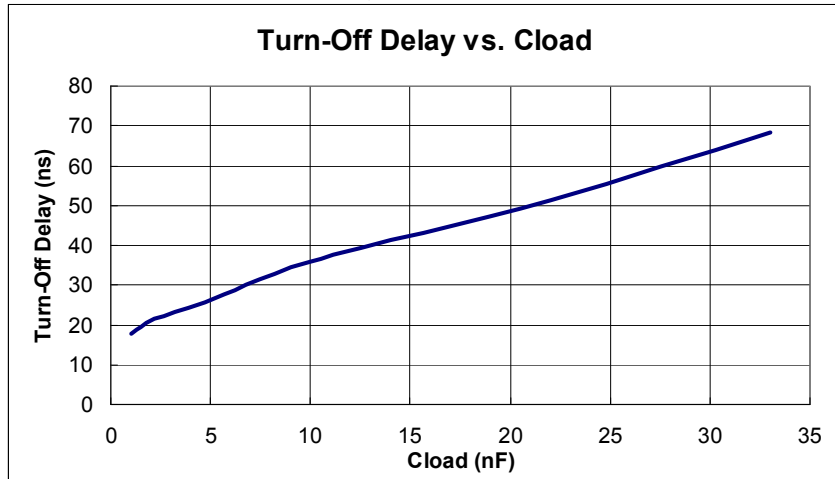


Figure 24 — Turn off Delay vs. C_{LOAD} for MP6902

Figure 24 shows the typical turn off delay of MP6902 with different capacitor load on gate driver. If this turn off delay is smaller than the CCM current turn-off falling time (t_f , from t_1 to t_2 in figure 23), no shoot through occurs, such like in figure 23(b).

The CCM current turn-off falling time in figure 23 can be derived as:

$$t_f = \frac{I_f}{di/dt} \tag{19}$$

Where I_f is switching current level when the CCM turn off occurs, di/dt is the turn-off current slew rate which can be derived from (17).

In Flyback CCM operation, I_f can be calculated as:

$$I_f = \frac{I_{OUT}}{1 - \frac{n \cdot V_{OUT}}{V_{IN_DC} + n \cdot V_{OUT}}} - \frac{n^2 \cdot V_{OUT}}{2 \cdot L_m \cdot f_s} \cdot \left(1 - \frac{n \cdot V_{OUT}}{V_{IN_DC} + n \cdot V_{OUT}}\right) \tag{20}$$

Where L_m is the transformer primary winding inductance, I_{OUT} is the output current and f_s is the system switching frequency.

From figure 23, known that in order to avoid reverse current lead by shoot through in CCM Flyback with MP6902, it is preferred $T_{D_off} \leq t_f$ to make sure the gate driver be pulled down before switching current drops to zero.

But when the Flyback system operates in CrCM, in which condition I_f in (20) is nearly zero, the reverse current (I_{rr}) lead by shoot through will easily occurred, see figure 25:

$$I_{rr} = \frac{di}{dt} \cdot (t_{D_off} - t_f) \approx \frac{di}{dt} \cdot t_{D_off} \tag{21}$$

When apply MP6902 in a CCM Flyback system, we need always to take such critical (CrCM) conditions into consideration, which may has highest reverse current or voltage spike.

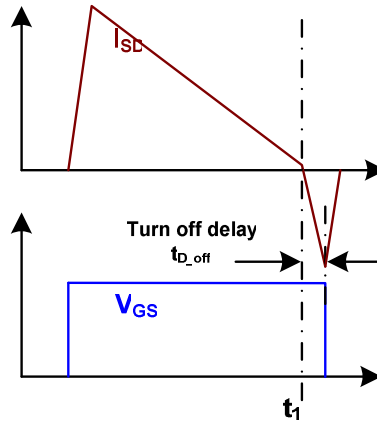


Figure 25 — CrCM Turn off of MP6902 in Flyback Converter

Basically there are two critical conditions which need to pay attention to:

- i. At steady state: with the input voltage when the system is working in CrCM at full load condition.
- ii. At system transient (start-up etc.): system output start-up with maximum input voltage, during which the system may also works in CrCM.

Following are some design guides which to reduce the reverse current and voltage spike on SR FET for these critical conditions:

- Design proper snubber network on SR FET to absorb the energy lead by the reverse current to avoid high voltage spike on MOSFET. Refer to “RC Snubber Design Guide” section.
- Select the SR FET with smaller Q_g , which help to reduce the t_{D_off} . Basically we can evaluate our desired t_{D_off} based on figure 14 and equation (12):

For example, if we hope the maximum voltage spike V_{F_MAX} be less than 1.5 times of V_D , then known from figure 14, to get $V_{F_MAX}/V_D \leq 1.5$, we need to design $y \leq 1$:

$$y = \frac{I_{rr}}{V_D} \cdot \sqrt{\frac{L_S}{C_S}} \leq 1$$

Because L_S , C_S (selected as 2~3 times of C_P , can preset a certain value) value is already known, we can get the desired reverse current level as follows:

$$I_{rr} \leq V_D \cdot \sqrt{\frac{C_S}{L_S}}$$

According to equation (21) for the reverse current in critical condition, the desired t_{D_off} is finally derived as:

$$t_{D_off} \leq \frac{V_D \cdot \sqrt{\frac{C_S}{L_S}}}{dl/dt}$$

- Add totem-pole circuit on driver to increase the sink ability, which could help to decrease the gate driver falling time during turn-off.
- According to (17), increase the leakage inductance of the transformer is an effective way to make dl/dt smaller. A small saturable core put in series with the primary winding is also helpful to decrease the dl/dt .

By above actions, we need to make sure that the BV of the SR FET never be crossed in such critical conditions to ensure the system’s safety with MP6902.

CCM Flyback SR Design Example with MP6902

A detailed Flyback SR design example based on a 20W universal input adapter will be presented in this section. The system specification is as following:

- Input Voltage V_{IN_DC} : 120V to 380V (85VAC to 265VAC)
- Output DC voltage V_{OUT} : 5V
- Output Current I_{OUT} : 4A
- Transformer turn ratio n : 15
- Transformer inductance L_m : 1.8mH
- Switching frequency f_s : 60kHz max
- Secondary-side leakage inductance L_S : ~0.2uH (Refer to “RC Snubber Design Guide” section for how to get this value)
- RC snubber Capacitor C_S : 2~3 times of C_P , preset as 2.2nF

This Flyback system is designed to operate in CCM at full load with low line input, while at high line input, the system will always operate in DCM at steady state.

So considering the CCM operation, get the secondary CCM current turn-off slew rate di/dt according to (17) and (18):

$$\frac{di}{dt} = \frac{V_D}{L_S} = \frac{V_{OUT} + V_{IN_DC} / n}{L_S}$$

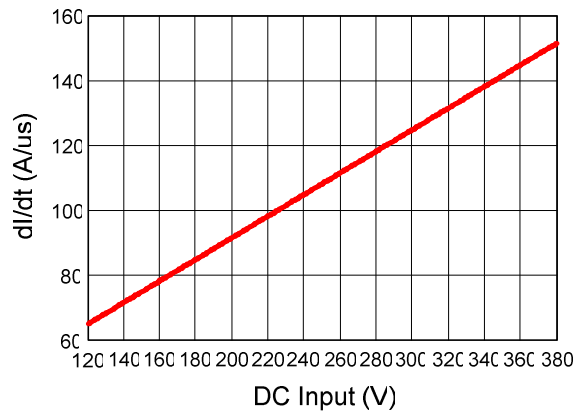


Figure 26 — Secondary CCM Current Slew Rate

Figure 26 shows the SR CCM current slew rate. Because the system is designed work at CrCM at full load in ~170VAC (240V DC) input, the critical conditions which may occur highest reverse current or voltage spike for this case is:

1. Steady state: 170VAC (240V DC) input, full load condition. (~100A/us di/dt according to figure 25)
2. System start up: 265VAC (380V DC) input, full load condition. (~150A/us di/dt according to figure 25)

For this 5V output Flyback system, the maximum V_D from (18) will be ~30V, so a 60V MOSFET is selected. Considering 25% margin for the BV of the SR FET, it is desired that the maximum voltage spike on SR FET (V_{F_MAX}) be less than ~45V, which means $V_{F_MAX}/V_D \leq 1.5$.

So from figure 14 and equation (12), to make $V_{F_MAX}/V_D \leq 1.5$, the y value in (12) should follow:

$$y = \frac{I_{rr}}{V_D} \cdot \sqrt{\frac{L_S}{C_S}} \leq 1 \tag{22-a}$$

$$L_S = 0.2\mu\text{H}; C_S = 2.2\text{nF} \tag{22-b}$$

Put (21) and (22) into the two critical conditions for this case:

1. Steady state, 170VAC (240V DC) input:

$$I_{rr} = t_{D_off} \cdot 100\text{A}/\mu\text{s} \leq 2.2\text{A} \tag{23-a}$$

2. System start up, 265VAC (380V DC) input:

$$I_{rr} = t_{D_off} \cdot 150\text{A}/\mu\text{s} \leq 3.15\text{A} \tag{23-b}$$

From (23), we can get the desired T_{D_off} for this case is $\sim 22\text{ns}$. Then select the 60V SR MOSFET as AM90N06 from Analog Power, which has about 25ns turn-off delay according to figure 24.

After determine the t_{D_off} , maximum I_{rr} can be get then from (21). Then design the R_S for the RC snubber network (refer to “RC Snubber Design Guide” section), which is $\sim 12\Omega$.

Verify the design in bench test for the two critical conditions, check the reverse current and voltage spike which is in figure 27 and figure 28.

From the bench verification results, we can see that the reverse current and voltage spike in both critical conditions are within the desired target.

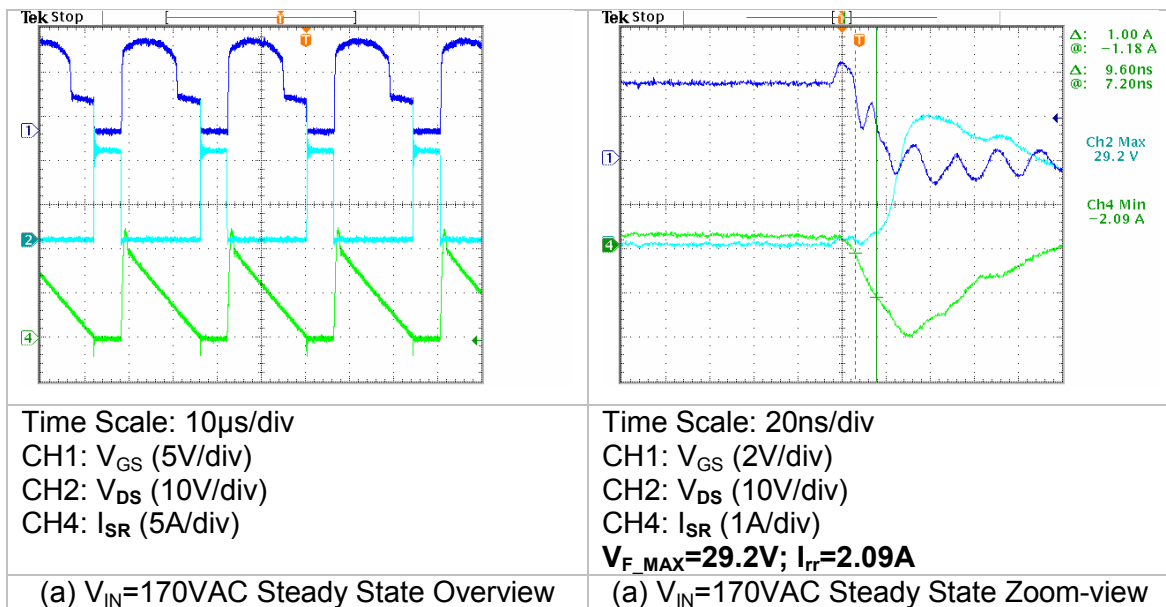


Figure 27 — Reverse Current and Voltage Spike in the Critical Condition (Steady State)

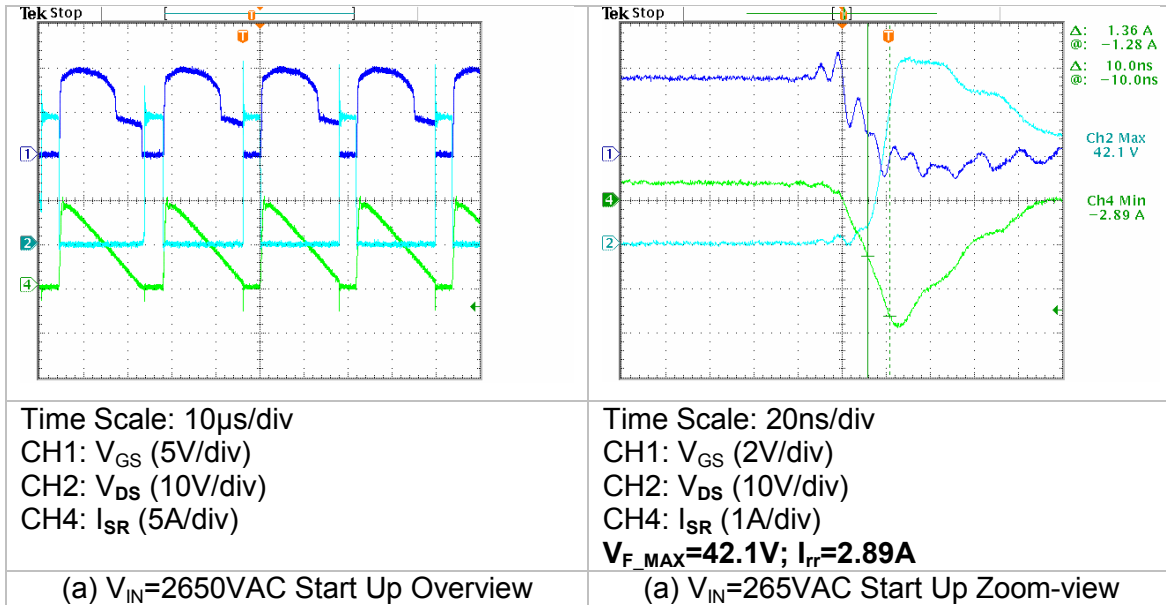


Figure 28 — Reverse Current and Voltage Spike in the Critical Condition (Start Up)

Sometimes you may find some error between the calculation and experimental results, which makes the bench verified reverse current and voltage spike exceed your desired target, or you may find the calculated t_{D_off} from (22) and (23) is so small which you can't select proper SR MOSFET. In these cases, you may need to:

- Select the C_S larger, recalculate the desired I_{rr} and t_{D_off} according to (22) and (23). Recalculate R_S for the RC snubber.
- Make the L_S larger, recalculate the di/dt in (17) and desired I_{rr} , t_{D_off} according to (22) and (23). Recalculate R_S for the RC snubber.

Figure 29 shows the summarized design procedure for applying MP6902 in CCM Flyback system.

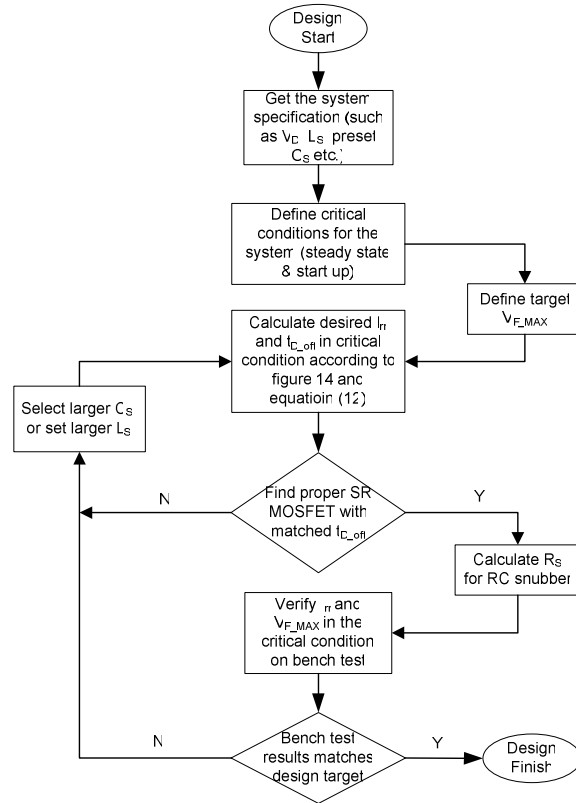


Figure 29 — MP6902 Design Procedure in CCM Flyback System

LAYOUT CONSIDERATIONS

Listed below are the main recommendations which should be taken into considerations when designing the PCB with SR driver in a Flyback converter:

Sensing for V_D/V_{SS}

The sensing connections (V_D/V_{SS} pin) must be as close as possible to the MOSFET (drain/source). Make the sensing loop as small as possible, put the IC out of the power loop to make sure the sensing loop and power loop won't interfere each other. (See figure 30)

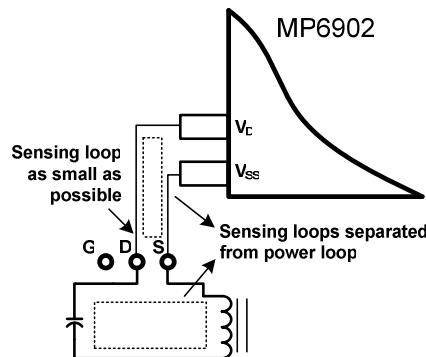


Figure 30 — Voltage Sensing for V_D/V_{SS} on SR Driver

V_{DD} Decoupling Capacitor

A decoupling ceramic capacitor (no small than 1 μ F) from V_{DD} to PGND is recommended to be put close to the IC in order to get adequate filtering.

Gate Driver Loop

In order to minimize the parasitic inductance, the gate driver loop is recommended to be as small as possible. Leave the driver signal far away from the V_D sensing trace on the layout.

Layout Example

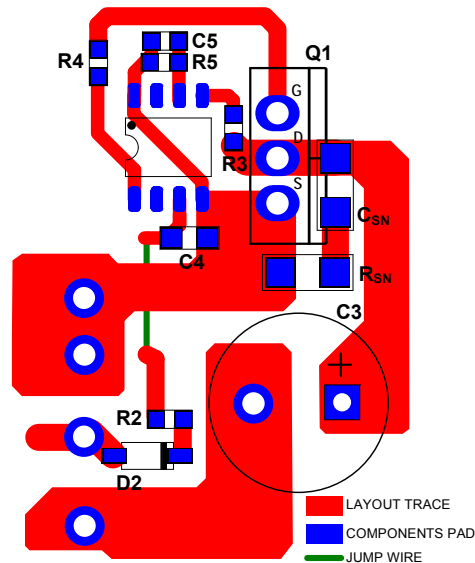


Figure 31 — Single Layer with TO220 Package SR FET

Figure 31 shows a layout example of single layer with a through-hole transformer and TO220 package SR FET, correspond with the application circuit in figure 1 (R_{SN} and C_{SN} are the RC snubber network for the SR FET).

The sensing loop (V_D/V_{SS} pin to the SR FET) is minimized and separate from the power loop, V_{DD} decoupling capacitor (C_4) is put just beside the V_{DD} pin.

Figure 32 shows another layout example of single layer with a PowerPAK/SO8 package SR FET, which also has a minimized sensing loop and power loop without interfering each other.

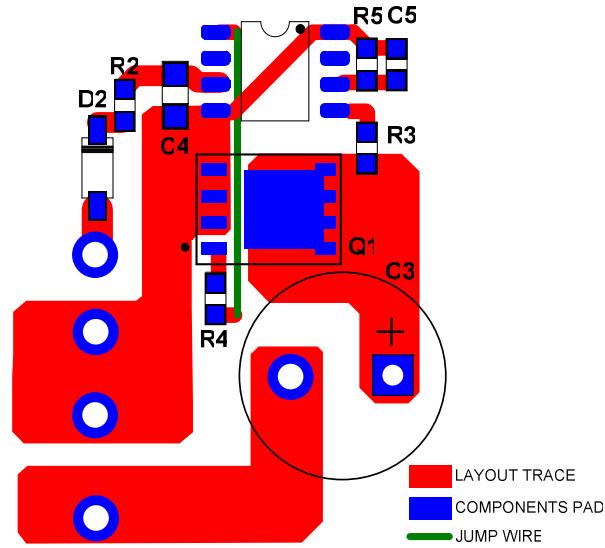


Figure 32 — Single Layer with Power PAK/SO8 Package SR FET

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