

# PCB Layout Design Guidelines for MP2932+MP86884

## Application Note

*Prepared by Wei Yuan*

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## ABSTRACT

This application note gives the detail layout guidelines for MPS high current VR solution--MP2932+MP86884, combined with AN057, this AN focus on how to make a proper PCB layout and then reach an optimal and stable operation.

### Layout for High Current Intergrated intelli-phase

Other than the traditional VR power solution that makes driver and MOSFETs separately, MPS provides a high power density integrated solutions for the driver and MOSFETs, with output current around 40A in a small QFN6\*6 package, named as Intelli-phase, this kind of integrated structure makes the converter much smaller and can also reduce the leakage parameters, contribute to higher switching frequency and also higher efficiency by optimal dead time control. However, the advantage of the fully integration of the driver logic and power FETs makes these parts noise sensitive once the PCB layout is not well designed, what worse is, the leakage inductance from a poor PCB layout may cause strong ringing and then deteriorate the reliability and efficiency, hence, a carefully designed PCB Layout is required to ensure a proper operation.

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## INTRODUCTION

### How Important a Layout is to the High Current DC-DC Converters

The MP2932+MP86884 is a compact high efficiency power solution for high current power supply, etc., CPU, it can support up to 240A output current by one controller(MP2932) and interleaved intelli-phase(MP86884). For these highly integrated devices with high current and high switching frequency, a poor layout will degrade the performance of the converter, cause ground bounce, EMI problems, resistive power loss, high voltage stress on power FETs, poor line and load regulation and even system instability. Hence, a good layout is one of the key factors in the switching mode power supply system

### General Design Guidelines

There are some general design guidelines for a proper layout. Generally, the MP86884 is the power device so that it requires more careful design layout, and what need to be done for MP86884 is noise immunity and remote sense.

#### 1. For MP86884:

- 1) The power trace (IN, PGND, SW) should be placed short and wide with minimized loop area. That means, the input capacitor should be placed as close as possible to the IC, etc., placed next to IN and PGND, the inductor should be placed close to the SW PIN and connect directly to the output capacitor.
- 2) The VDD decoupling capacitors should be placed close to VDD and VSS PIN, for each phase of MP86884, connect its VSS to inner PGND layout by vias. The VDDDRV decoupling cap should also be connected next to the VDDDRV and PGND.
- 3) For a better thermal performance, at least two layers are required to form IN and PGND trace, add several Vias with 10mil\_drill/20mil\_copper width in the bottom and also close to the IN and PGND pads to help on thermal dissipation. And 8 layers are the Min requirement for the PCB board
- 4) The sensitive traces like VDD and CS (current sense), remote sense (VSEN, RGND), should be placed far from high dv/dt signals, ( e.g SW, PWM, BST).
- 5) Keep the BST voltage path (path from BST to SW) as short as possible with at least 25mil trace. and put the BST cap as close to the device as possible.

#### 2. For MP2932:

- 1) The VCC decoupling capacitor should be placed close to VCC and connected to inner PGND layer by vias.
- 2) The remote sense point should be connected to the sense point near CPU separately with small loop traces, do not mix the VSEN and RGND with any other signal. 3) The noise sensitive

trace (FB, CS, VCC) should be placed far away from SW, PWM or BST trace. 4) Suggest no via on FB pin, that means put the compensation loop parameters in the same layer with the controller.

## CRITICAL DESIGN NOTES FOR THE PCB LAYOUT

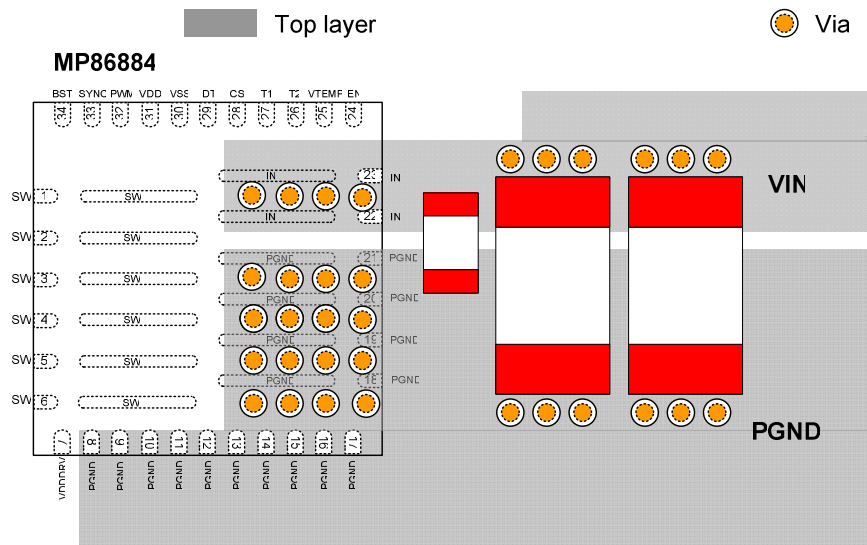
The above section describes some general layout recommendations that should be considered, this section will focus on some specific layout suggestions that are quite important for this system. One should strictly follow these design notes for a better and strong performance.

### Input Capacitor

#### 1) Input Cap without Forbidden area

For the main power loop, the input capacitors should be placed as close to the IN and PGND pins as possible, these connections should be done with short, direct and wide traces. The decoupling cap, usually the smallest ceramic cap, should be placed most close to the IN and PGND pins of the MP86884, so as to make the best decoupling effect.

Figure 1 describes the optimized input cap placement based on MP86884



**Figure 1—Optimized and recommend input capacitor placement**

The input cap should be carefully placed to reduce the leakage inductance, or else, the high voltage spike caused by the  $di/dt$  would cause extra voltage stress to the HS MOS. Layout shown in Figure 2 are some common unqualified VIN capacitor layouts which will degrade the performance and stability.

For Figure 2-a), the input cap is put far away from Vin and PGND pins, this will increase the leakage from Vin Cap to HS MOS, leading to higher voltage stress during switching periods. This layout is quite common because of the forbidden area.

For Figure 2-b), the input cap is placed quite close to the IN pin, however, the cap that placed closest to IN and PGND should be the ceramic decoupling Cap, not the Bulk Cap.

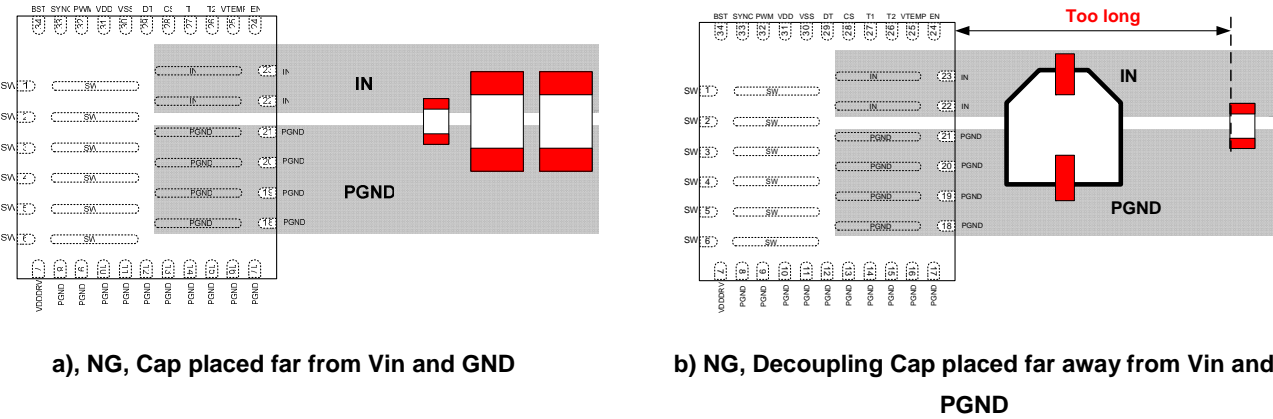


Figure 2— Unqualified input capacitor placement

2) Input Cap with Forbidden area

In some of the applications, there is a forbidden area around the IC, and it is not allowed to put the decoupling cap close to the IC inside the forbidden area. In this case, it is strongly recommended to place a ceramic cap in the bottom of the part, Figure 3 shows the recommend input capacitor layout for applications with forbidden area

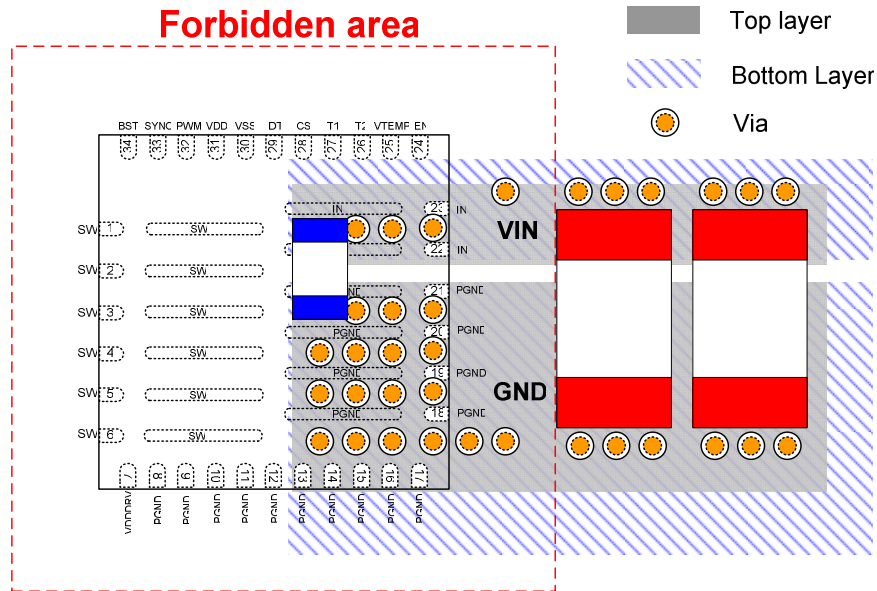


Figure 3—Recommend input capacitor placement for applications with forbidden area

### VDD/VDDDRV Decoupling Capacitors

The VDD/VDDDRV are 5V inputs that powers internal logic/driver of MP86884, the decoupling capacitors plays an important role in the DC-DC converters to make the logic circuits not noised coupled and also limit the driver leakage inductance.

The VDD/VDDDRV cap is required to be placed as close to the VDD/VDDDRV pin as possible. It is highly recommended to put these caps in the same layers with the MP86884 so that less or no via is required since via will induce additional leakage inductance.

Figure 4-a) describes the recommend VDDDRV cap placement. While Figure 4-b) has a VDD cap placed far away from VDDDRV and AGND pins, which is not good.

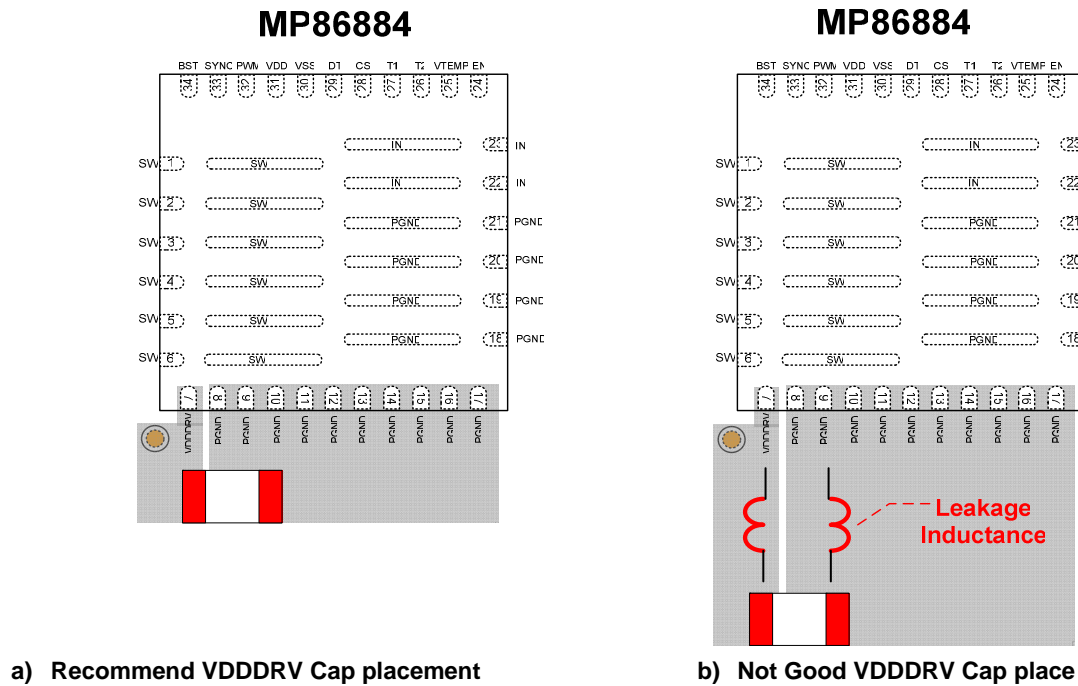


Figure 4—VDDDRV capacitor placement for MP86884

For the VDD decoupling Cap, it should be connected to VSS first before the VSS is connected to PGND. Figure 5-a) describes the recommend VDD cap placement; the cap is connected to VDD and VSS directly in the same layer of the MP86884. And VSS is then connected to inner PGND layer by vias near the cap. Figure 5-b) shows an improper cap to VSS connection, this improper layout will increase the leakage from cap to the VSS Pin, and the system might get noise affected sense the PGND is quite noisy.

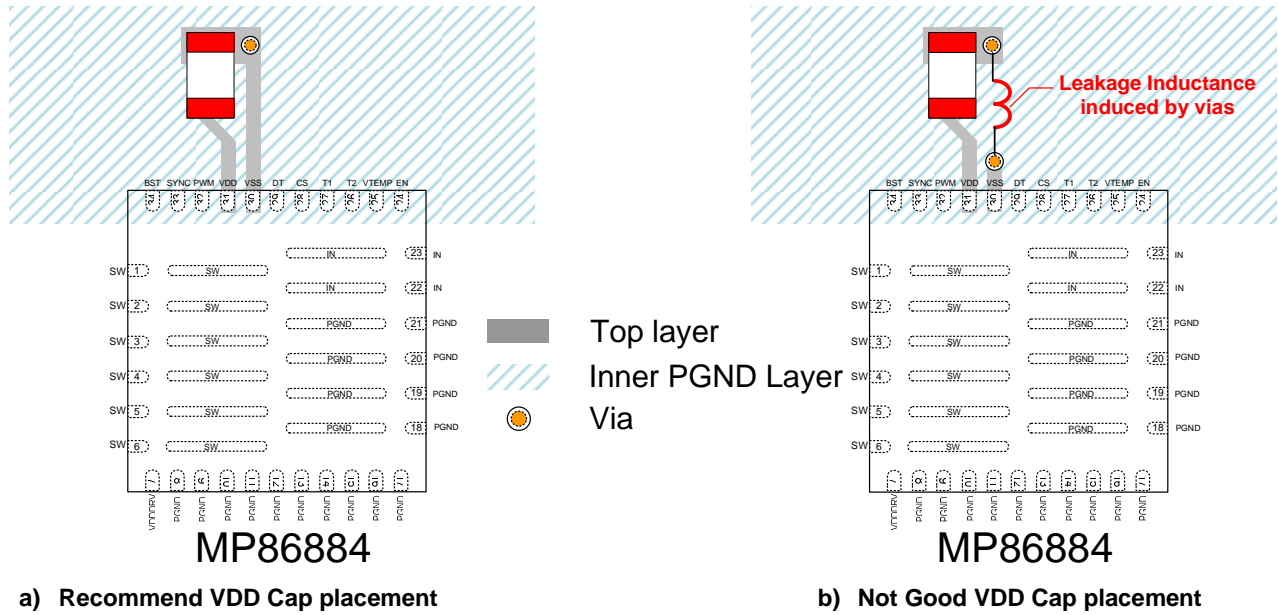


Figure 5—Recommend VDD capacitor placement for MP86884

**Enhance Input Power Trace**

The MP86884 series provides high power density solutions for DC-DC converters with output current up to 40A in a small QFN6\*6 package, hence, a better thermal design is expected to prevent the converter from a high temp rise. It is recommended that:

- 1) At least two layers is need for the IN and PGND power trace, keep it short, direct and wide, and connect the two layers with vias. These vias are recommended to have 10mil\_drill/20mil\_copper width.
- 2) The Vias placed under the part is quite important for the thermal dissipation, it also helps to reduce the leakage inductance to the power MOS. It is strongly recommended to place vias on the IN and PGND pins under the part.
- 3) Also, for a better thermal dissipation, place as many vias as possible (>20) between the two input trace layers next to the VIN and PGND pins around the input capacitors.
- 4) Do not place too much vias that will block the current flow, etc., room between outside input cap and MP86884's IN and PGND pins. See Figure 6 for details

Figure 5 and 6 describe the recommend layout for the enhanced IN and PGND trace. For Figure 5 the enhanced input layer is Top (IN and PGND, SW), inner1 (PGND) and inner2 (IN and PGND)



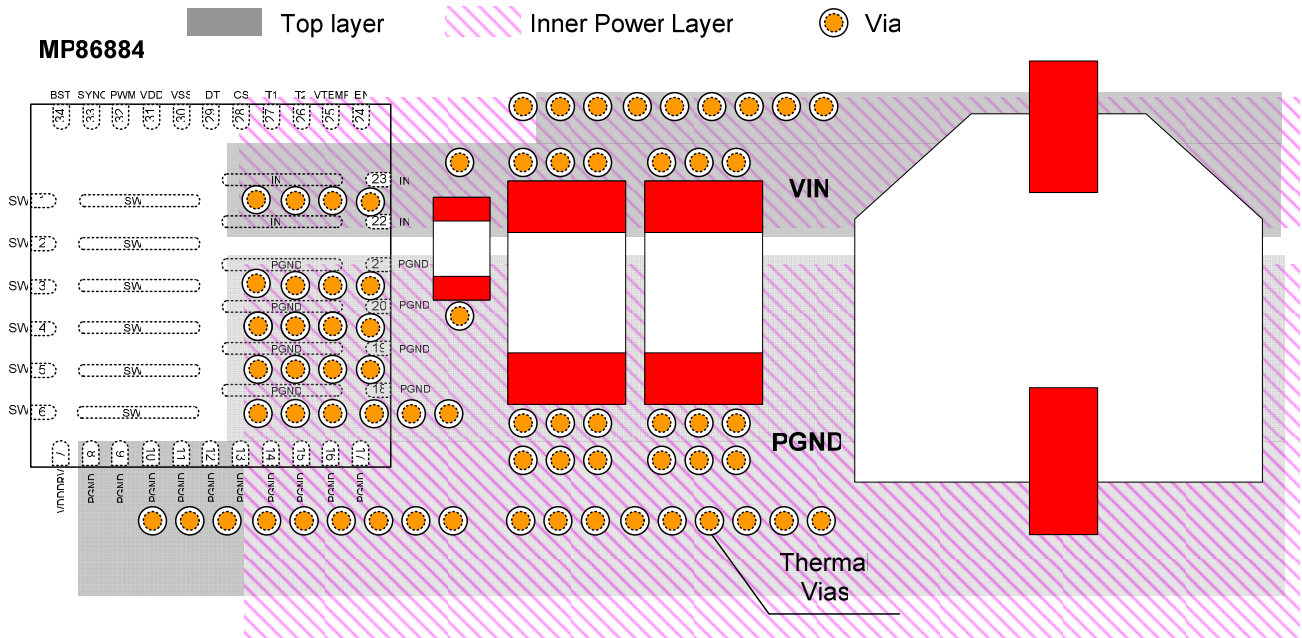


Figure 5—Recommend enhanced VIN and PGND Trace for MP86884

Figure 6 is the recommend layout when there is a bottom decoupling cap due to the forbidden area, the enhanced input layer is top (IN and PGND,SW), inner1 (PGND) and inner 7 (assume total 8 layers), bottom(IN and PGND)—refer to Figure 6.

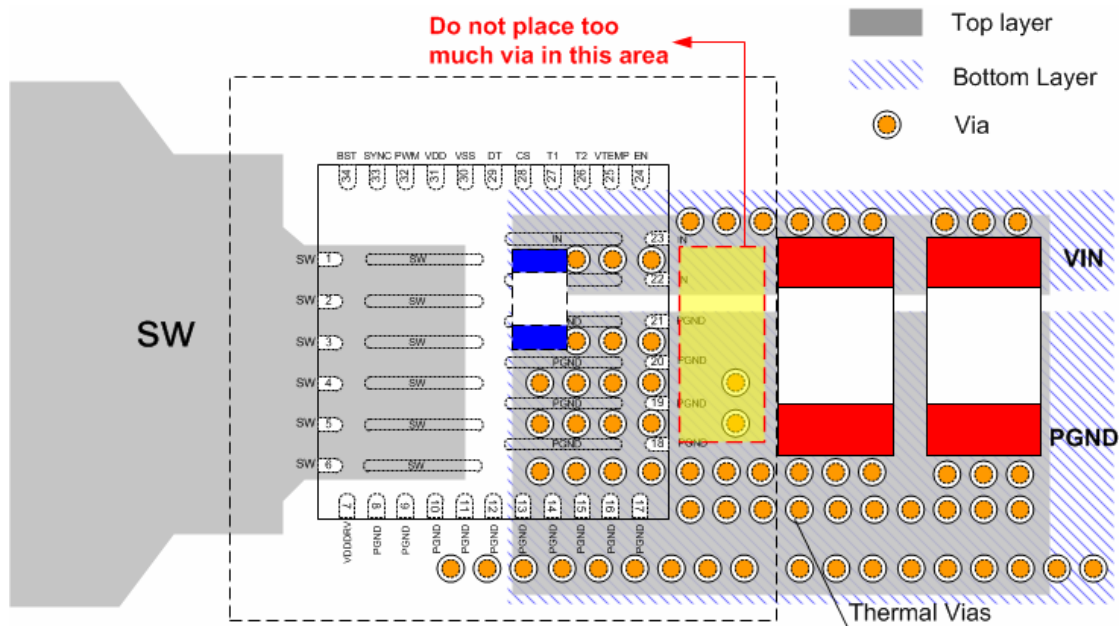
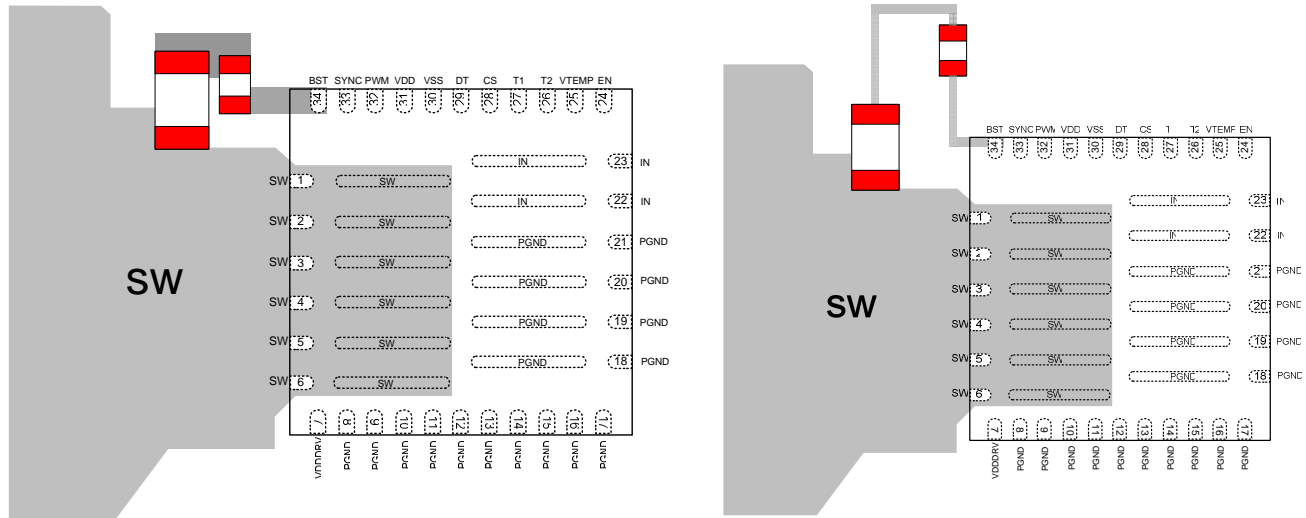


Figure 6—Recommend enhanced VIN and PGND Trace for MP86884 with Forbidden area

**BST RC Place and Trace**

The BST Cap provides a power source for the HS MOS driver, the BST node changes when SW switches, so it is recommended to shrink the loop from the BST to SW and also make the leakage inductance smaller by >25mil traces. Figure 8-a) shows the recommend BST RC traces, and Figure 7-b) presents an example of a not good BST trace.



a) Recommend VDD cap and resistor placement, small loop and with 25mil traces

b) Not Good BST trace

Figure 7—Recommend feedback resistors placement

**GND Connections**

For the MP2932+MP86884 solutions, there are several GNDs that should be designed carefully.

- 1) For the MP2932, it is a controller with no high power loop, so all the pull low(except the RGND) should be connected to a AGND pad before it is connected to PGND layer, so it is suggested to set a inner AGND island for MP2932, all the AGND(signal GND) near the chip would connected to this island first by vias, do remember that these vias are not connected to inner PGND layer, the inner AGND island should be connected to PGND with kelvin connections finally.
- 2) For the MP86884, the Input cap and VDDDRV Cap should be connected to PGND in the same layer with the IC, and the VSS should be first connected to the VDD Cap before it is connected to PGND layer by vias.
- 3) For the MP86884, each phase should have a separated GND traces before they are connected to inner PGND layer, that means, do not connected the PGND of one phase to VSS of another phase in the top or bottom layer.

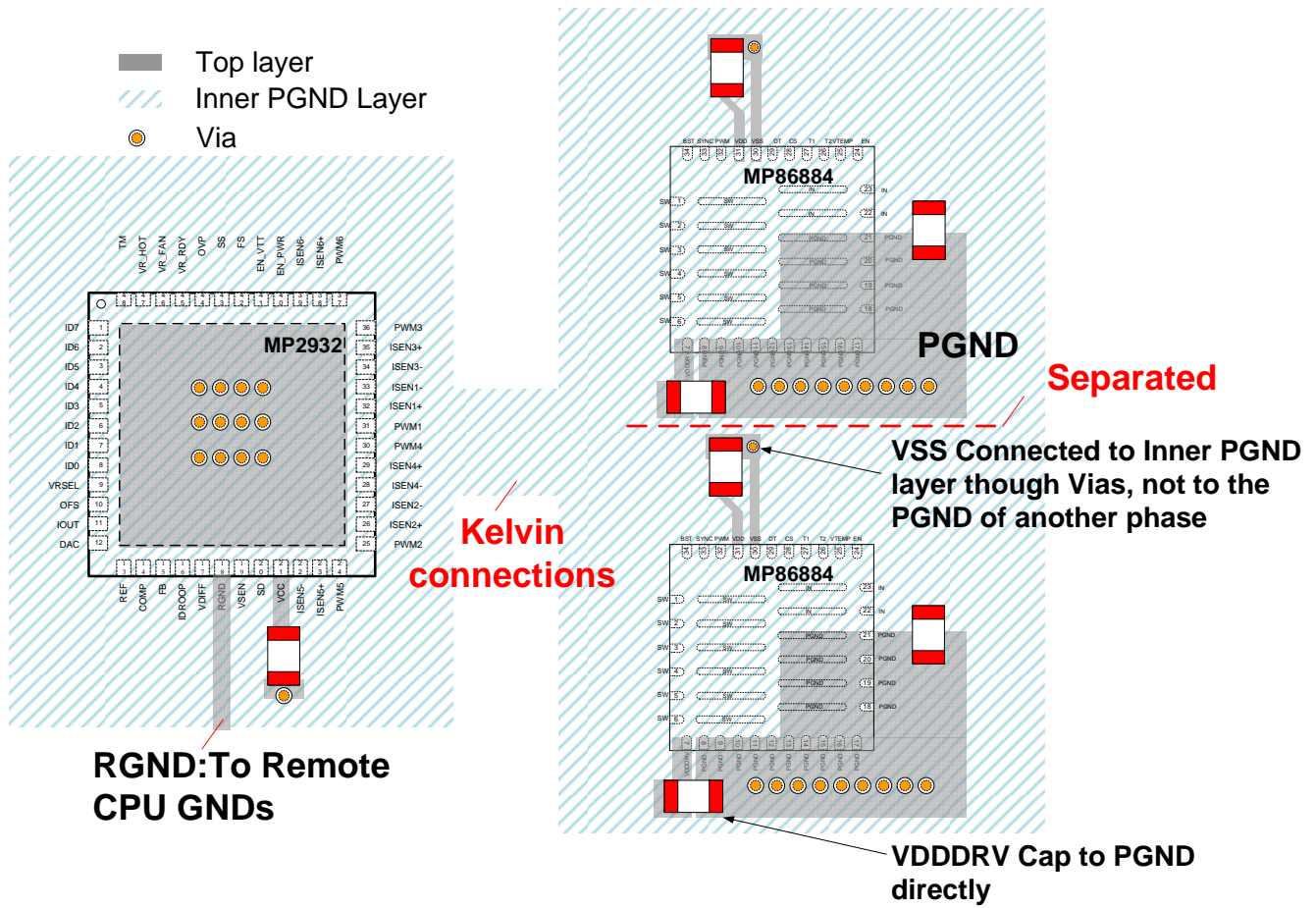


Figure 8—Recommend System GND connections

## GENERAL RECOMMEND PCB LAYOUT FOR MP86884

Based on above sections, the map of PCB layout with all the design noted included is shown below. We recommend use at least 8 layer PCB for the MP2932+MP86884 high current solution. The layer structure could be as follow.

### Recommend Layout For MP86884 without Forbidden Area

At least 8 layers board is required for our high current Intelli-phase. Make sure that there is PGND layer next to the main power layer so as to make a small power loop.

- 1) For the structure like Figure 9, the Min required main power loop will be in top 3 layers
- 2) Do not put the noise sense signal (such as CS, Vsen, FB, VDIFF) close to noise node (SW, BST or PWM), even they are placed in different layers, remember to separated them with proper distance.

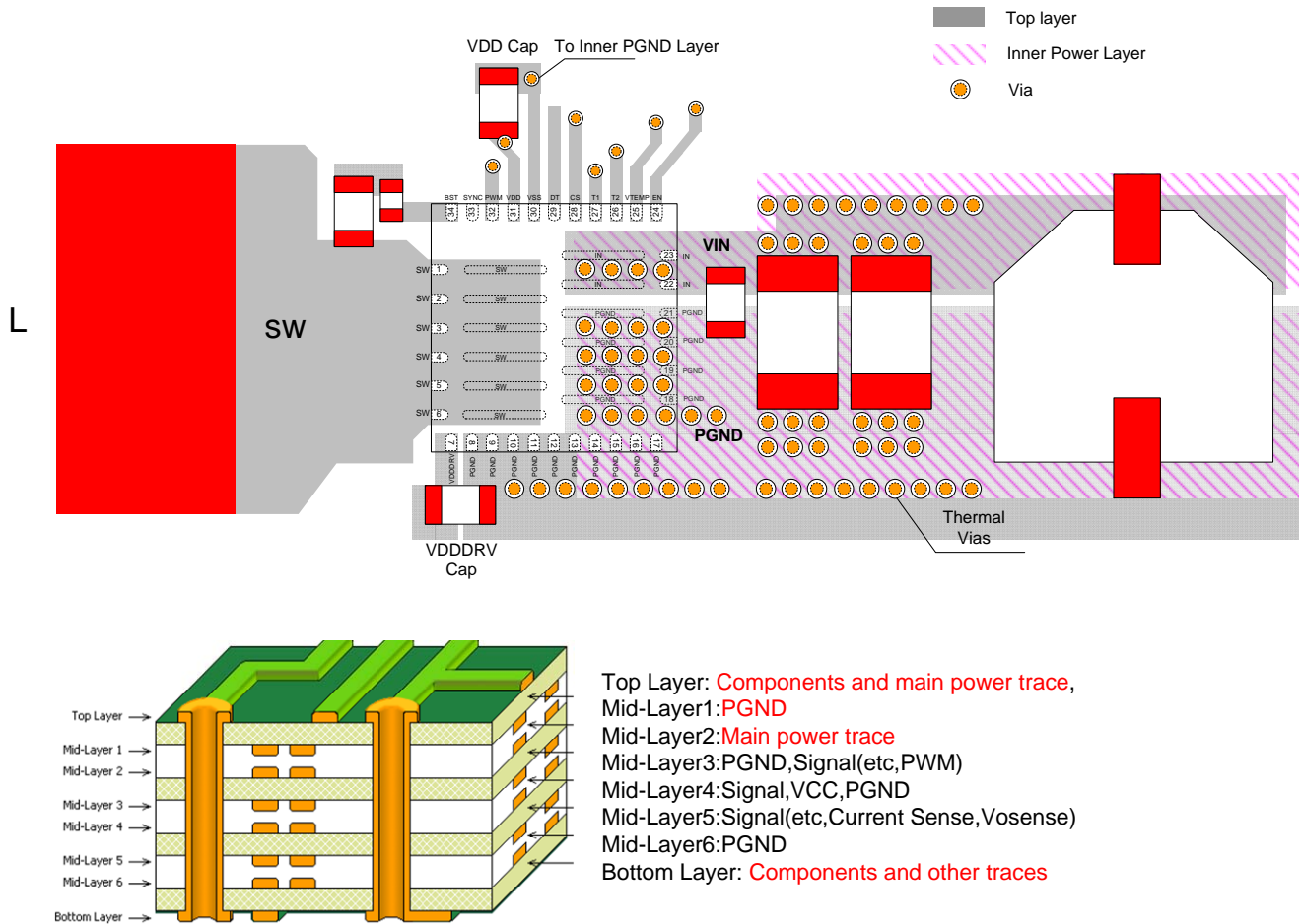


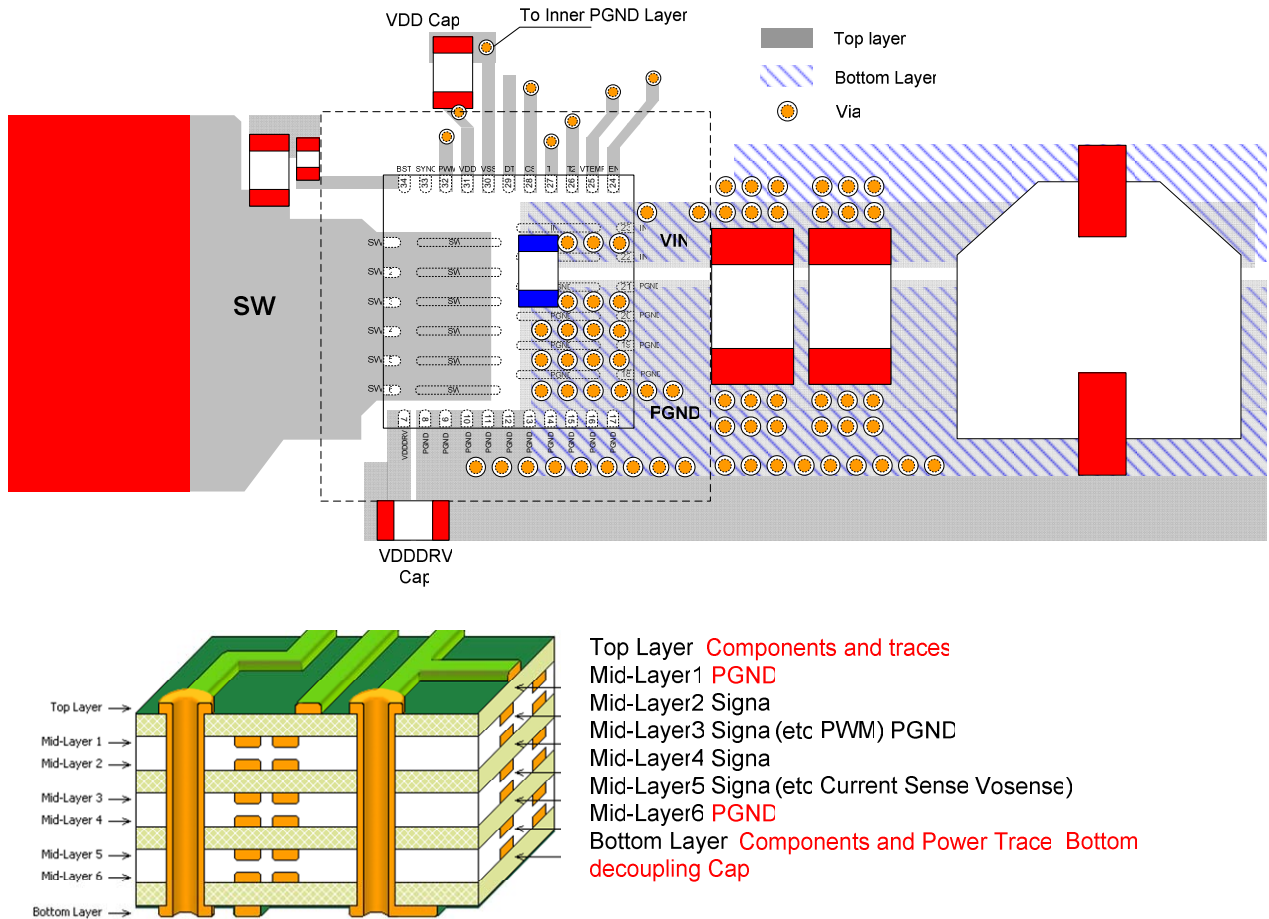
Figure 9—Recommend PCB Layout for MP86884

**Recommend Layout For MP86884 with Forbidden Area**

At least 8 layers board is required for our high current Intelli-phase. Make sure that there is PGND layer next to the main power layer so as to make a small power loop.

- 1) For the structure like Figure 10—with forbidden area, the Min required main power loop will be in top and bottom layers, also, with PGND layers next to the top and bottom layers, to reach a small power loop.

Do not put the noise sensitive signal (such as CS, Vsen, FB,VDIFF) close to noise node(SW,BST or PWM), even they are placed in different layers, remember to separated them with proper distance.



**Figure 10—Recommend PCB Layout for MP86884 with Forbidden area**

### MP2932 PCB GUIDELINES

Other than the GND connection that is described in the above section, there are some other notes for MP2932 layout.

#### Remote Sense on MP2932

The VSEN and RGND pin on MP2932 provides a way to accurately sense the output voltage from the remote load (CPU), hence:

- 1) The sense point should be placed near the CPU with separated wire. Do not connect the RGND directly to PGND layer, or connect the VSEN to Vout that is far from the CPU.
- 2) Suggest putting two 5-20ohms impedance match resistors in the remote sense wire, and a 10-100pF Cap (optional) for high frequency noise filter.

Figure 11 shows the details of the recommended remote sense of MP2932.

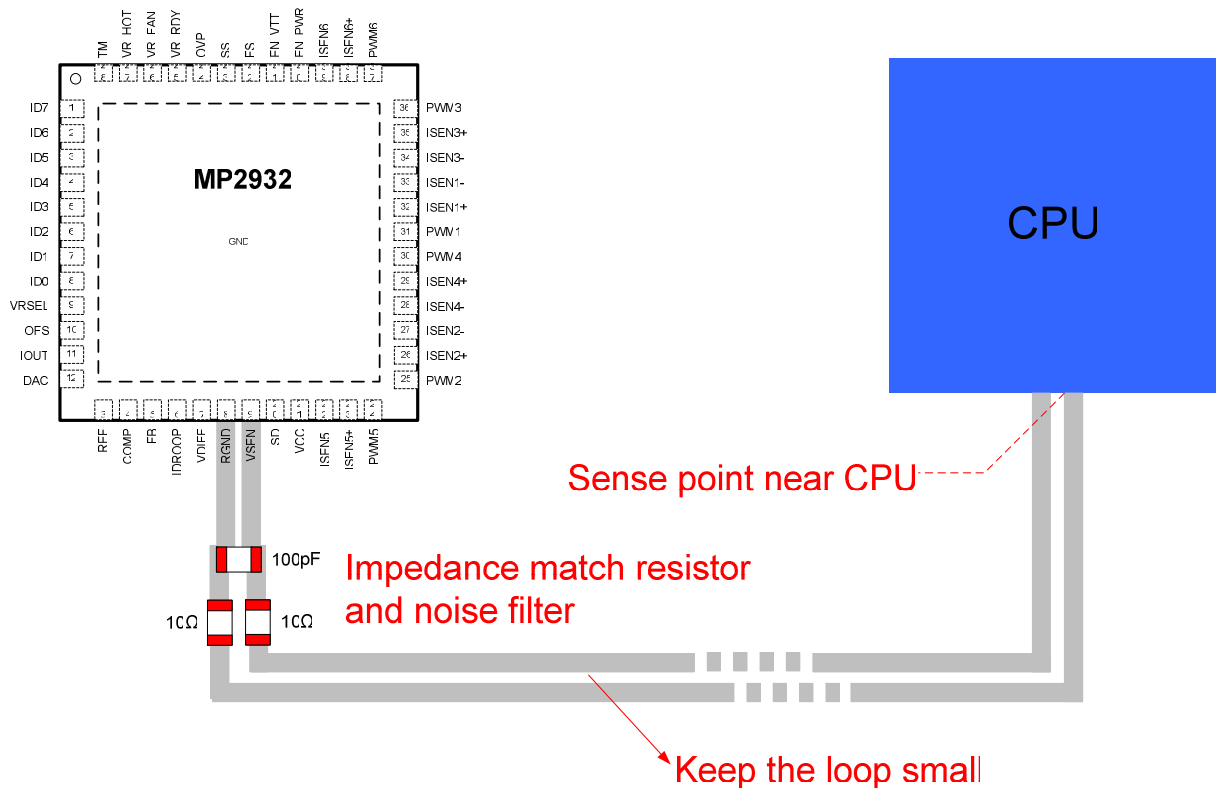


Figure 11—Recommend remote sense of MP2932.

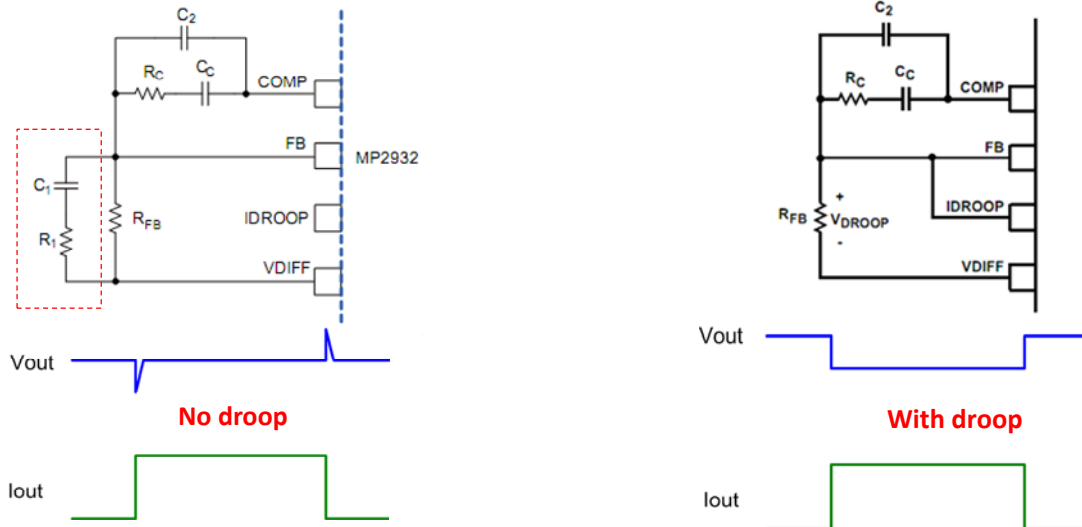
#### Feedback Loop of MP2932

The feedback loop plays an important role for the system stability, usually there are two kinds of compensation loop, type III and type II compensation as shown in Figure 12.

- 1) Type III compensation is commonly used for traditional no droop voltage mode control, where the output voltage keeps the same when load increase, as was shown in Figure 12-a), and It should be

noted that usually, type III compensation is suggested on the PCB Layout for it is also compatible for type II compensation where the droop function is applied, as shown in Figure 12 –b).

- Place a resistor footprint (Can be NS or 0ohm) between FB and IDroop pin if it is not decide to use droop or not. This is to increase the design flexibility.



- Type III compensation-suggested for no droop applications and PCB layout since the R1 and C1 can be NS
- Type II compensation, only applied when there is droop function.

Figure 12—Recommend compensation of MP2932.

- FB pin is noise sensitive, to avoid the leakage inductance, via is not allowed between FB pin and resistors/capacitors that are connected to it. So it is recommended that the feedback loop should be placed in the same layer with MP2932, as shown in Figure13.

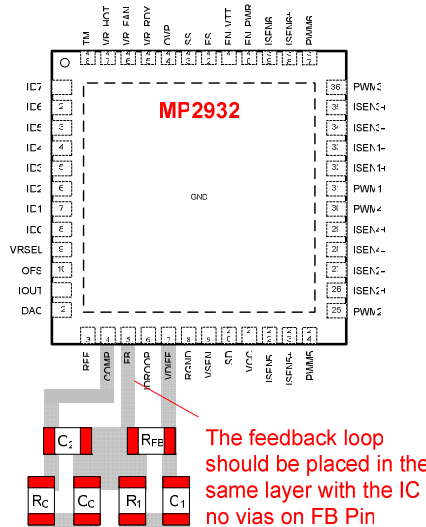
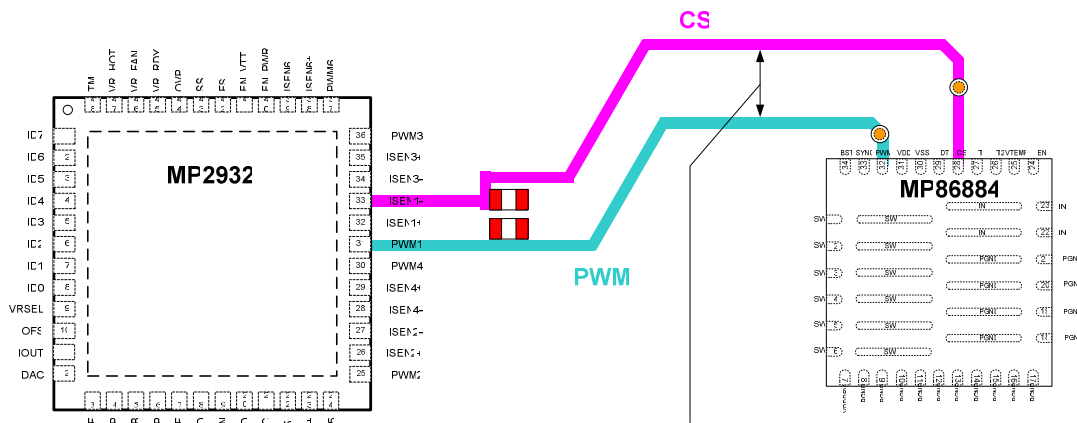


FIGURE 13—RECOMMEND COMPENSATION LOOP PLACEMENT.

### CURRENT SENSE FROM MP86884 TO MP2932

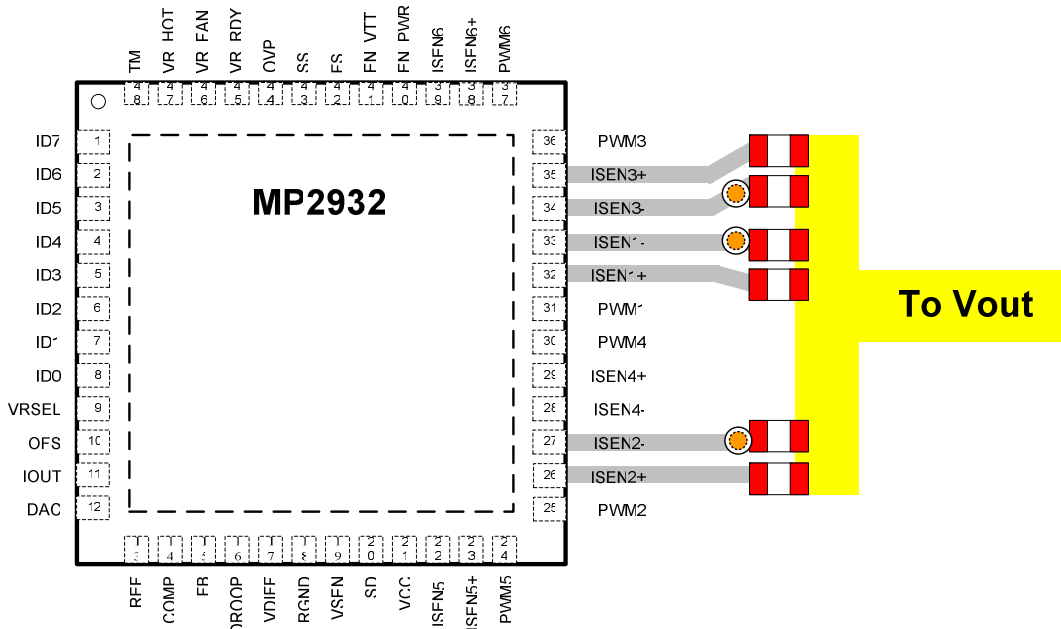
The communication signal between MP86884 to MP2932 includes CS and PWM, the PWM is noisy while the CS signal is noise sensitive for its current since accuracy, these two signals need to take good care for a better layout, generally, the layout should follow:

- 1, The distance from CS to PWM trace should be kept longer than 3 times of PWM width, usually >30mil, even if they are set in different layers, see figure. 14
- 2, The CS trace should also be kept away from SW pad, which is much more noisy than PWM.
- 3, The Vout point of the CS loop should be kept together before it is tied to output Cap.



**Keep Distance between PWM and CS of each phase, and CS signal should also keep distance from SW pad**

**Figure 14—Recommend CS and PWM signal placement.**



**Figure 15—Recommend Vout connection for CS Loop.**



## VR PLACEMENT

The VR module handles large current and the efficiency and thermal is quite important for the system reliability, the distance between VR and CPU will affect the copper impedance and also the leakage from VR to CPU, the copper impedance will cause higher conduction loss and then temperature rise, and the leakage inductance will affect the loop Bandwidth, so improve the efficiency and also simplify the loop design, it is suggest to put the VR as close to CPU as possible, and set the initial BW to  $1/10 F_s$ . Figure 16 shows the recommend VR module placement.

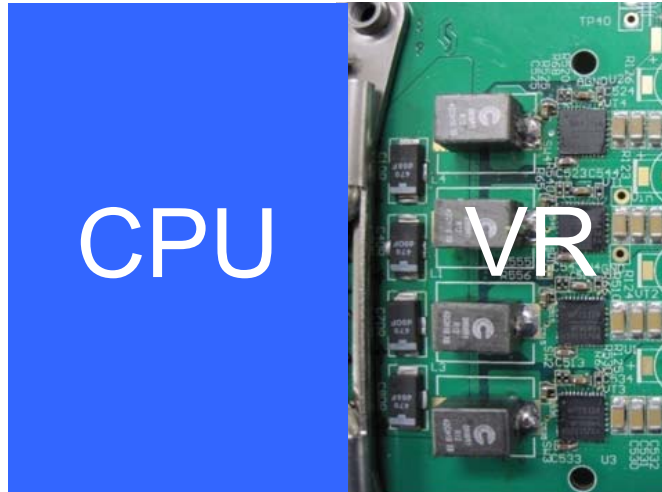


Figure 16—Recommend VR placement- place the VR close to CPU.

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