MP4020

Primary-Side–Control, TRIAC-Dimmable, Offline LED Controller Application Note

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1. INTRODUCTION

The MP4020 is a primary-side–control LED lighting controller with TRIAC dimming. Primary-side control can significantly simplify the LED lighting driving system by eliminating the opto-coupler and the secondary feedback components in an isolated single stage converter. Its proprietary real-current–control method can accurately control the LED current from the primary-side information. The MP4020 also integrates active power factor correction (PFC) with boundary-conduction mode operation.

This application note will introduce the basic function of MP4020, and then gives design examples that describe how to configure MP4020 for a TRIAC-dimmable LED driver with a single-stage power-factor–corrected flyback solution.

Figure 1 shows the MP4020 block diagram and simple application circuit. Detail design specification will be described in the next sections.

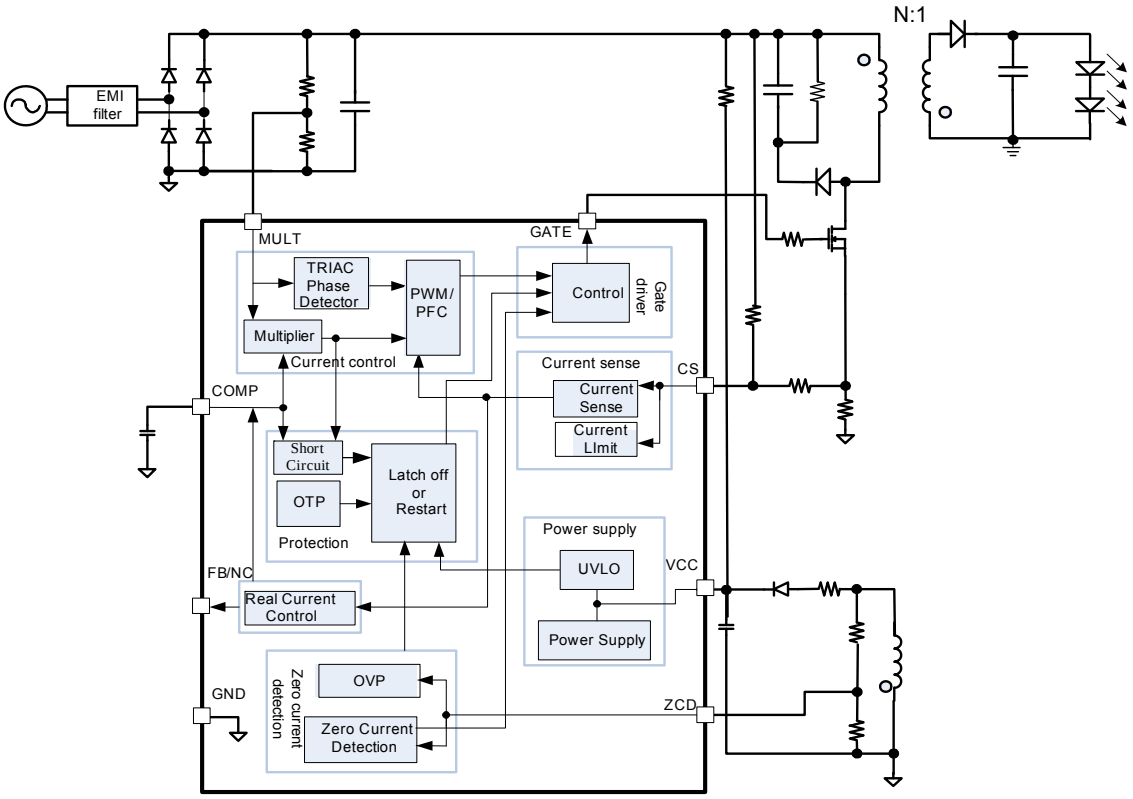

Figure 1—MP4020 Function Block Diagram and Typical Circuit

2. PRIMARY-SIDE–CONTROL, BOUNDARY-CONDUCTION–MODE OPERATION AND TRIAC DIMMING

2.1. Primary-Side–Control

The conventional off-line LED lighting driver usually uses secondary side control. The LED current is directly sensed from the transformer secondary side and comparared to a reference from a TL431. The EA output is compensated and fed to the primary side by an opto-coupler to determine the duty cycle that regulates the LED current. This control method has the advantage of directly and accurately controlling the LED current, but a substantial number of external components and circuits that significantly increase cost and system complexity.

As shown in Figure 1, the MP4020 uses primary-side–control, which eliminates the secondary feedback components. Given that the LED current is the average current of the secondary side during a half-line cycle ($I_o = I_{s\_avg}$), the MP4020 can calculate the average current of the transformer secondary side from the primary side current and control it with an internal reference voltage, this is the MP4020 primary-side-control principle. With the addition of a dimmer to the driver, MP4020 will detect the dimming phase and change the internal reference accordingly. So the average current of the LED will be proportional to the dimming phase and realize dimming function.

2.2. Boundary-Conduction Mode Operation

The MP4020 works in boundary-conduction mode (also canlled quasi-resonant mode), where the transformer works at the boundary between the continuous and discontinuous modes. Figure 2 shows the drain-source voltage waveform of the primary switch in a conventional current-mode flyback converter operating in discontinuous conduction mode (DCM). During the first time interval, the drain current ramps up to the desired current level, then the power MOSFET turns off. The leakage inductance in the flyback transformer rings with the MOSFET parasitic capacitance and causes a high voltage spike, which is limited by a clamp circuit. After the inductive spike has been damped, the drain voltage stabilizes to the input voltage plus the reflected output voltage. When the current in the output diode drops to zero, the drain voltage immediately drops to the bus voltage plus any ringing caused by the primary parasitic inductance and total parasitic capacitance.

For example, if the inductance is 1mH and the parasitic capacitance is 100pF, then the resonant frequency is ~500 kHz. The resonant circuit is lightly damped and the resonant frequency given below is independent of the input voltage and load currents:

$$f_{resonant} = \frac{1}{2\pi \cdot \sqrt{L_m \cdot C_{eqp}}}$$

Where L_m is the primary inductance; and C_{eqp} is the equivalent primary-side parasitic capacitance. C_{eqp} includes the parasitic capacitance of the primary winding, the parasitic capacitance of the MOSFET, and the parasitic capacitance of the secondary side (including the secondary winding and output rectifier diode) reflecting to the primary side.

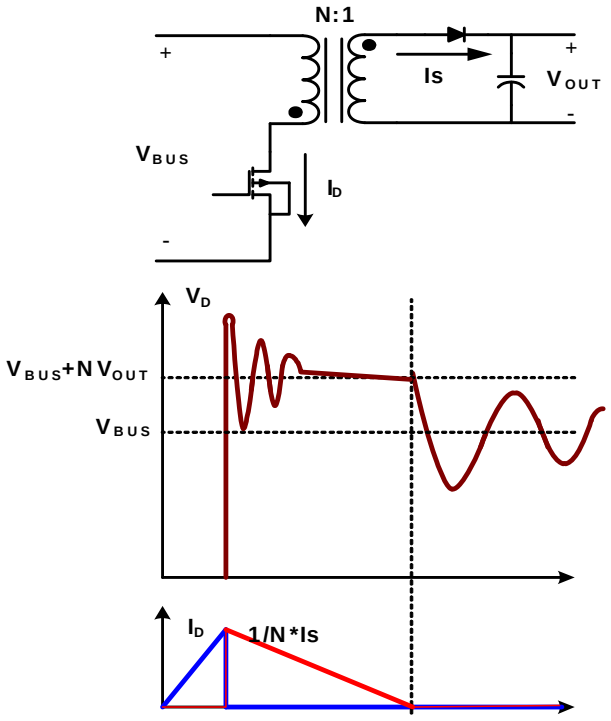

Figure 2—Single-Pulse of DCM Flyback Converter

In a conventional fixed-frequency flyback converter at DCM operation, the primary MOSFET turns on at a fixed frequency and turns off when the current reaches the desired level. The device may turn on at any point during the parasitic ringing. In some cases the device may turn on when the drain voltage is lower than the bus voltage (meaning low switching losses and high efficiency), and in some cases the switch will turn on when the drain voltage is higher above the bus voltage (meaning high switching loss). This characteristic is often observed in the efficiency curves of discontinuous flyback converters with a constant load, where the efficiency fluctuates with the input voltage and the turn-on switching loss changes due to the variation of the drain voltage at the turn-on point.

For the boundary conduction operation, the rectified input voltage is applied across the primary side inductor (Lm) and the primary current increases linearly from zero to its peak value (I_{pk}) during the external MOSFET on time (T_{ON}). When the external MOSFET turns off, the energy stored in the inductor forces the secondary side diode to turn-on, and the inductor current decreases linearly from I_{pk} to zero. When the current reaches zero, the resonance of the inductor with parasitic capacitance makes the MOSFET drain-source voltage decrease (see Figure 3). This decrease is also reflected on the auxiliary winding. A zero-current detector generates turn-on gate driver for the external MOSFET when the ZCD pin voltage is less than 0.35V. This ensures that the MOSFET will turn-on at a valley voltage (see Figure 3).

As a result, there are virtually no primary switch turn-on losses and no secondary diode reverse-recovery losses. This technique ensures high efficiency, lower temperature rise, and low electromagnetic interference (EMI) noise.

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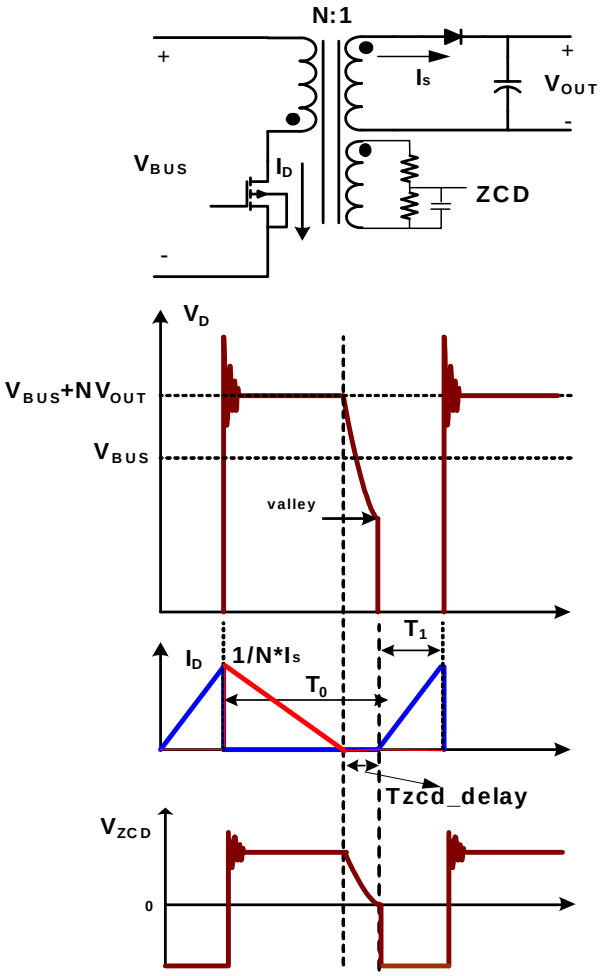


Figure 3—Boundary Conduction Mode

2.3. TRIAC Dimming

There are two kinds of phase-cut dimmers: leading-edge (TRIAC based, shown in Figure 4), and trailing-edge (transistor based, shown in Figure 5).

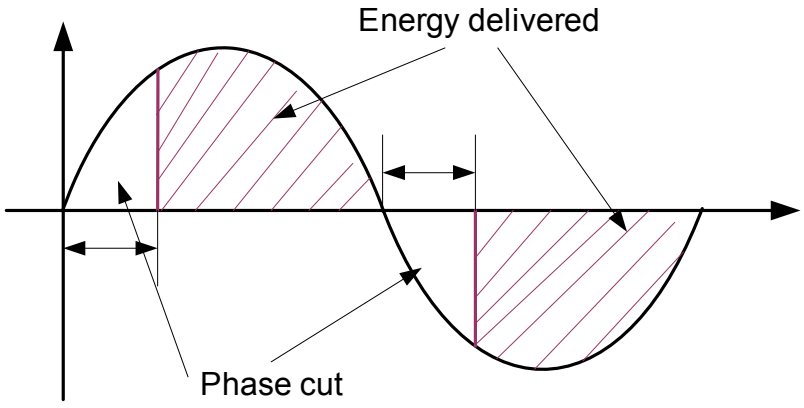


Figure 4—Leading-edge Phase Cut Mode

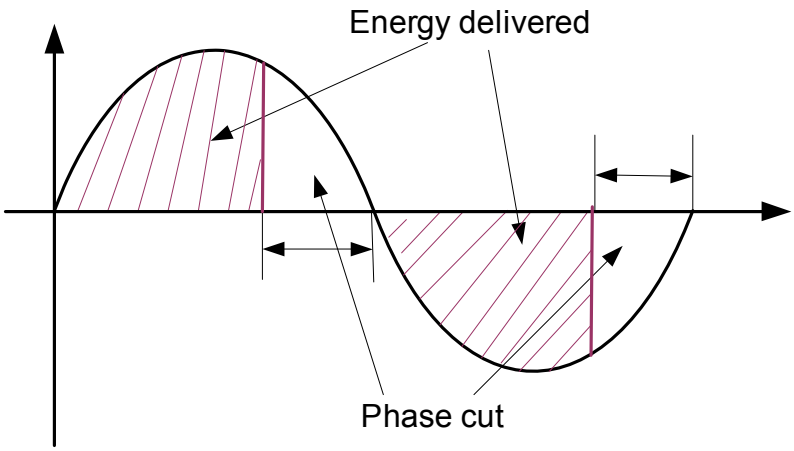


Figure 5—Trailing-Edge Phase-Cut Mode

In leading-edge phase cut mode，the dimmer is always TRIAC-based as shown in Figure 6. The TRIAC turns on after an RC delay, and the input voltage goes to the driver every half line-cycle. The high-input skipping voltage on the input capacitors causes a large input current: This current may cause the lamp to flicker and high power loss. For applications, the input capacitance—including the EMI filter capacitor and the input buffer capacitor—must be as small as possible. Use an additional damping circuit to avoid flicker from current oscillations.

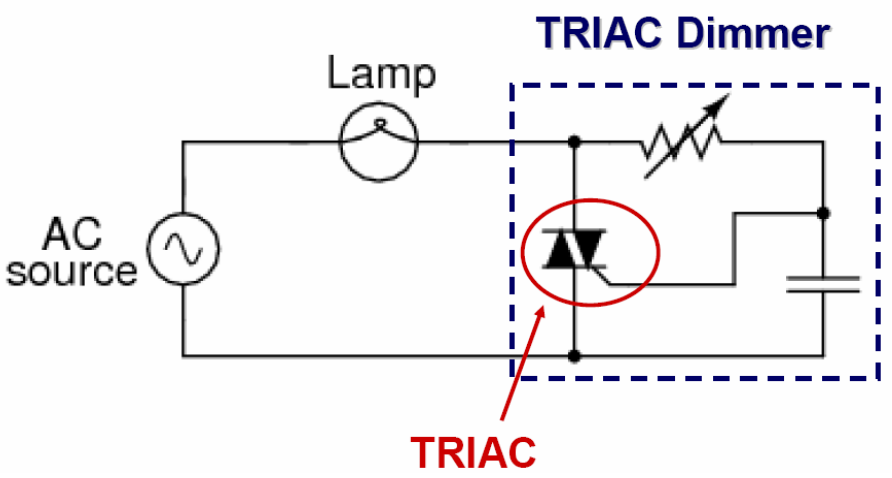
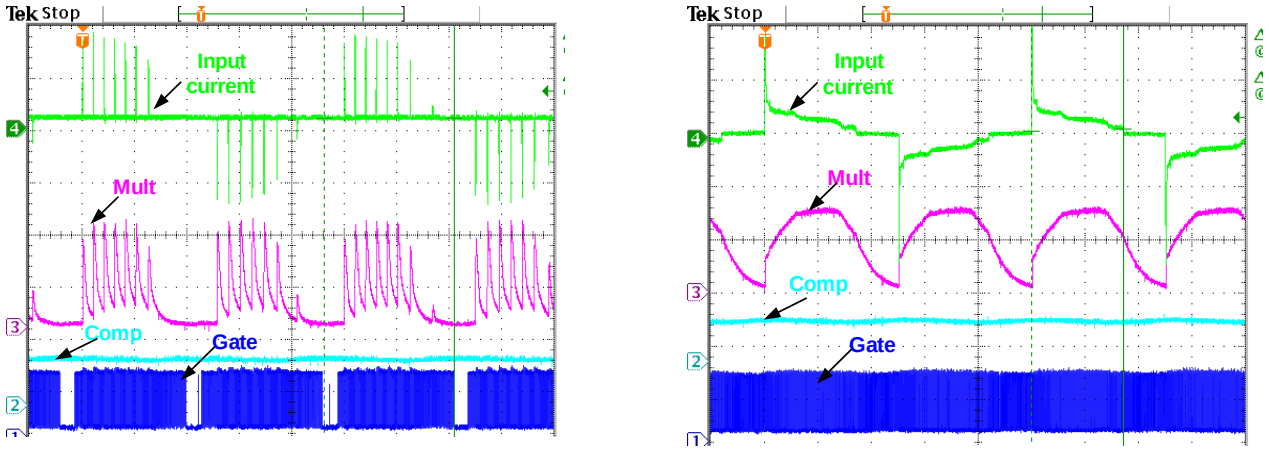


Figure 6—TRIAC Based Leading-Edge Dimmer

Figure 7(a) shows the input current without a damping circuit. In this situation, the inrush current when triac on rushes to zero and the triac is turned off abnormally. After a short time, the TRIAC turns on again. The driver input voltage (the same as MULT Pin voltage) also turns on and off repeatedly, which causes the LED to flicker.



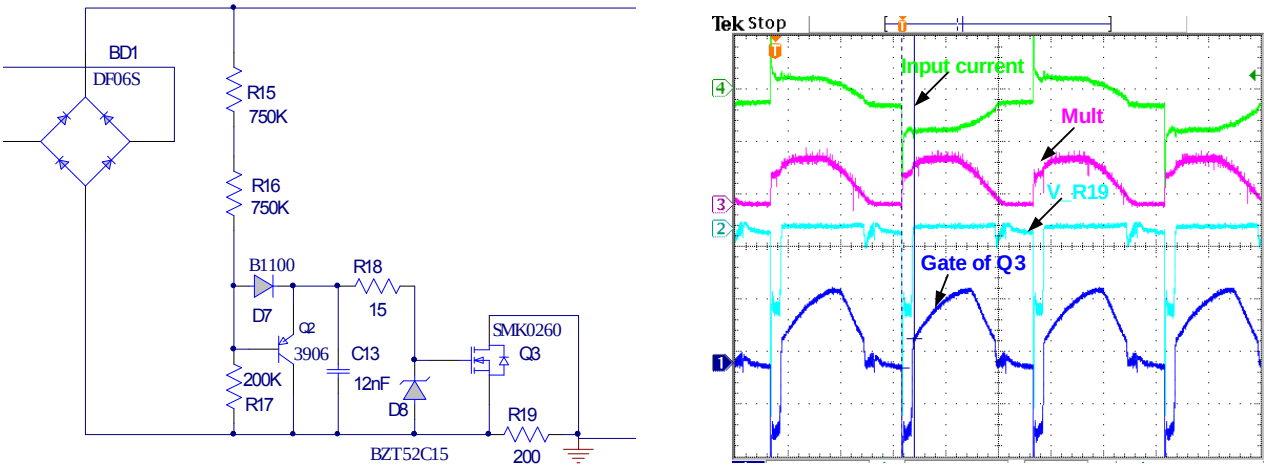
a. Input Current without Damping Circuit

b. Input Current with Damping Circuit

Figure 7—Input Current without and with Damping Circuit

Figure 8(a) shows the damping circuit. R19 is the damping resistor used to damp the input current when TRIAC turns on. Figure 7(b) shows the input current with damping circuit. The current is damped when the TRIAC turns on and the current will gradually reach zero to avoid flicker. But if R19 is always connected in the circuit, the energy consumed by R19 will be large and the efficiency will be low. Instead, an active damping circuit composed of R15 to R18, C13, D7, D8, Q2, Q3 in figure 8(a) selectively connects R19 to the rest of the circuit.

When TRIAC turns on, Q3 is off and R19 is in series to damp the input current. The base of Q2 is high so it's off, and C13 can be charged by input voltage through R15, R16 and D7. When the voltage on C13 is enough, Q3 is turned on and R19 is shorted, so it can save the energy and increase the efficiency. When TRIAC is off, the base of Q2 is low and Q2 is on, so C13 discharges through Q2, Q3 will then turn off for the next cycle. The waveforms are shown in figure 8(b), and the re. GND is the part's GND.



a. Active Damping Circuit

b. Active Damping circuit working waveform

Figure 8—Damping Circuit

The TRIAC-based leading-edge dimmer needs a holding current (usually 20 to 30mA) to maintain TRIAC on. the TRIAC will turn off unpredictably with a smaller holding current. If the holding current reduced too early, the flicker will be seen in the lamp. An extra bleeding circuit can resolve the flicker as a preload to increase the minimum holding current.

Figure 9 shows the bleeding circuit used to preload the TRIAC dimmer. The bleeding circuit is a capacitor in series with a resistor. It can block the line frequency power but provide a path for the resonant frequency current, so this can help keeping the line current above the holding current and avoid flicker caused by current resonance.

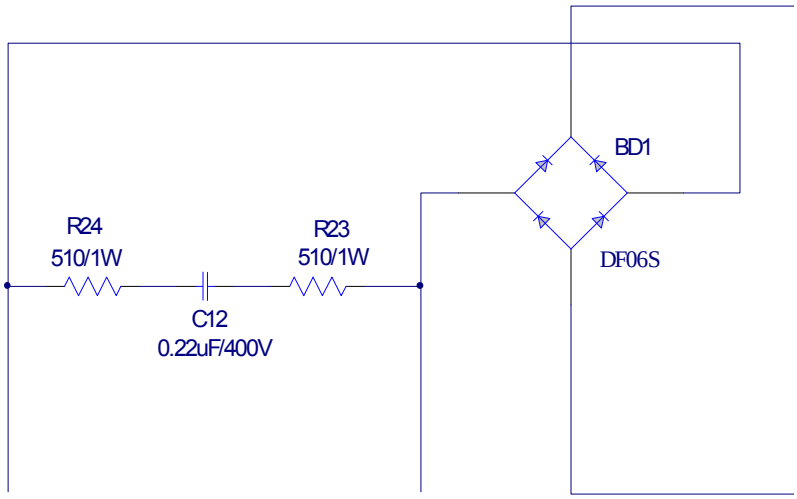


Figure 9—Damping Circuit

For a trailing-edge dimmer, the dimmer turns on when the input line voltage near zero, so there is no inrush current to the capacitor, and no flicker caused by the inrush current. The dimmer turns off after a manual adjusting time, and not turned off by current zero-crossing like the TRIAC dimmer. Therefore, a trailing-edge dimmer doesn't need either bleeding or damping circuits, but the line voltage will not decrease to zero immediately after dimmer turns off as the input voltage is cut off at a high point. In addition, if the input capacitance is too large, the dimmer output voltage may decrease more slowly

than the dimmer input voltage, the dimmer may turn on randomly and cause flicker. Therefore, chose small values for the EMI filter capacitor and buffer capacitor.

3. PIN FUNCTION AND OPERATION INFORMATION

3.1. Pin1 (MULT)

The MULT pin is one of the input pins of the internal multiplier, and it is used for PFC function and dimming phase detection in MP4020. The MULT pin connects to the tap of the resistor divider from the rectified instantaneous line voltage, so that the output of the multiplier will have the same shape as the rectified voltage. This voltage provides the reference for the current comparator which sets the primary peak current.

For non-dimmer applications of the MP4020, the primary peak current is shaped as a sinusoid in phase with the input line voltage cycle by cycle and it can realize the PFC function. Otherwise, the MULT pin is used to detect the dimming phase. When mult voltage is higher than 0.35V, it means dimming on and the part will work in the dimming on state. When mult voltage is lower than 0.1V, it means dimming off. The internal reference will linearly change with the dimming duty and dim the output current accordingly.

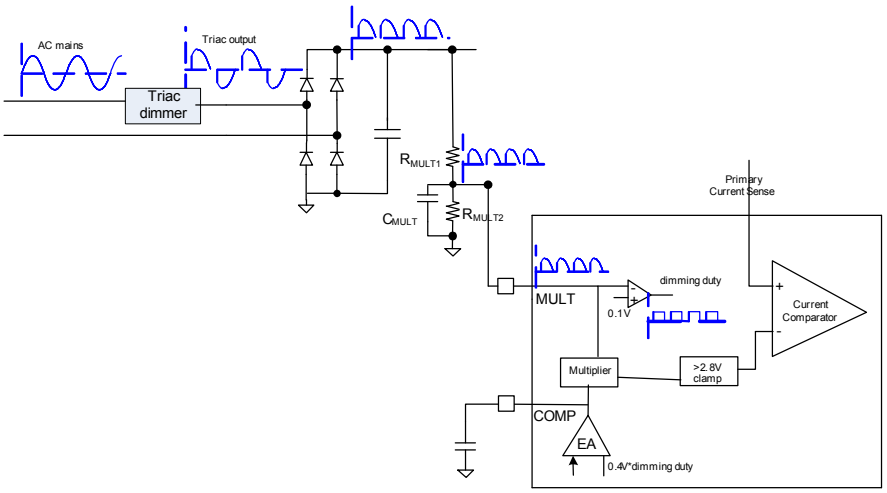


Figure 10—MULT Pin Connection Circuitry

The MULT pin linear operation voltage range is 0 to 3V. If the MULT voltage is much higher than 3V, the power factor (PF) will be lower and the total harmonic distortion (THD) will be higher. However, the MULT pin voltage can not be set too low or this will cause a high COMP voltage to regulate the same LED current: the COMP voltage may saturate when the MULT pin is set too low. In addition, if the MULT voltage, at low input voltage the MULT pin may not be able to detect the dimming on signal (0.35V). Set the MULT voltage using the model shown below:

$$\sqrt{2} \times V_{IN\_MIN(rms)} \times \frac{R_{Mult2}}{R_{Mult1} + R_{Mult2}} > 0.5 \sim 1$$

$$\sqrt{2} \times V_{IN\_MAX(rms)} \times \frac{R_{Mult2}}{R_{Mult1} + R_{Mult2}} < 2.5 \sim 3$$

Considering the power loss, the R_{MULT1} should be large enough, usually 1M for high-input voltage use.

3.2. Pin2 (ZCD)

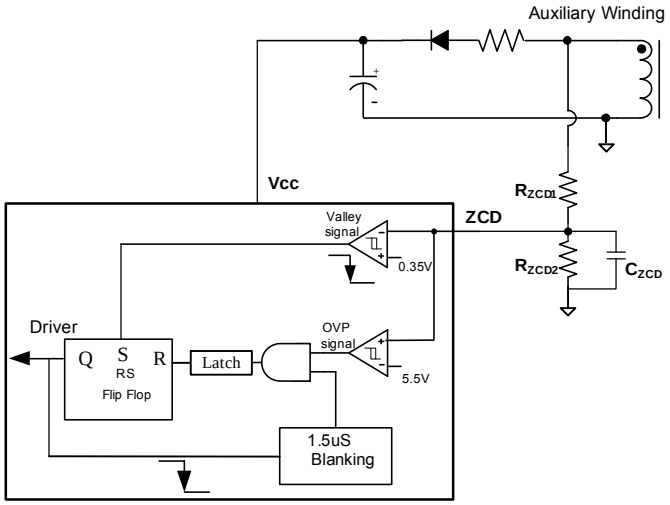


Figure 11—ZCD Pin Connection Circuitry

The ZCD pin connection circuitry is shown in Figure 11. It connects to the auxiliary winding through a resistor divider. The ZCD pin is used for two functions: one is to detect the valley voltage of the MOSFET, which occurs when the secondary side current decreases to ensure the boundary conduction mode operation; the other is to implement the output over-voltage protection (OVP) when compared to the internal 5.5V reference.

Figure 12 shows the ZCD voltage. The internal valley signal triggers when the falling edge of the ZCD pin voltage drops below 0.35V. A ceramic bypass capacitor absorbs the high frequency oscillation caused by the leakage inductance and the parasitic capacitance after the primary switch turns off. Without the bypass capacitor, this oscillation may cause the false-positives in ZCD valley detection.

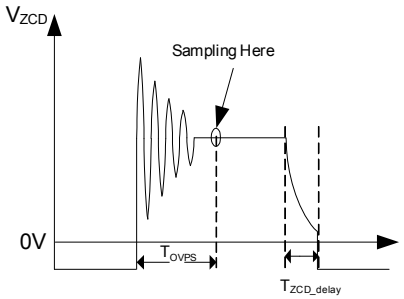


Figure 12—The ZCD Voltage

The switching frequency of MP4020 changes with the input instantaneous line voltage. To limit the maximum frequency and attain good EMI and efficiency performance, MP4020 employs an internal minimum off time limiter—3.5μs, shown in Figure 13. The ZCD signal is external in Figure 13, after gate off, there will be a min off time even the part has detect the gate on signal from ZCD pin.

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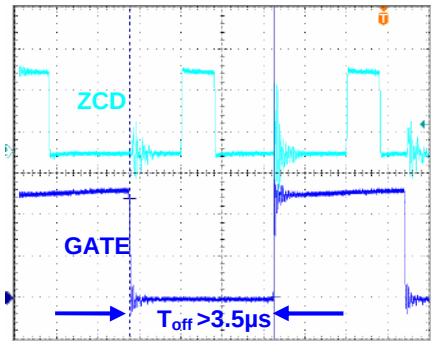


Figure 13—Minimum Off Time

The output over voltage protection is achieved by detecting the positive plateau of auxiliary winding voltage which is proportion to the output voltage (see Figure 12). Once the ZCD pin voltage is higher than 5.5V after a blanking time, the OVP signal will be triggered, the gate driver will be turned off and the VCC voltage dropped below the UVLO which will make the IC reset and the system restarts again. The part will work in hiccup mode. The output OVP setting point can be calculated as:

$$V_{out-ovp} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 5.5V$$

Where:

V_{OUT_OVP}—Output over voltage protection point

N_{AUX}—The auxiliary winding turns

N_{SEC}—The secondary winding turns

To avoid the OVP mistriggering caused by ringing after the switch turns off, the MP4020 integrates an internal T_{OVPS} blanking time of 1.5μs for the OVP detection (see Figure 12).

3.3. Pin3 (VCC)

The VCC pin provides the power supply to both the internal logic circuitry and the gate driver signal. Figure 14 shows the VCC pin connection circuit and the power supply flow-chart. The bulk capacitor C_{VCC1} (typically 22μF) initially charges from the AC line through R_{VCC1} when AC power initially turns on. Once the VCC voltage reaches UVLO_H (12V), the IC will turn on and begin switching. The power consumption of the IC increases, then the auxiliary winding starts working and mainly takes in charge of the power supply for VCC. Since the auxiliary winding voltage is proportional to the secondary winding voltage, the VCC voltage stabilizes to a constant value. If VCC drops below the UVLO_L threshold (7.6V) before the auxiliary winding can provide power, the IC will shut down and VCC will begin to charge from the Bus voltage again.

If OVP or other hiccup signal happens at normal operation, the switching signal will stop and the IC works in quiescent mode. When the VCC voltage drops below 7.6V the system restarts.R_{VCC1} must be large enough to limit the charging current which ensures the VCC voltage can drop below 7.6V (typically 1mA consumption current in quiescent mode). However, an extremely large R_{VCC1} will delay start-up. Also, a small ceramic capacitor C_{VCC2} (typically 100pF) is needed to reduce the noise.

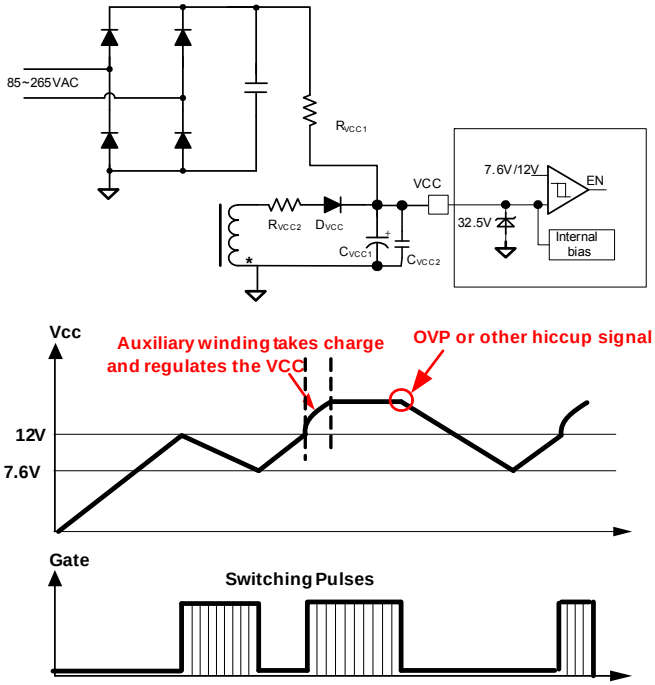


Figure 14—VCC Pin Connection Circuitry and the Power Supply Flow-Chart

3.4. Pin4 (GATE)

Pin 4 is the gate driver output to drive an external MOSFET. The internal totem-pole output stage can drive an external high-power MOSFET with 1A source and 1.2A sink capability. The pin voltage is clamped to 13V to avoid excessive gate driver voltage. Connect this pin to the MOSFET gate in series with a driving resistor. A smaller driving resistor provides faster MOSFET switching, reduces switching loss, and improves MOSFET thermal performance. However, larger driving resistors usually provide better EMI performance. For this reason, the driving resistors should be tuned for different applications. Typically, the value of the driving resistor ranges from 5Ω to 20Ω.

3.5. Pin5 (CS)

The CS pin senses the primary side current using a sensing resistor. The resulting voltage is fed to both the current comparator to determine the MOSFET turn off time and the average current calculation block to calculate the primary current average value. The output LED mean current can be calculated approximately as:

$$I_O \approx \frac{N \times V_{FB}}{2 \times R_S}$$

Where:

N is the turn ratio between the primary winding and the secondary winding

V_{FB} is the feedback reference voltage (typically 0.4)

R_s is the sensing resistor connected between the MOSFET source and GND.

The maximum voltage on CS pin is clamped at 2.8V to get a cycle-by-cycle current limit.

In order to avoid premature termination of the switching pulse due to parasitic capacitance discharge when the MOSFET turns on, the MP4020 uses an internal leading-edge blanking (LEB) unit between the CS Pin and internal feedback. During the blanking time, the internal fed path is blocked. Figure 15 shows the LEB

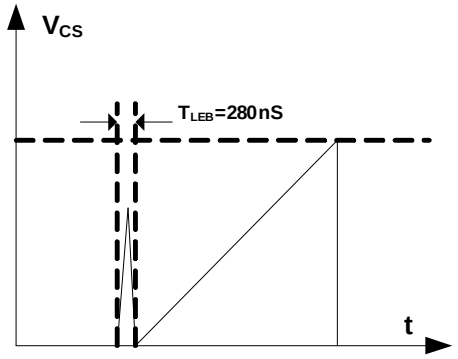


Figure 15—Leading-Edge Blanking

3.6. Pin6 (GND)

The ground pin is the current return for the control signal and the gate driver signal. Connect this pin to both power and analog GND on the PCB layout. Otherwise, keep power and analog GNDs on separate planes on the PCB.

3.7. Pin7 (FB/NC)

Pin 7 is the feedback signal pin. As shown in Figure 16, the FB signal connects to the negative input of the error amplifier (EA) and compared against the 0.4V reference when dimming on, so at steady state, the average value of FB will be regulated to $0.4V*D_{dimming}$. The average current calculation block output is internally connected to the FB with high input impedance. If there is no other external feedback signal is applied on FB pin, the average current from CS pin will be regulated, if there is external FB signal with low input impedance apply in this pin, the external FB signal will be regulated. This structure makes the MP4020 suitable for both primary side control application without other feedback signals and direct control application with an applied external feedback signal.

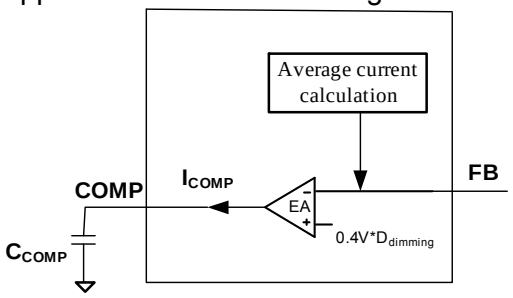


Figure 16—FB Pin Structure

3.8. Pin8 (COMP)

Pin 8 is the loop compensation pin. Connect a low-ESR ceramic compensation capacitor—such as an X7R capacitor—from this pin to AGND. The COMP pin is the internal current-source error amplifier output with maximum 75uA source current and 200uA sink current. Select a capacitor value between 2.2uF and 10uF in order to get a limit loop bandwidth of <20Hz. A small cap will result in low PF, because the comp voltage will change to compensate the mult voltage, and the multiplier output voltage could not follow the line voltage and the PF is low. A large capacitor results in small input and output current ripple and better thermal, EMI, and steady-state performance. However, a large capacitor also results in a longer soft-start time which will cause a bigger voltage drop for VCC at start up (see figure 17)—if VCC drops below UVLO, start-up may fail..

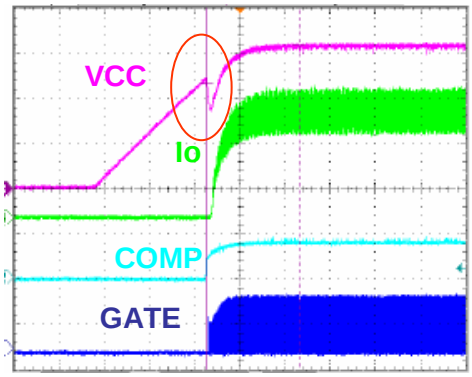


Figure 17—COMP and VCC Waveform at Start Up

3.9. Auto Restart

The MP4020 integrates an auto starter that begins when the MOSFET turns on. If ZCD fails to send out another turn-on signal after 130us, the starter will automatically send a turn-on signal that can avoid unnecessary IC shutdown by ZCD missing detection.

3.10. Output Short-Circuit Protection

In the event of an output short circuit, the positive plateau of the auxiliary winding voltage is also near zero. so the gate signal is 130us auto starter, the VCC can not be held on and it will drop below VCC UVLO. The IC will run at hiccup mode.

4. DESIGN EXAMPLE

Example 1: 8W, 120V, TRIAC-Dimmable LED Bulb Driver

A. Specifications

Parameter	Symbol	Value	Unit
Input voltage	Vac	95 to 135	V
Output voltage	Vo	16	V
Output current	Io_max	500	mA

B. Schematic

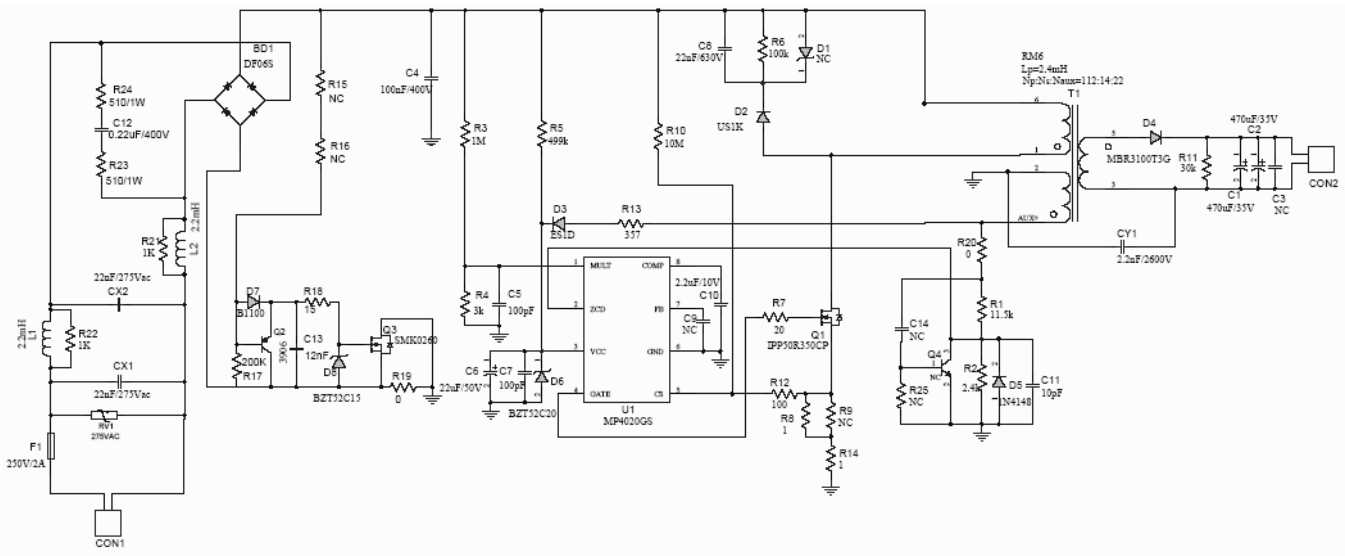


Figure 18—Schematic of Example 1

C. Transformer Design Spreadsheet (THE SOFTWARE IS MPS DESIGN TOOL FOR MP4020 TRANSFORMER DESIGN)

C.1. Input and Output Spec

The underlined red data is user input. This tool can calculate the cyan data.

1. System Spec			
Input Spec			
minimum line voltage	Vin_ac_min	95	V
maximum line voltage	Vin_ac_max	135	V
line frequency	f	50	Hz
maxmum DC voltage	Vin_dc_max	191	V

Output Spec			
output voltage	Vo	16.00	V
output current	Io	0.500	A
output power	Po	8.00	W
estimate efficiency	η	85.0	%
input power	Pin	9.412	W

C.2. Transformer Turn Ratio

The primary voltage spike occurs at the MOSFET Q1. It usually results from energy dissipation from the leakage inductance of the transformer and the RCD snubber circuit as shown in Figure 19.

R6 and C8 can regulate the primary voltage spike. Larger values of C8 and smaller values of R6 result in a smaller spike, but very small spikes result in low efficiency. For optimal results, select voltage spike amplitudes between 100 and 150V.

Reflected output voltage is the voltage reflecting from the secondary side of the transformer to the primary side when the MOSFET is off. It determines the Q1 MOSFET voltage rating, the D2 diode voltage rating, and the transformer turn ratio. A larger reflected output voltage means a higher Q1 voltage rating, and a smaller reflected output voltage means a higher D2 voltage rating. Selected a reflect output between 100 and 150V.

2. Transformer Turns Ratio			
primary voltage spike	Vspike	150	V
secondary output recitify diode forward voltage	Vf	0.7	V
reflected output voltage	Vreflect	130	V
Transformer Turns Ratio (Np:Ns1)	N	8	
maximum DS voltage of primary MOSFET	Vds_max	471	V
maximum reverse voltage of output diode	V_diode_max	41	V

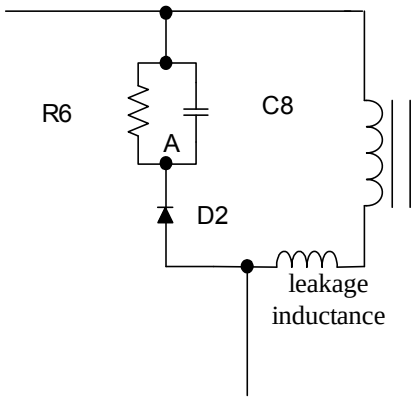


Figure 19—RCD Snubber Circuit on Primary Side

C.3. The Frequency and Primary Inductance of the Transformer

The min frequency of the transformer occurs at the peak of the min input voltage, and determines the primary side inductance and the max frequency.

In the universal input case, select the min frequency somewhere between 40kHz and 45kHz. In narrow input case, select the min frequency between 60kHz and 80kHz. Lower frequency can decrease the switching loss and improve EMI performance, but increase the size of the transformer.

3. Transformer			
switching frequency @minimum Vin, full load	fs_min	60	kHz
primary inductance	Lp	2.425	mH
primary peak current @minimum Vin, full load	Ip_max	0.46	A

C.4. Transformer Core and Turns

Users need to determine which core to use and then input the Ae and Aw. This tool will calculate the turns and diameter of each winding using the user's core information. This tool will also check the fill factor: if the fill factor is larger than 0.3, users need to select a larger core; if the fill factor is much lower than 0.3, users need to select a smaller core. After filling in the parameters, users can press the OK! Please generate a check list. button and the tool will print the specs of the transformer as shown in Figure 20.

1. Determine the Transformer Core and Turns			
the maximum flux density Bmax	0.27	T	Typically, 0.2T-0.3T !
current density Jmax	600	A/cm^2	Typically, 400-600A/cm^2 !
requiered AP value	274.55	mm^4	

2. Design by Yourself?

(•) Yes, I can manage it! ( ) No, no need to waste time.

3. Manual Design

transformer core area Ae	36.6	mm^2
winding area Aw	26	mm^2
transformer core AP	951.6	mm^4

primary winding	112	Turns
output winding	14	Turns
auxiliary winding	22	Turns

4. Determine the diameter of the coil

skin depth 0.31 mm

	select coil	diameter		area		parallel windings
primary winding	33#	0.18	mm	0.03	mm^2	1
output winding	28#	0.32	mm	0.08	mm^2	2
auxiliary winding	34#	0.16	mm	0.02	mm^3	1
fill factor	0.22					

OK! Please generate a check list.

If the user does not know which core to select, there is an auto-select core method. Users just need to select the core shape, and the tool will auto-select a suitable core for the spec and calculate the winding turns. Then users need to determine the diameter of the windings. Then the tool can check the fill factor and generate the transformer specs as the first method shows.

For example, we use the same core shape in two different methods, the result are the same, just as Figure 20 shows.

1. Determine the Transformer Core and Turns

the maximum flux density Bmax	0.27	T	Typically, 0.2T-0.3T !
current density Jmax	600	A/cm^2	Typically, 400-600A/cm^2 !
requiered AP value	274.55	mm^4	

2. Design by Yourself?

○ Yes, I can manage it!

◉ No, no need to waste time.

3. Automatic Design

select the core shape: RM

GO!

the selected core	RM6	
effective area Ae	36.6	mm^2
effective length Le	28.6	mm
winding area Aw	26	mm^2
AP of the selected core	951.6	mm^4

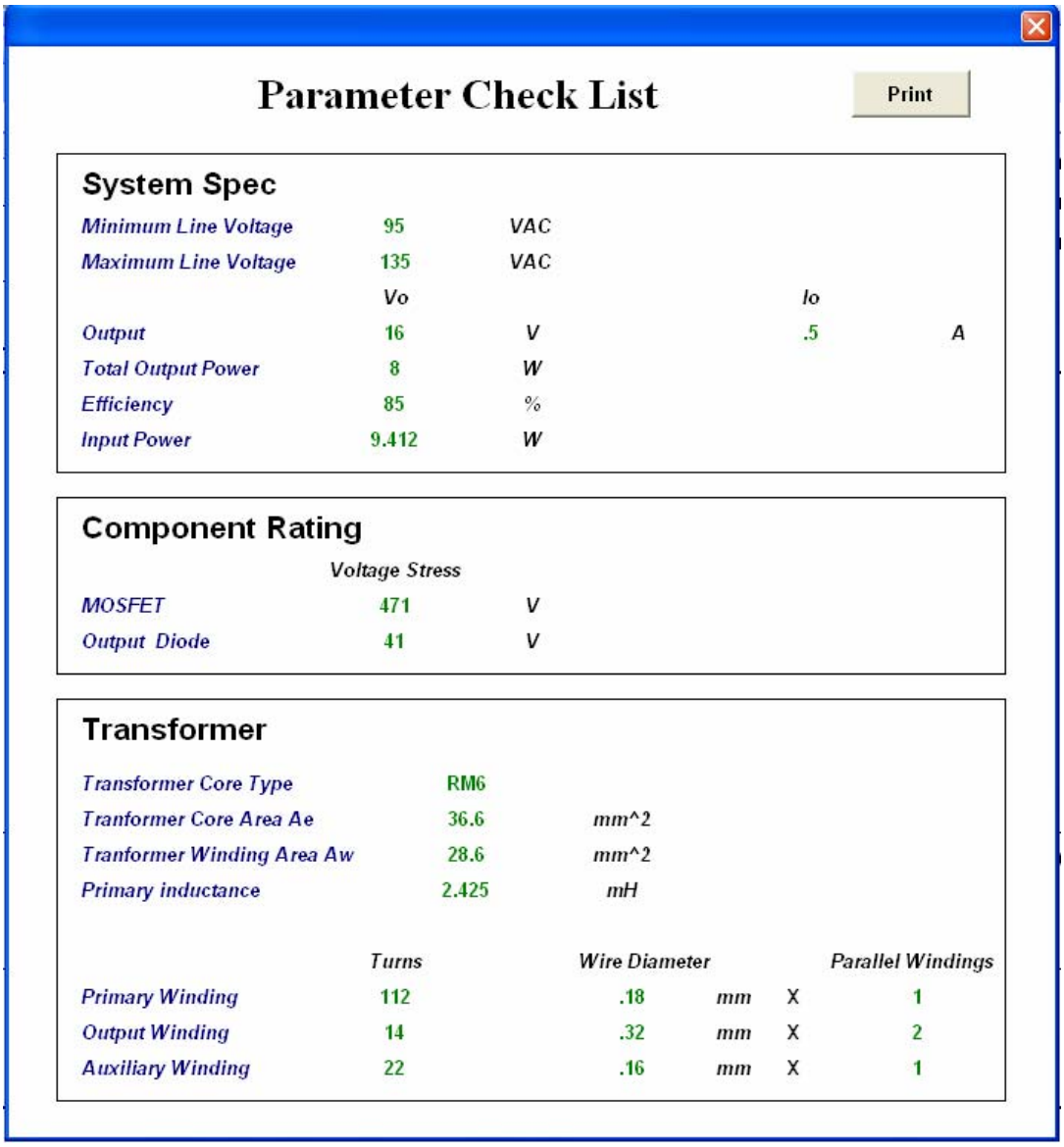
primary winding	112	Turns
output winding	14	Turns
auxiliary winding	22	Turns

4. Determine the diameter of the coil

skin depth: 0.31 mm

	select coil	diameter		area		parallel windings
primary winding	33#	0.18	mm	0.03	mm^2	1
output winding	28#	0.32	mm	0.08	mm^2	2
auxiliary winding	34#	0.16	mm	0.02	mm^3	1
fill factor	0.22					

OK! Please generate a check list.



Parameter Check List

Print

System Spec

Minimum Line Voltage	95	VAC		
Maximum Line Voltage	135	VAC		
	Vo		Io	
Output	16	V	.5	A
Total Output Power	8	W		
Efficiency	85	%		
Input Power	9.412	W		

Component Rating

	Voltage Stress	
MOSFET	471	V
Output Diode	41	V

Transformer

Transformer Core Type	RM6	
Tranformer Core Area Ae	36.6	mm^2
Tranformer Winding Area Aw	28.6	mm^2
Primary inductance	2.425	mH

	Turns	Wire Diameter			Parallel Windings
Primary Winding	112	.18	mm	X	1
Output Winding	14	.32	mm	X	2
Auxiliary Winding	22	.16	mm	X	1

Figure 20—Paper Design Result of the Transformer

D. Transformer Manufacture Instructions

There are two main considerations for the transformer design. To minimize the effect of the leakage inductance spike, the coupling between the transformer primary side and the secondary side should be as tight as possible. This can be accomplished be interleaving the primary and secondary winding in transformer manufacture (shown in figure 21). To minimize the coupling capacitance between the primary winding and the secondary winding, the auxiliary winding can be sandwiched between them as shown in Figure 21. The Drain pin should be the starting dot of the primary side winding. And on the PCB layout, the GND of the auxiliary winding must be placed between the primary side and the auxiliary side as shown in Figure 22.

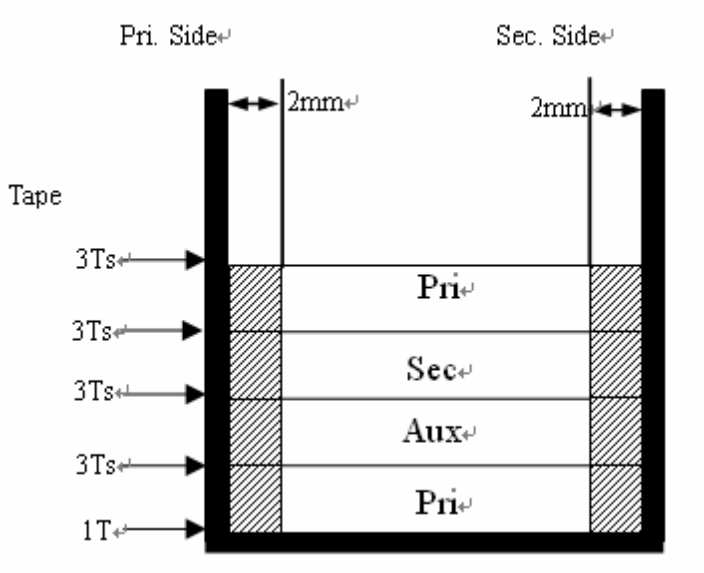


Figure 21—The Transformer Winding Diagram

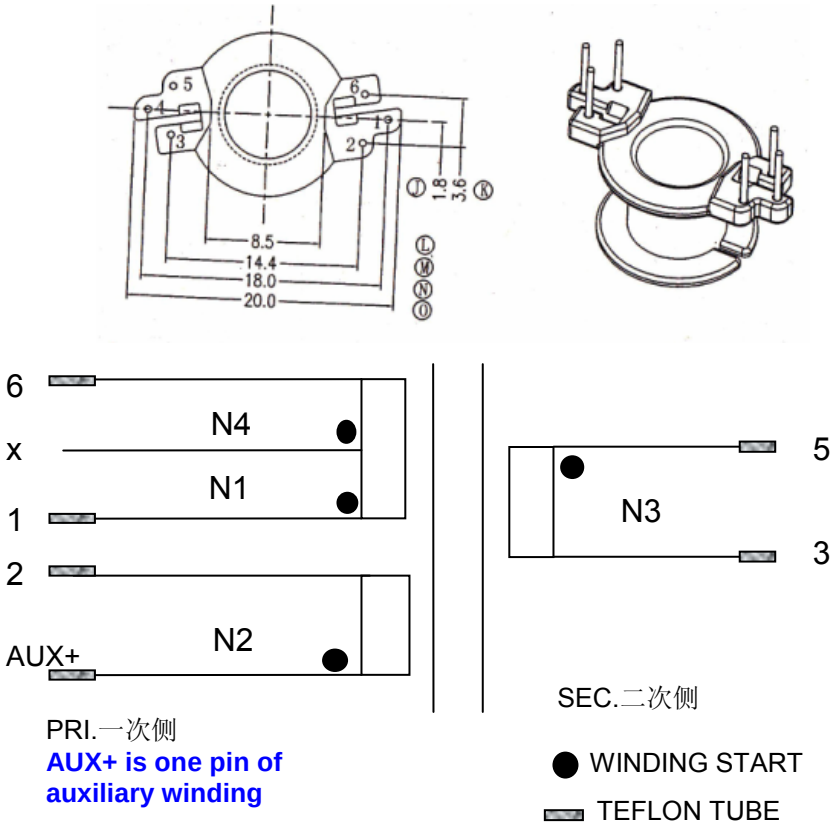


Figure 22—Transformer Pin-Out and the Connection Diagram

E. Input EMI Filter (L1, L2, CX1, CX2, CY1)

The input EMI filter is comprised of L1, L2, CX1, CX2, and the safety rated Y class capacitor CY1. The value of the components should be selected to pass the EMI test standard EN55015 for lighting production.

Usually, the interference below 1MHz is caused by differential mode (DM). Noise interefence from 1MHz to 5MHz is caused by both common mode (CM) and DM. CM causes interference above 5MHz. The interference is low enough (tested without common choke, as the results show), to only require DM capacitors (CX1 = CX2 = 22nF) and inductors (L1 = L2 = 2.2mH) in this case.

Increasing the DM capacitor and inductor can improve the EMI result below 1MHz. But in the TRIAC dimming condition, a large capacitor may cause flicker, so chose a small capacitor.

If the event of poor results between 1MHz and 5MHz ,add common choke to the filter: this choke can also improve results above 5MHz. The Y class capacitor can improve results from 20MHz to 30MHz.

F. Input Bridge (BD1)

The input bridge can use standard slow recovery, low-cost diodes. Diode selection involves consideration of 3 criteria: the maximum input RMS current, the maximum input line voltage, and the thermal performance.

G. Input Capacitor (C4)

Chose a relatively small value for the input decoupling capacitor to get a high power factor. The function of the capacitor is mainly to attenuate the switching current ripple of the transformer at high magnetizing frequencies. The worst case occurs at the peak of the minimum rated input voltage. The maximum high frequency voltage ripple of the capacitor should be limited to 20%, or the large voltage ripple will influence the sensing accuracy of the MULT pin which will also influence the PFC function.

In real applications, the input capacitor must be as small as possible, and designed to account for the EMI filter, the power factor value, and TRIAC dimming performance

H. Damping and Bleeding Circuit

The principle of the Damping and Bleeding circuit is described in “2.3 TRIAC dimming”.

R15, R16, R17, R18, C13, D7, D8, Q2, Q3 are used with R19 to consist an active damping circuit. In this case, as the resonance is not so strong, so R19=0, and the damping circuit can be removed from the circuit. As a reference, we put the parameters in the circuit. Larger R19 (usually from 200 Ω to 500Ω， too large will cause low efficiency) will result in strong damping, increasing the RC time of (R15+R16)*C13 can also increase the function of the damping circuit. And other components can usually use the commend parameters as the SCH shows.

R23, R24 and C12 consist of the bleeding circuit. It can block the line frequency power but provide a path for resonant frequency current, so this can help keeping the line current above the holding current and avoiding flicker caused by resonant current. Larger C12 results in strong bleeding, and C12 is usually selected from 100nF to 220nF.

R19, R23, R24 and C12 need to be regulated in the real circuit.

I. ZCD and OVP Detector (R1, R2, C11, D5)

Please refer to page 12 and 13 for detailed design information.

The resistor divider by R1 and R2 sets the OVP threshold:

$$V_{o\_ovp} \cdot \frac{N_{aux}}{N_s} \cdot \frac{R_2}{R_1 + R_2} = 5.5V \quad (32)$$

Where V_{o_ovp} is the output OVP setting voltage; N_{aux} is the auxiliary winding turns of the transformer and N_s is secondary winding turns of the transformer. In this case, V_{o_ovp} is about 20V, N_{aux} = 22, N_s = 14, so we can select R2 = 2.4k, R1 = 11.5k. A 10pF ceramic bypass capacitor (C11) is added on ZCD pin absorbs the high frequency oscillation on ZCD voltage when the MOSFET turns off. In addition, a diode (D5) connected from ZCD pin to GND clamps the ZCD negative voltage, which can help improve the noise influence on the ZCD pin.

J. MULT PIN Resistor Divider (R7, R3, R4, C5)

For the MULT pin resistor divider setting information, please refer to design information on page 11. In this example, we have chosen R3 = 1MΩ, R4 = 3kΩ, and C5 = 100pF.

K. Current Sensing Resistor (R8, R9, R14)

The current sensing resistor can be approximately set by the following equation:

$$R_s \approx \frac{V_{FB} \cdot N}{2 \cdot I_o} \quad (33)$$

Where N is the turn ratio of primary winding to secondary winding, V_{FB} is the feedback reference voltage (typically 0.4V), R_s is the sensing resistor connected between the MOSFET source and GND.

But in real applications with primary-side control, modeling accuracy for the output current is much more difficult because there are many factors influencing the output current setting value—such as the internal logic delay of the IC, the transformer inductance, the MOSFET input and output capacitor, the ZCD detection delay time, the RCD snubber, the gate driver resistor, among them. With this in mind, determine the current sensing resistor last after fine-tuning the resistance with a bench test.

L. Layout Guideline

- The path of the main power flow should be as short as possible, and the trace should be as wide as possible, the cooper pour for the power devices should be as large as possible to get a good thermal performance.
- Separate the power and the analog GNDs, except at a single via to the GND of C4.
- In order to minimize the coupling interference between the primary winding and the auxiliary winding, the same mean dot of the two windings should be far away. It is better to be separated by the GND.
- Make a loop from C4, through the primary winding of T1, through Q1, .R8, R9, and R14 as small and short as possible. Do not run the loop under the IC.
- The IC pin components should be placed as close as possible to the corresponding pin, especially the ZCD bypass capacitor and the COMP pin capacitor.
- The primary side and the secondary side should be well isolated, and the trace from the transformer output return pin to the return point of the output filter capacitor should be as short as possible.

M. BOM

Qty	Designator	Value	Description	Package	Manufacturer	Manufacture_PN
1	BD1	DF06S	DIODE/BRIDGE /DF06S/B	SMD	Qianlongxin	DF06S
2	C1, C2	470uF/35V	Electrolytic Capacitor;35V	DIP	Rubycon	470uF/35V
1	C3	NC				
1	C4	100nF/400V	CBB,400V	DIP	Panasonic	CBB 0.1uF/400V
2	C5, C7	100pF	Ceramic Cap,50V,NPO	0603	LION	0603B10K500T
1	C6	22uF/50V	Electrolytic Capacitor;50V	DIP	Jianghai	CD281L-50V22
1	C8	22nF/630V	Ceramic Cap, 630V，X7R	1210	muRata	GRM32QR72J223KW01
1	C9	NC				
1	C10	2.2uF/10V	Ceramic Capacitor;10V;X7R;0805	0805	LION	C1608X7R1H102K
1	C11	10pF	Ceramic Cap,50V,X7R	0603	LION	0603N100J500T
1	C12	220nF/400V	CBB,400V	DIP	Panasonic	ECQE4224KF
1	C13	12nF	Ceramic Cap,50V,X7R	0603	muRata	GRM188R71H123KA01D
1	C14	NC				
2	CX1,CX2	22nF	Film Capacitor, X2,275V	DIP	carli	
1	CY	2.2nF	Y Capacitor,2600V	DIP	Hongke	JN09F222ML72N
1	D1	NC				
1	D2	US1K-E3	Diode, 1A,800V	SMA	Vishay	US1K-E3/61T
1	D3	ES1D	Diode, 1A,200V	SMA	Premier	ES1D
1	D4	MBRS3100T3G	Diode,3A,100V	SMC	ON Semiconductor	MBRS3100T3G
1	D5	1N4148W	DIODES/SOD-123	SOD-123	Diodes	1N4148W
1	D6	BZT52C20	DIODES/SOD-123	SOD-123	Diodes	BZT52C20
1	D7	B1100	schottky diode	SMA	Diodes	B1100-13-F
1	D8	BZT52C15	DIODES/SOD-123	SOD-123	Diodes	BZT52C15
1	F1	250V/2A	SS-5-2A	DIP	COOPER BUSSMAN	SS-5-2A
2	L1,L2	Inductor,2.2mH	Inductor,2.2mH	DIP		
1	Q1	IPP50R350CP	MOSFET, 550V	TO-220		IPP50R350CP
1	Q2	MMBT3906LT1	PNP,transistor	SOT-23	ON Semiconductor	MMBT3906LT1

Qty	Designator	Value	Description	Package	Manufacturer	Manufacture_PN
1	Q3	SMK0260D	MOSFET, 600V	TO-252	AUK	SMK0260D
1	Q4	MMBT3904LT1	NPN, transistor	SOT-23	ON Semiconductor	MMBT3904LT1
1	R1	11.5k	Film RES, 1%	0603	Yageo	RC0603FR-0711K5L
1	R2	2.4k	Film RES, 1%	0603	LIZ	CR0603JA0242G
1	R3	1M	Film RES, 1%	1206	Panasonic	RC1206FR-071ML
1	R4	3k	Film RES, 1%	0603	Yageo	RC0603FR-073KL
1	R5	499k	Film RES, 1%	1206	Panasonic	ERJ8EF4993V
1	R6	100K	Film RES, 5%	1206	Yageo	RM12JTN104
1	R7	20	Film RES, 1%	0603	Yageo	RC0603FR-07560KL
2	R8,R14	1	Film RES,1%	1206	Royalohm	1206F100KT5E
1	R9	NC				
1	R10	10M	Film RES,1%	1206	Royalohm	12061005T5E
1	R11	30k	Film RES,1%	1206	Royalohm	12063002T6E
1	R12	100	Film RES,1%	0603	Yageo	RC0603FR-07100RL
1	R13	357	Film RES,1%	1206	Yageo	RC1206FR-07357RL
2	R15,R16	750k	Film RES,1%	0603	Yageo	RC0603FR-07750KL
1	R17	200k	Film RES,1%	0603	Yageo	RC0603FR-07200KL
1	R18	15	Film RES,1%	0603	Yageo	RC0603FR-0715RL
1	R19	200	DIP, 2W	DIP		
1	R20	0	Film RES, 1%	0603	Royalohm	RR0603L0R0JT
2	R21,R22	1K	Film RES,1%	1206	Royalohm	1206F1001T5E
2	R23,R24	510	DIP,1W RESISTOR	DIP		
1	R25	NC				
2	JR1	0	Film RES, 1%	0805		0805S8J0000T5E
1	RV1	NC				
1	T1	RM6	Np:Ns:Naux=11 2:14:22 Lp=2.4mH	RM6		
1	U1	MP4020GS	MP4020GS	SOIC8	MPS	

5. EXPERIMENTAL RESULT

All measurements performed at room temperature

5.1. Efficiency vs. Line Voltage

Vin(V)	Pin(W)	Vo(V)	Io(mA)	Efficiency
95	7.13	15.26	379	81.12%
100	7.67	15.3	410	81.79%
110	8.84	15.44	469	81.92%
120	8.96	15.44	478	82.37%
135	9.21	15.47	493	82.81%

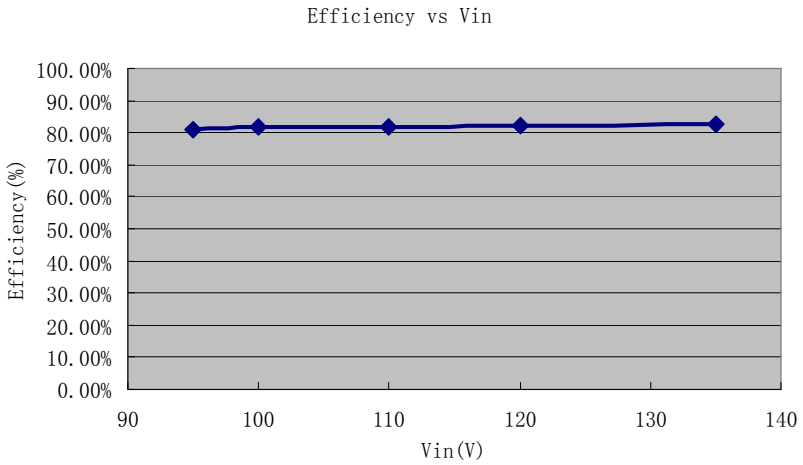


Figure 23— Efficiency vs. Input Line Voltage

5.2. Output LED Current Dimming Curve

Dimming on Phase(°)	180	134	114	94	73	63	50	35	27
I_O (mA)	478	444	386	318	245	190	132	67	43

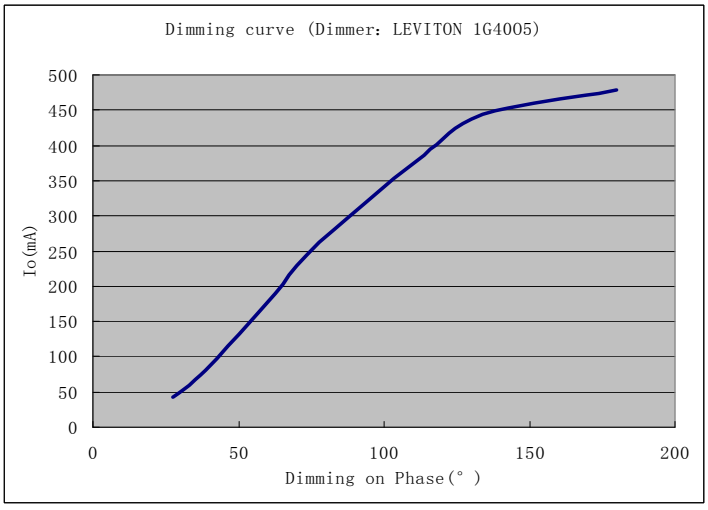


Figure 24— Output Current Accuracy vs. Input Line Voltage

5.3. PF, THD vs. Line Voltage

Vin(V)	PF	THD	3rd harmonics	IEC61000-3-2
95	98.80%	9.10%	8.40%	29.64%
100	98.70%	9.30%	8.60%	29.61%
110	98.50%	9.50%	9.00%	29.55%
120	98.00%	9.60%	9.20%	29.40%
135	97.20%	9.80%	9.40%	29.16%

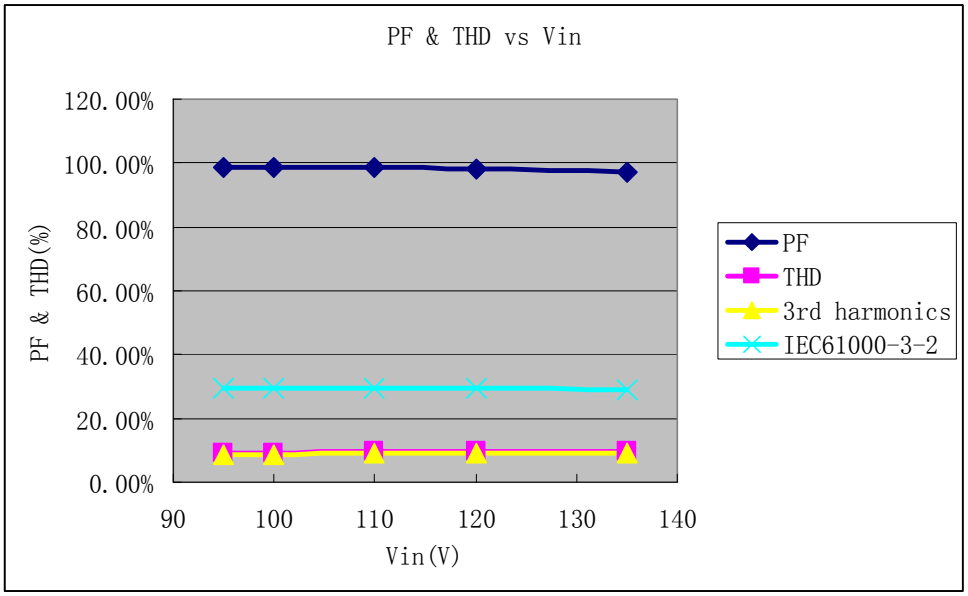


Figure 25—Output Current Accuracy vs. Input Line Voltage

5.4. Conducted EMI (V_{IN}=120V)

EMI test condition: Figure 26 shows the test conditon

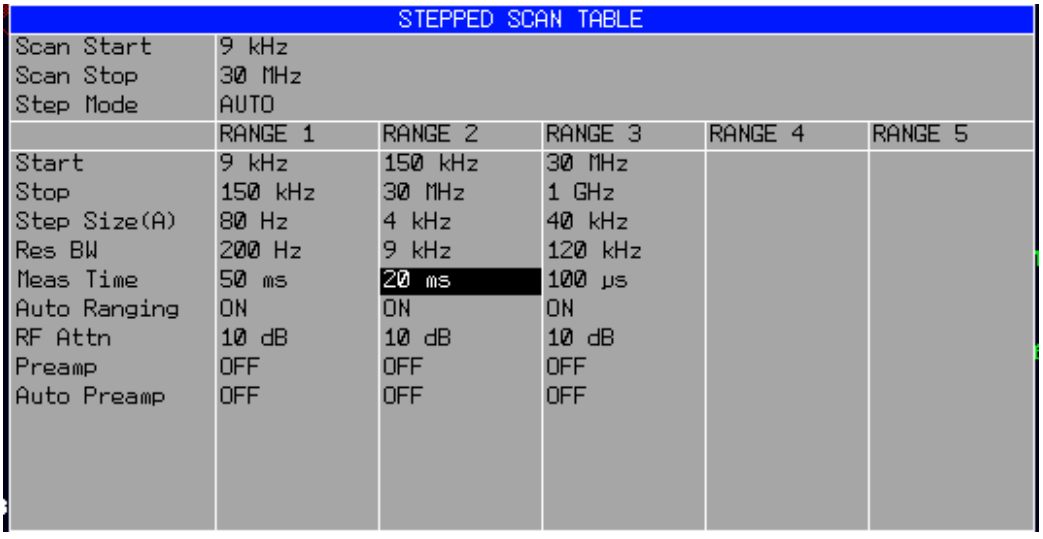
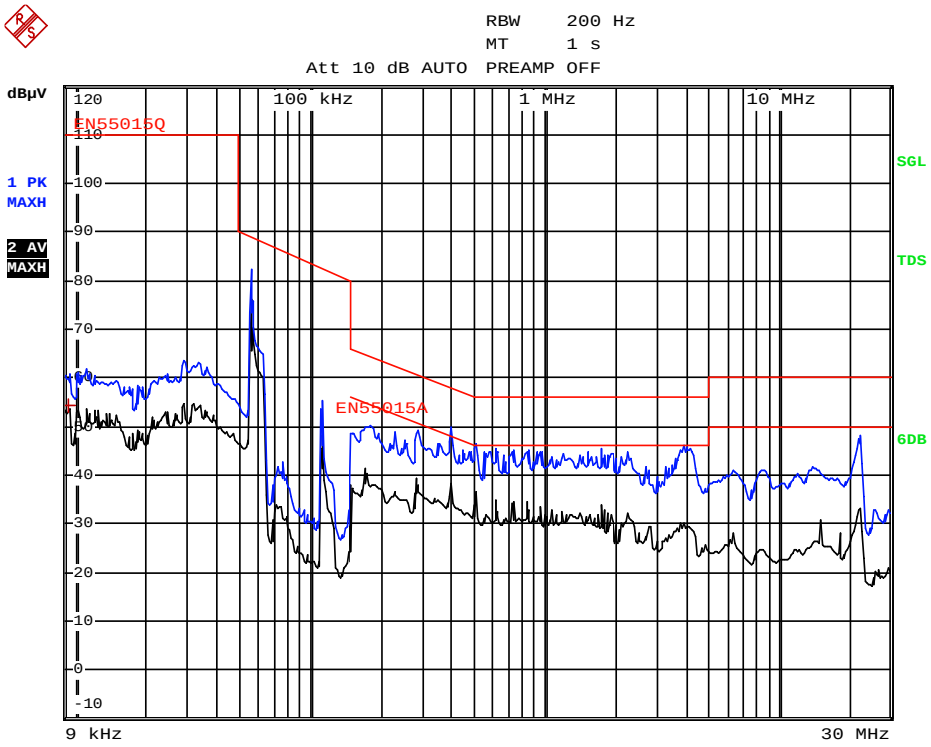


Figure 26—EMI Test Condition

Test Result: as Figure 27 shows, the result meets the standard EN55015, and the margin is enough.



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

	TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	9.24 kHz	56.59	-53.41
2	CISPR Average	9.48 kHz	51.50	
1	Quasi Peak	39.8 kHz	53.30	-56.69
2	CISPR Average	54.6 kHz	61.72	
1	Quasi Peak	250 kHz	43.85	-17.90
2	CISPR Average	298 kHz	35.04	-15.25
2	CISPR Average	566 kHz	31.93	-14.06
1	Quasi Peak	938 kHz	41.20	-14.79
2	CISPR Average	2.15 MHz	31.23	-14.76
1	Quasi Peak	2.182 MHz	37.73	-18.26
2	CISPR Average	8.858 MHz	25.45	-24.54
1	Quasi Peak	27.226 MHz	21.83	-38.16

Figure 27—Conducted EMI Performance at 220V AC Input

5.5. Steady State: V_{IN} =120V

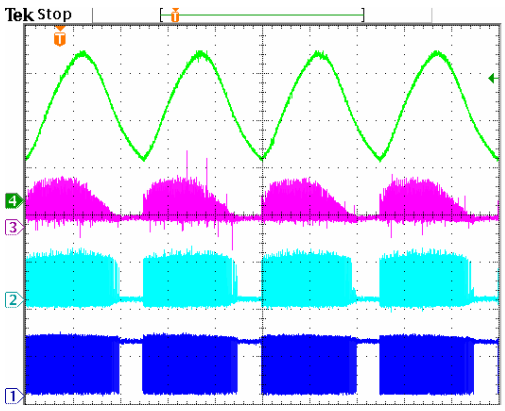


Figure 28—Max Dimming Phase

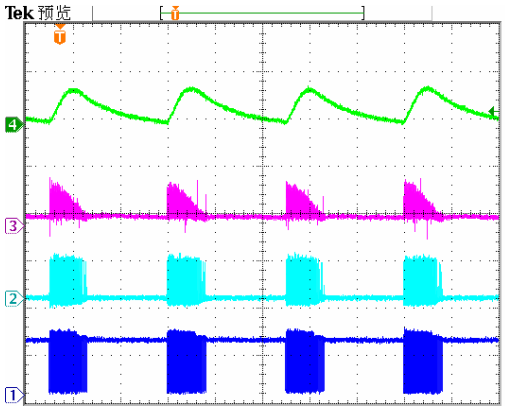


Figure 29—220 VAC, Full Load

Channel 4 : ILED, 200mA/div
Channel 3 : V_{CS}, 1V/div
Channel 2 : V_{ZCD}, 5V/div
Channel 1 : Gate, 10V/div, 4ms/div

5.6. Input Current and MULT Voltage: V_{IN}=120V

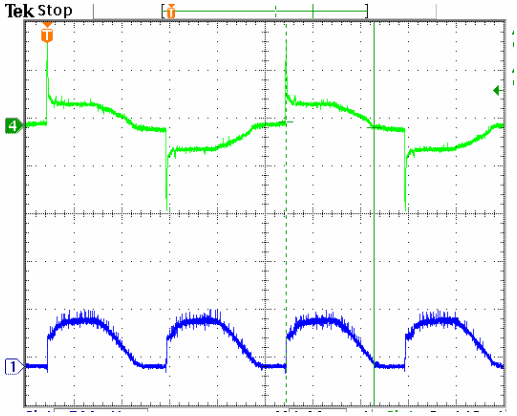


Figure 30—Max Dimming Phase

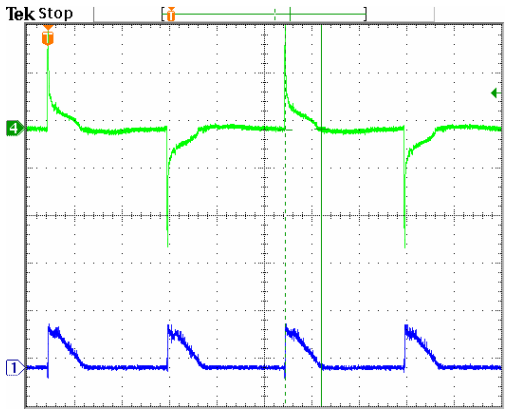


Figure 31—Min Dimming Phase

Channel 4 : ILED, 200mA/div
Channel 1 : VMULT, 500mV/div, 4ms/div

5.7. Start Up and Shut Down: V_{IN} =120V

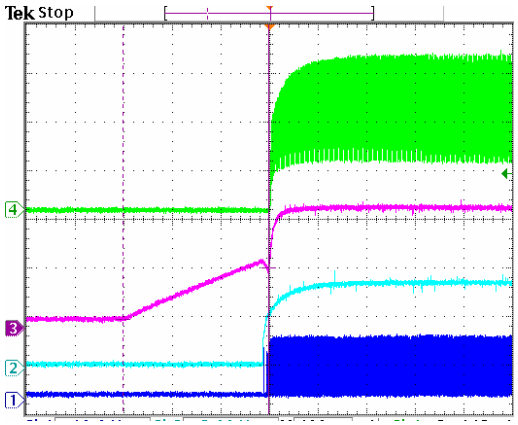


Figure 32—Start up, Full Load

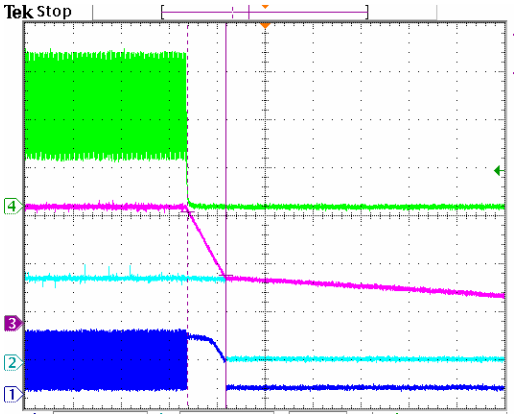


Figure 33—Shut Down, Full Load

Channel 4 : ILED, 200mA/div
Channel 3 : V_{CC}, 10V/div
Channel 2 : V_{COMP} 2V/div
Channel 1 : Gate, 10V/div, 4ms/div

5.8. OVP (open load at normal operation and OVP recovery): V_{IN} =120V

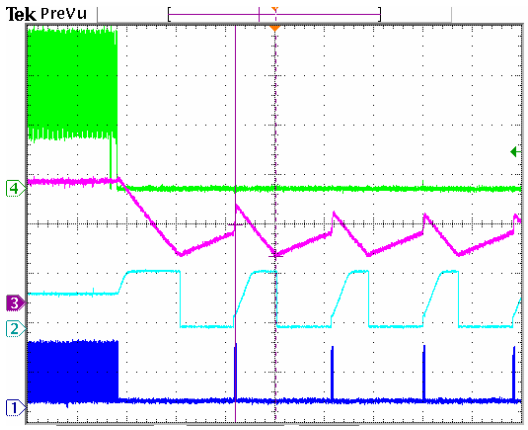


Figure 34—OVP at Normal Operation

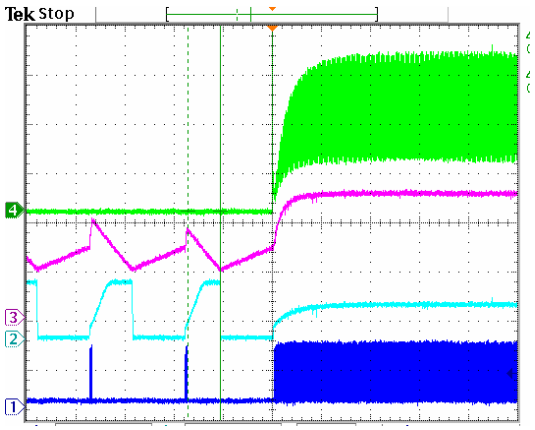


Figure 35—OVP Recovery

Channel 4 : ILED, 200mA/div
Channel 3 : V_{CC}, 10V/div
Channel 2 : V_{COMP}, 2V/div
Channel 1 : Gate, 10V/div, 4ms/div

5.9. SCP (Short LED+ to LED- at Normal Operation and SCP Recovery): V_{IN} =120V

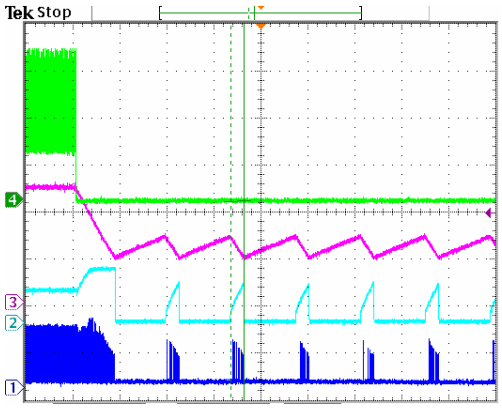


Figure 36—SCP at Normal Operation

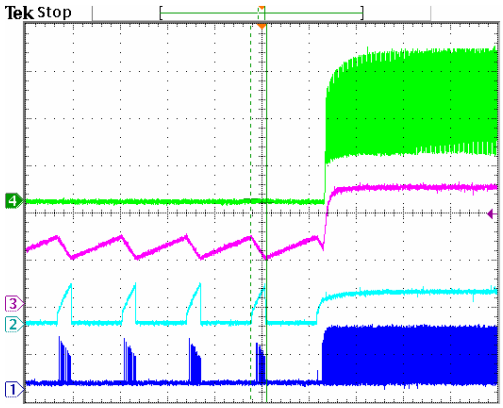


Figure 37—SCP Recovery

Channel 4 : ILED, 200mA/div
Channel 3 : V_{CC}, 10V/div
Channel 2 : V_{COMP}, 2V/div
Channel 1 : Gate, 10V/div, 4ms/div

5.10. TRIAC Dimmer Compatibility Test

This spec and board is compatible with the following dimmers and the list will be updated after more test.

Manufacturer	Part No.	Power Stage	Imax (mA)	Imin (mA)
LUTRON	6B38-DV-600P	600W	433	110
LUTRON	6B38-DVLV-600P	600W	434	126
LUTRON	6B38-DV-603PG	600W	384	116
LUTRON	6B38-S-600P	600W	435	107
LUTRON	6B38-S-603PG	600W	387	105
LUTRON	6B38-S-600	600W	456	109
LUTRON	6B38-SLV-600P	600W	439	118
LUTRON	6B38-GL-600-IV	600W	457	135
LUTRON	6B38-GL-600-WH	600W	455	109
LUTRON	NTLV-600-AL	600W	455	112
LUTRON	LG-600PH-AL	600W	439	114
LUTRON	AY-600P-AL	600W	437	136
LUTRON	DNG-603PH-WH	600W	425	28
LUTRON	TG-603GH-WH	600W	374	135
LUTRON	TG-600PH-WH	600W	433	137

Manufacturer	Part No.	Power Stage	Imax (mA)	Imin (mA)
LUTRON	CN-600P	600W	432	125
LUTRON	6B38-Q-600P	600W	438	147
LUTRON	TT300	300W	460	87
LEVITON	6633-P	600W	467	87
LEVITON	6633-P	600W	467	99
LEVITON	6633-P	600W	463	96
LEVITON	6631	600W	440	69
LEVITON	IG40O5	600W	441	39
LEVITON	TBI03	300W	470	25