Reference design – Xilinx ZU3EG Industrial Networking Solution (using PMIC)

Last update: 1/18/17
ZU3EG Industrial Networking Solution

- **0.85V @ 3A**
- **1.8V @ 500mA**
- **1.2V @ 50mA**
- **3.3V @ 200mA**
- **0.85V @ 300mA**

- **0.85V**
- **1.8V**
- **1.2V**

**Rail3:**
- VCCINT
- VCCBRAM
- VCCINT_IO

**Rail4:**
- VCCAUX
- VCCAUX_IO
- VCCADC

**Rail10:**
- VREFP

**Rail5:**
- VCC_PSPINTP
- VCC_PSPINTF
- VCC_PSPINTF_DDR

**Rail6:**
- VCC_PSAUX
- VCC_PSAUX_PLL
- VCC_PSAUX_PLL_PLL

**Rail7:**
- VCC_PSAUX
- VCC_PSAUX
- VCC_PSAUX

**Rail8:**
- VCC_PSPDPLL
- VCC_PSPDPLL

**Rail9:**
- NOR Flash
- Share w/ LPDDR4 VDDQ & VDDCA

**VDDQ DDR3**

Optional:
- 1.25V@ 1mA

Rail3, Rail4, and Rail10 are tagged with their voltage levels and currents. The diagram shows the various voltage rails and their respective currents. The NOR Flash rail is labeled as optional and is shared with LPDDR4 VDDQ and VDDCA. The ZU3EG Industrial Networking Solution is presented with a diagram highlighting the power distribution and voltage levels.
<table>
<thead>
<tr>
<th>Rail #</th>
<th>VIN (V)</th>
<th>Rail</th>
<th>VOUT (V)</th>
<th>Load (mA)</th>
<th>Seq</th>
<th>MPS part#</th>
<th>Footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>18-36</td>
<td>Intermediate rail</td>
<td>5 ± 5%</td>
<td>3000</td>
<td></td>
<td>MP9457</td>
<td>TSSOP-20 EP 6.6x6.6mm</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>VCCINT, VCCBRAM, VCCINT_IO</td>
<td>0.85 ± 3%</td>
<td>3000</td>
<td>1 / 3</td>
<td></td>
<td>Vout1 (4.5A)</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>VCCAUX, VCCAUX_IO, VCCADC, VCC_PSAUX, VCC_PSAUX, VCC_PSAUX, VCC_PSDDR_PLL</td>
<td>1.8 ± 3%</td>
<td>500</td>
<td>2 / 2</td>
<td></td>
<td>Vout2 (2.5A)</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>VPS_MGTRAVCC</td>
<td>0.85 ± 3%</td>
<td>300</td>
<td>3 / 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>VPS_MGTRAVTT</td>
<td>1.8 ± 3%</td>
<td>50</td>
<td>3 / 1</td>
<td></td>
<td>PMIC MP5416</td>
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<tr>
<td>7</td>
<td>5</td>
<td>VCCPSPLL</td>
<td>1.2 ± 3%</td>
<td>50</td>
<td>2 / 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>5</td>
<td>VCC_PSIO</td>
<td>3.3 ± 5%</td>
<td>200</td>
<td>3 / 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>5</td>
<td>VCCO_PSDDR</td>
<td>1.5 ± 3%</td>
<td>1000</td>
<td>3 / 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>5</td>
<td>VREF (optional)</td>
<td>1.25 ± 0.2%</td>
<td>1</td>
<td>3 / 1</td>
<td></td>
<td>MP8201 (0.002A)</td>
</tr>
</tbody>
</table>
MP5416
PMIC with 4xBucks and 5xLDOs

FEATURES:
- **High Efficiency Step-Down Converters**
  - 4.5A / 2.5A / 4A / 2A Bucks
  - 2.7V to 5.5V Operating Input Range
  - Adjustable Switching Frequency
  - Programmable Forced PWM/Auto PFM/PWM Mode
  - Hiccup Over Current Protection
- **Low Dropout Regulators**
  - One RTC Dedicated LDO
  - Four Low Noise LDOs
  - Two Separate Input Power Supplies
  - 100mV Dropout at 300mA Load
- **System**
  - I2C Bus and OTP
  - Power On/off Button
  - Power On Reset Output
  - Flexible Power On/off Sequence via OTP
  - Flexible DC/DC, LDO On/off via OTP

**Application Circuit**

**Efficiency vs. Load Current**

\( V_{IN} = 5V, \text{ Auto PFM/PWM Mode} \)

- **Buck1** = 1.2V
- **Buck2** = 1.5V
- **Buck3** = 1.8V
- **Buck4** = 3.3V

**Package: QFN28 - 4mm x 4mm**
Recommended Layout MP9457

Schematics (Typical)

Layout guidelines

Top Layer

Bottom Layer

Inner Layer 1

Inner Layer 2
MPS design highlights—(PMIC)

• MP9457
  – High Efficiency
  – Cost effective

• MP5416
  – High integration
    • 4x Bucks
    • 5x LDOs
  – Minimum External Components
  – I2C control
  – Built in sequencing
  – Factory set voltages
For additional information please contact
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at referencedesign@monolithicpower.com

For general information
http://www.monolithicpower.com