Kintex US+ FPGA PMIC Solution

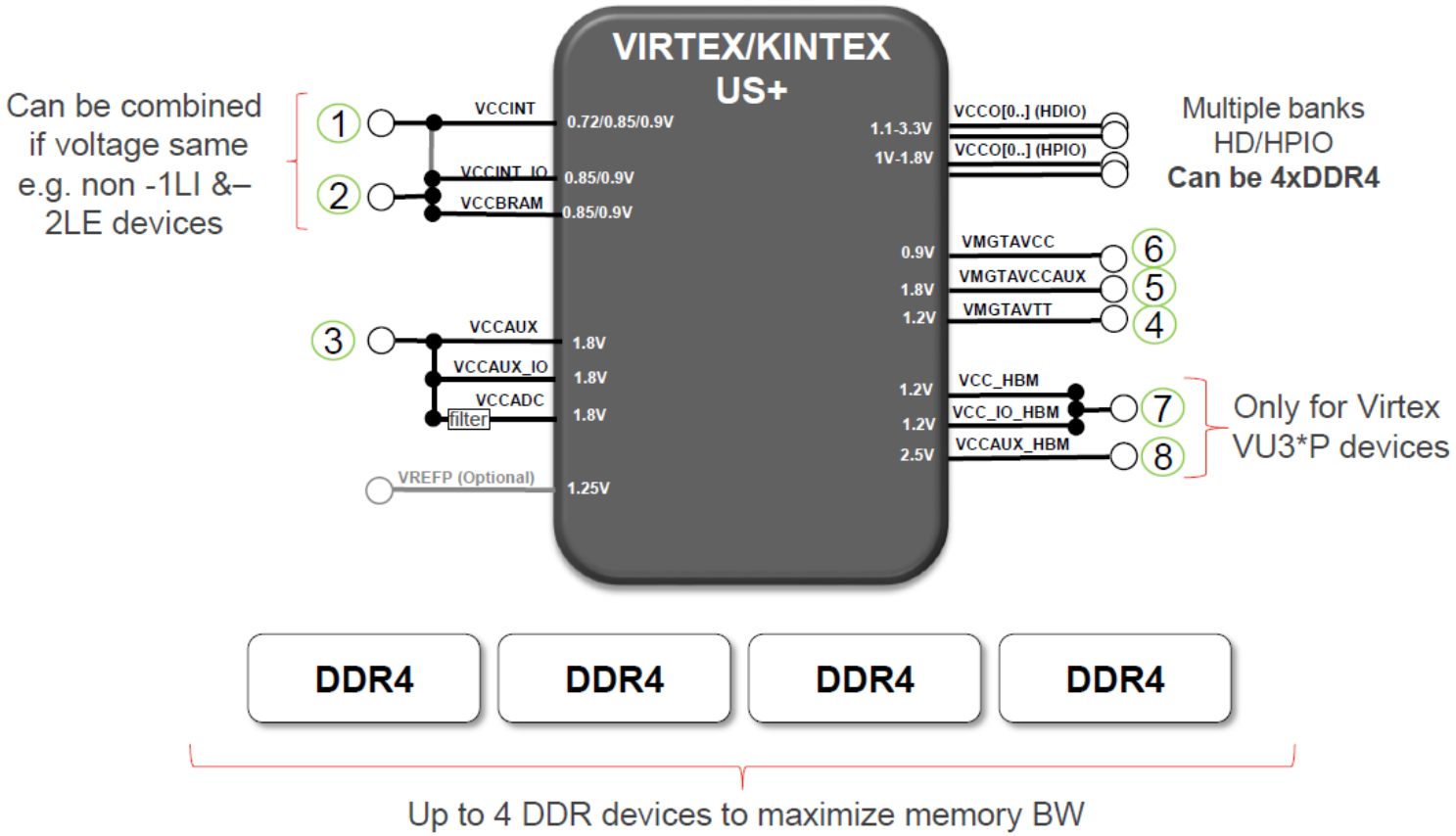
June 18, 2018

Simple, Easy Solutions™

rev 20170706

Power Rail Combination options

Rail Combination Options



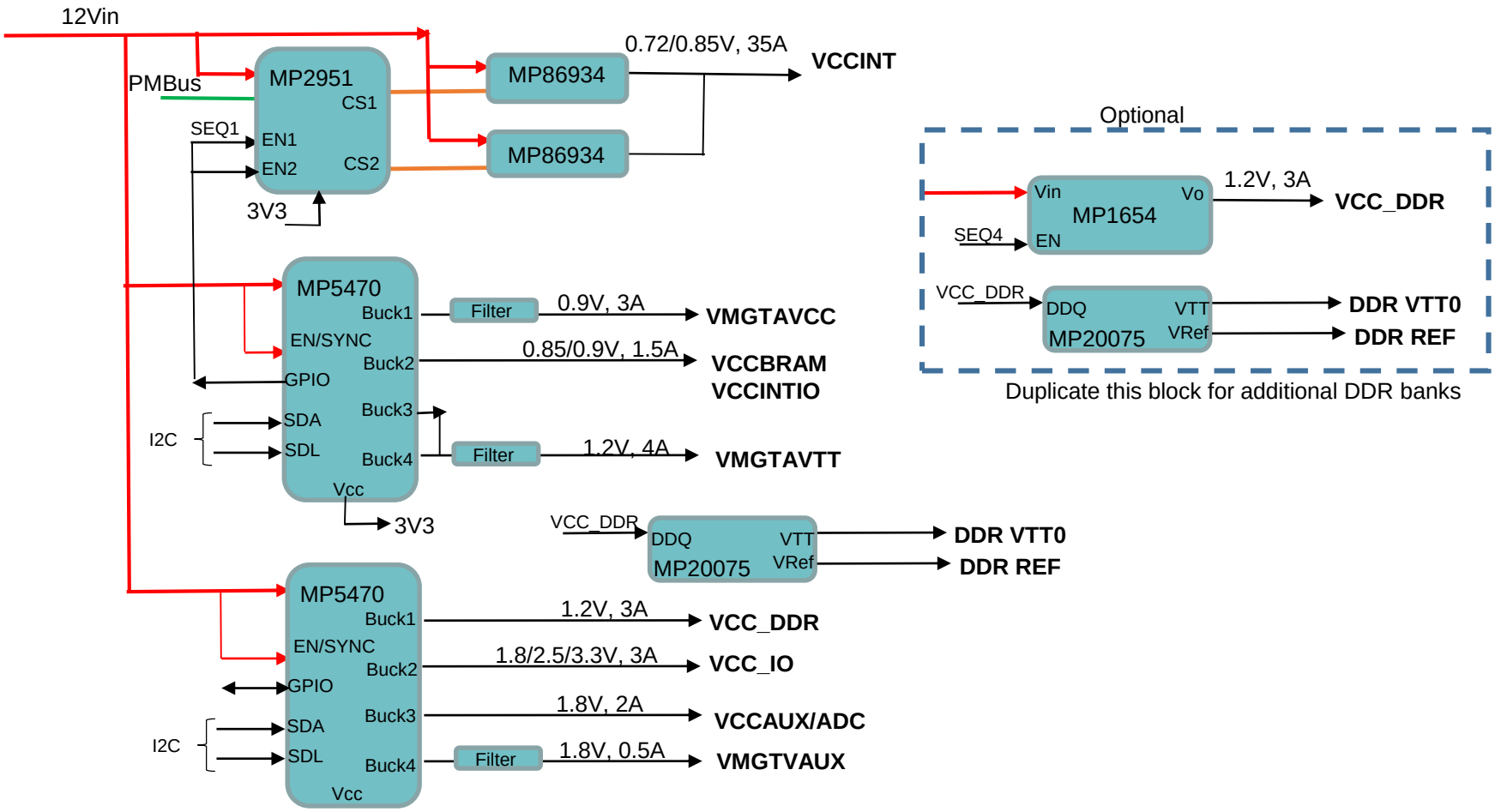
KintexUS+ Power Requirements

Vin=12V

Rail#	Rail	Voltage	Ripple (DC+AC)	Step Load	Comments	KIntexUS+
1	VCCINT	0.72/0.85/0.9V	±3%	25%	Assume up to 100A/us 25% load steps	10-35A
2	VCCBRAM/INT_IO	0.85/0.9V	±3%	40%	Normally tied to VCCINT, except for -L devices	0.8-2A
3	VCCAUX/ADC	1.8V ±3%	±3%	90%	Additional current may be needed for 1.8V IO	1-2A
4	VMGTAVTT	1.2V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	1-4A
5	VMGTVCCAUX	1.8V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	0-0.1A
6	VMGTAVCC	0.9V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	1-3A
7	VCC_HBM/IO	1.2V	±3%	80%	For VirtexUS+ only	N/A
8	VCCAUX_HBM	2.5V	±3%	80%	For VirtexUS+ only	N/A
9	VCC_IO	1.8/2.5/3.3V	±5%	90%	IO current varies widely depending on app	
10	VCC_DDR	1.2V		80%	Upto 4 Ext. DDR.	
11	DDR_VTT	VCC_DDR/2			Upto 4 Ext. DDR.	
12	DDR_VREF	VCC_DDR/2			Upto 4 Ext. DDR.	

Assume 10A/us for all rails except VCCINT

KintexUS+ Lowest Cost (PMIC)



MP5470 PMIC supports programmable power up/down sequencing

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Key Features KintexUS+ (PMIC)

VIN 12V +/-5%

Rail	VOUT	Ripple	Load	Step Load	Seq Up/Dwn	MPS Part#		pcb Area (mm2)	Efficiency @ 50% load
VCCINT	0.72/0.85/0.9V	+/-3%	10-35A	25%	1/4	MP2951 cntrl 2x MP86934		536	93.00%
VCCBRAM/VCCINTIO	0.85/0.9V	+/-3%	0.8-1.5A	40%	2/3	MP5470 PMIC1-buck2			85.52%
VCCAUX/ADC	1.8V	+/-3%	1-2A	90%	3/2	MP5470 PMIC2-buck3			88.69%
VMGTAVTT	1.2V	+/-3%	1-4A	25%	2/3	MP5470 PMIC1-buck3&4			82.93%
VMGTVCCAUX	1.8V	+/-3%	0.1A	25%	3/2	MP5470 PMIC2-buck4			78.00%
VMGTAVCC	0.9V	+/-3%	1-3A	25%	1/4	MP5470 PMIC1-buck1			80.96%
VCC_HBM/IO	N/A								
VCCAUX_HBM	N/A								
VCC_IO	1.8/2.5/3.3V	5%	3A	90%	4/1	MP5470 PMIC2-buck2			92.30%
VCC_DDR	1.2V	5%	3A	80%	4/1	MP5470 PMIC2-buck1		924	84.49%
DDR_VTT	VCC_DDR/2	5%	3A	80%	4/1				
DDR_REF						MP20075		19	
							sq mm	1479	
						Total	sq in	2.29	90.3%

Efficiency ~90.3%, size ~2.3sqin

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Overview – KintexUS+ Proposal

- 12Vin design (no intermediary regulator required)
- Design can be easily scaled/modified for customer requirements
- Common use of parts allow step and repeat for ease of design

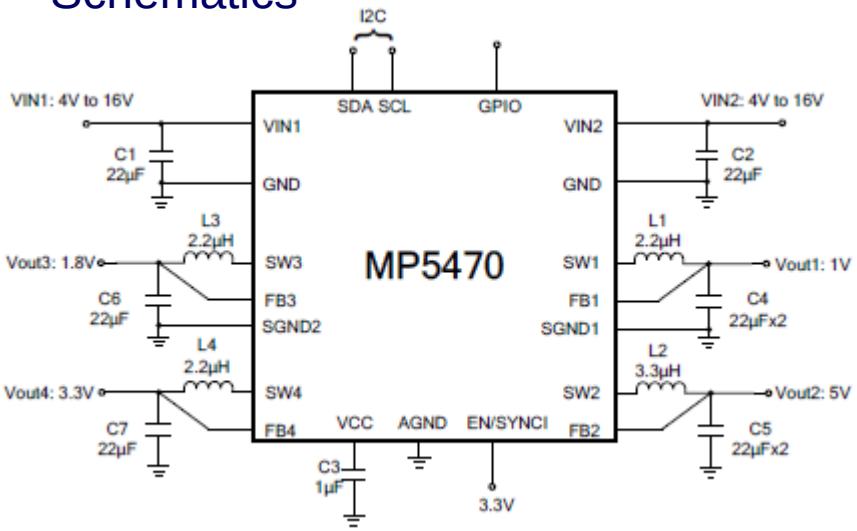
- Lowest cost
  - Discrete 2ph design (35A VCCINT) for high efficiency and fast transient response
  - Total system efficiency ~90.3%
  - Total solution size (~2.3 sqin) including input & output Caps
  - PMIC includes built in power up/down sequencing and requires minimum number of external components

Design details

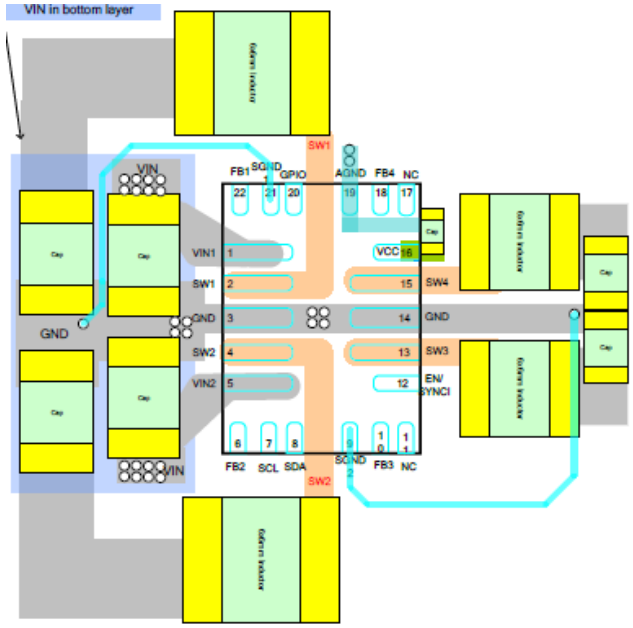
- Discrete solution
  - MP2888 + MP86945A (120A, 5phase discrete)
  - MP8733A/B (10A to 24A discrete)
  - MP5470 PMIC (3A/3A/2A/2A)
  - MP1476 (2A)
  - MP1654 (4A)
  - MP20075 (DDR TERM)

MP5470 PMIC

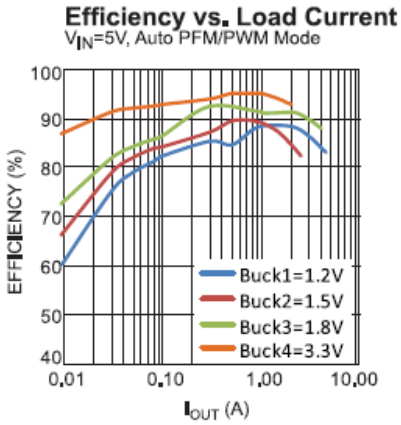
Schematics

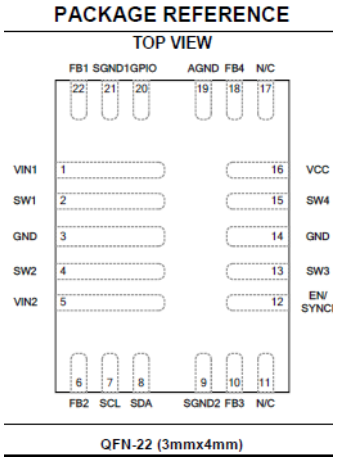


Layout guidelines



Solution size: 462mm2





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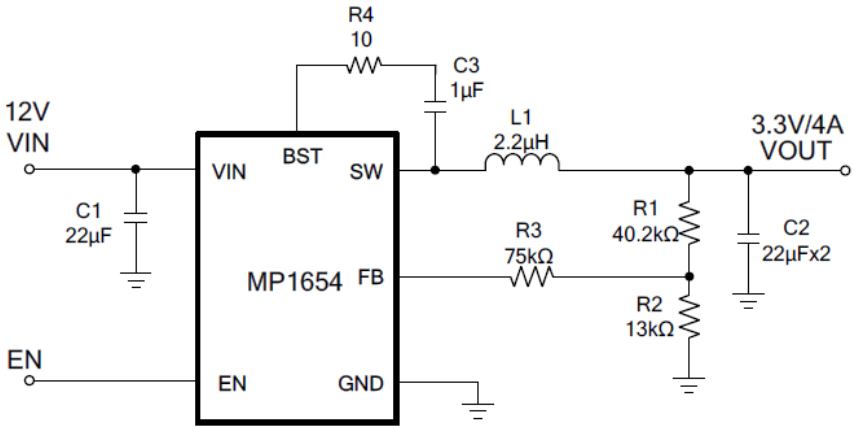
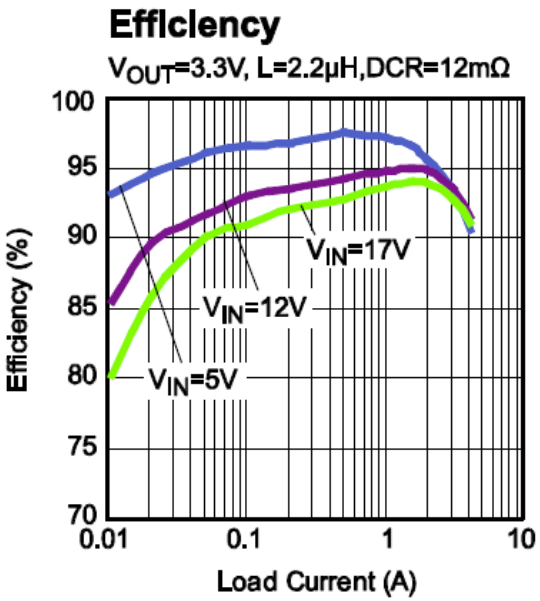
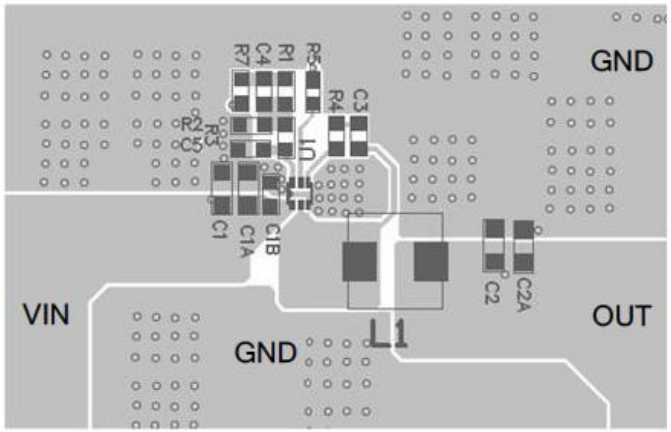
MP1654

Schematics

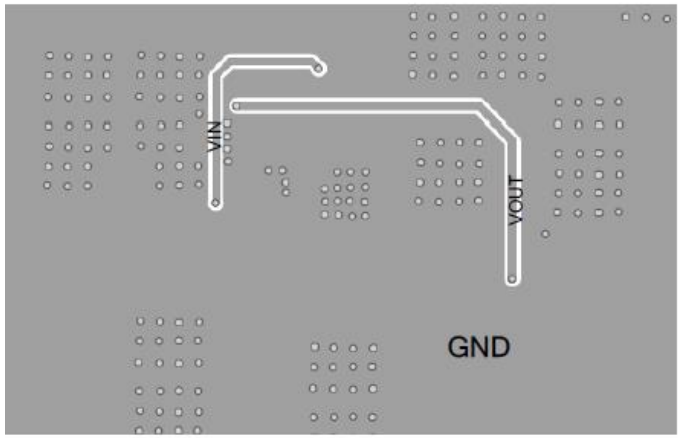




Layout guidelines



Top Layer



Bottom Layer

Solution footprint: 90mm2

External components: 9

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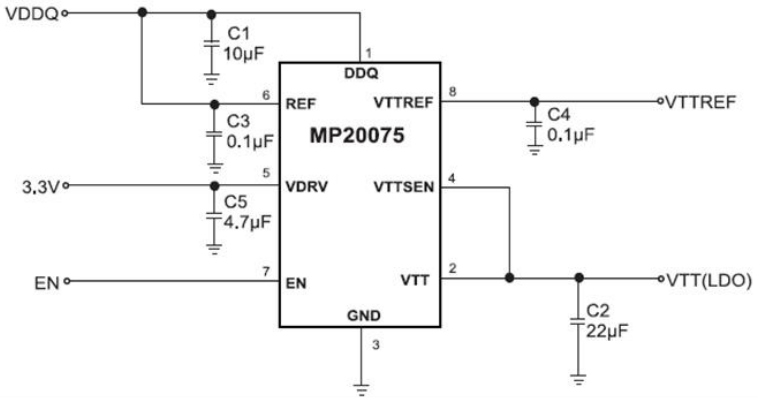
Schematics (Typical)



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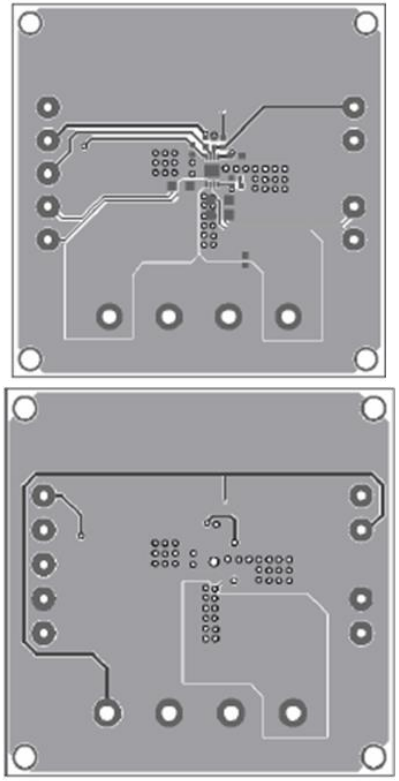

- For DDR4VTT
- Solution footprint: 19mm^2
- External Components:5

Caps included in area calculations:

Output Caps 1x 22uF 0805, 1x 0603 on PCB bottom

Input Caps: 3x 0603 on PCB bottom

MPS Support

MPS support for Xilinx customers

- Engineering support for design reviews, bring up and debug
- Our FAEs can assist with optimizing reference designs for customer's exact requirements
- MPS already working with leading SoC vendors and have support teams already in place for reference designs
- Power FAEs located in all major territories for world wide support

Simulation tools:

- Models available for predicting Efficiency, Power loss, Load step response, Phase margin and other key requirements.

Evaluation

- EVBs available
- MPS can provide free samples for evaluation and prototyping

MPS contact Thomas.fenn@monolithicpower.com

MPS Reference Design Team at referencedesign@monolithicpower.com

For general information
http://www.monolithicpower.com

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