



Zynq UltraScale+ RFSoc Power Delivery

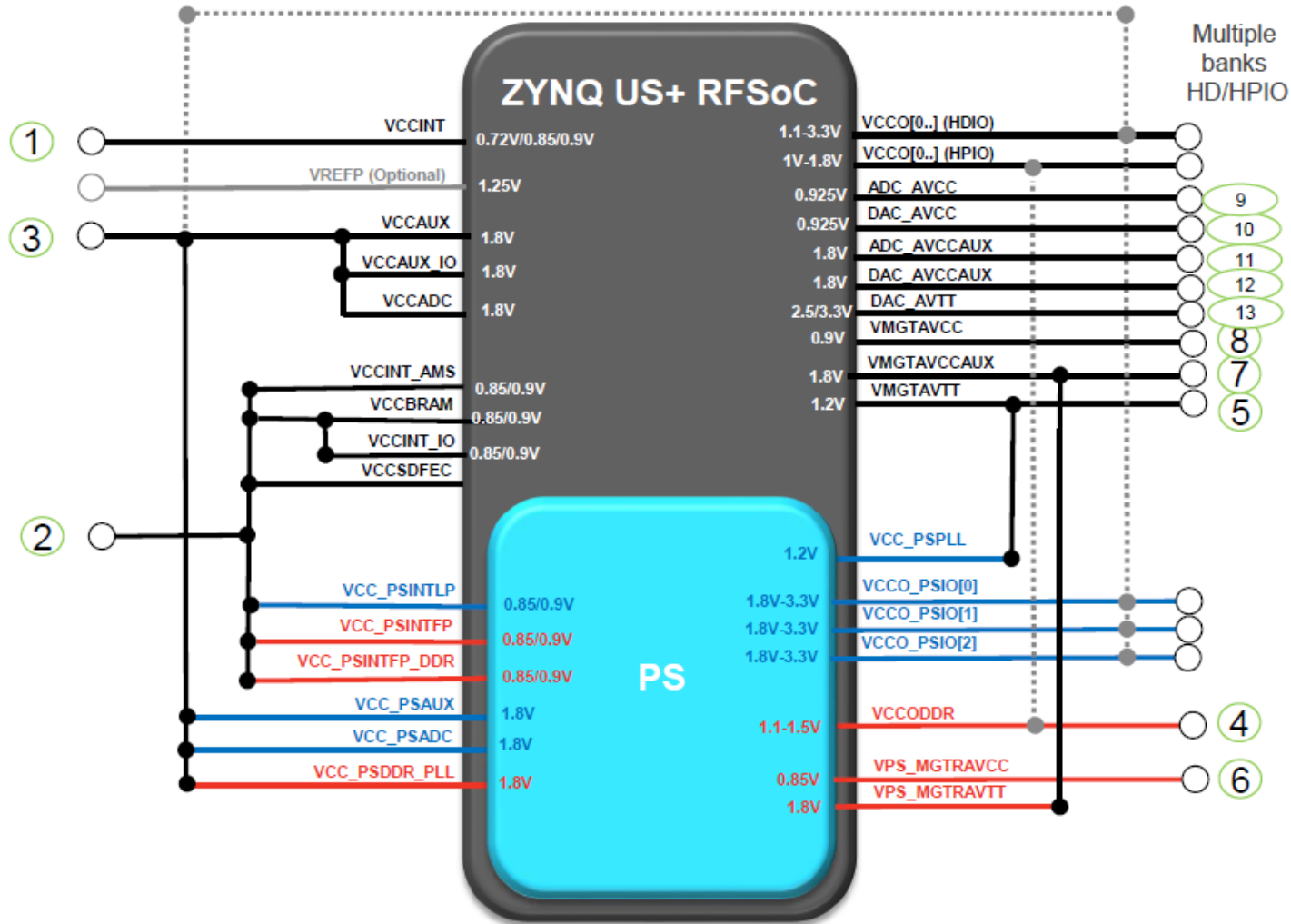
April 4, 2018

Zynq UltraScale+ RFSoc Power Rails

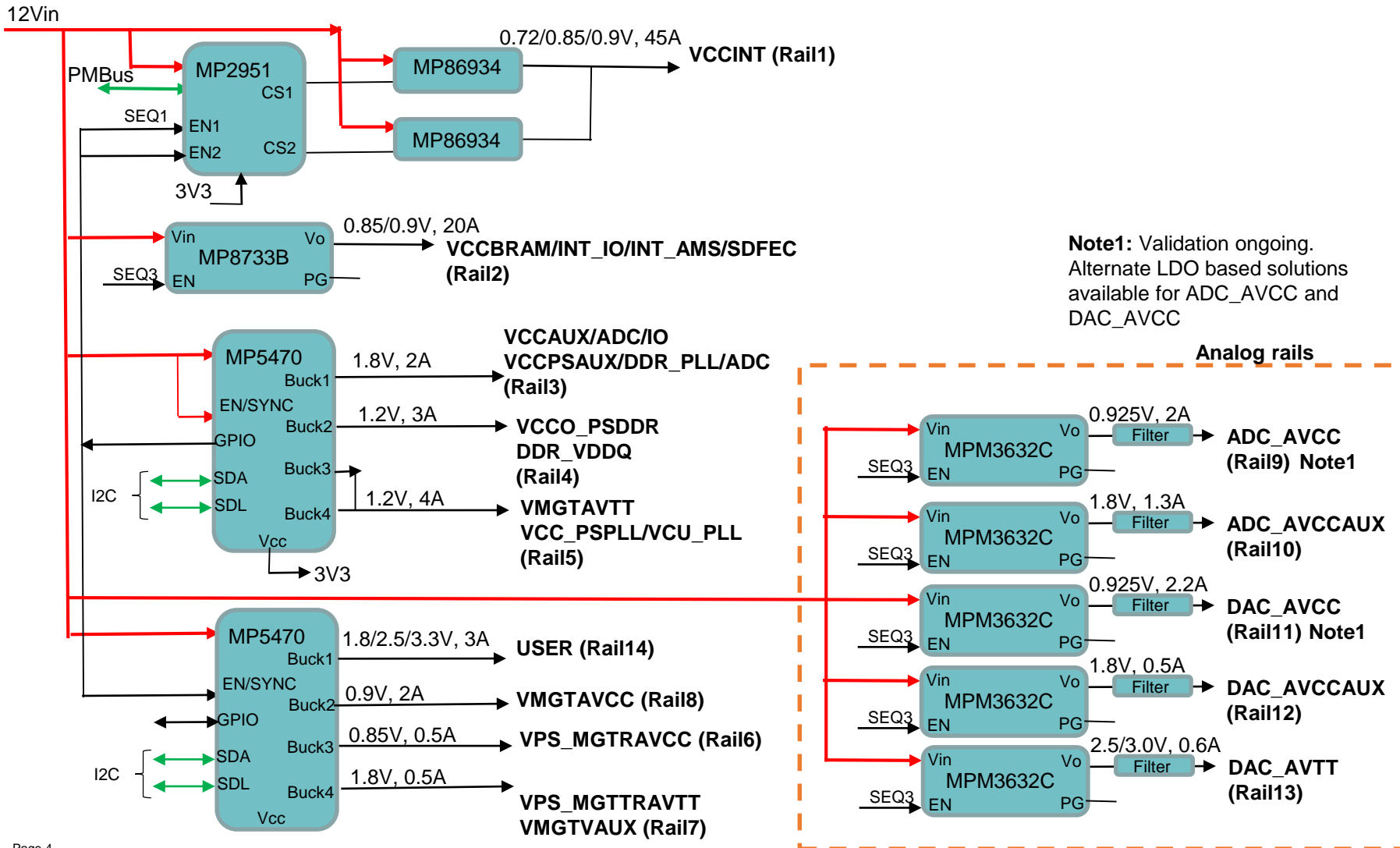
Vin=12V

Rail#	Rail	Voltage	Ripple (DC+AC)	Load	Step Load	Comments
1	VCCINT	0.72/0.85/ 0.9V	±3%	30-45A	25%	Assume up to 100A/us 25% load steps
2	VCCBRAM/INT_IO /INT_AMS/SDFEC	0.85/0.9V	±3%	10-20A	40-70%	Assume 40% for ZU25/27/29DR Assume 70% for ZU21/28DR
3	VCCAUX/ADC/IO VCC_PSAUX/DDR_PLL/ADC	1.8V	±3%	1.6-2A	90%	Additional current may be needed for 1.8V IO
4	VCCO_PSDDR DDR_VDDQ	1.1-1.5V	DDR	DDR	DDR	Powervendor use their expertise to for this rail
5	VMGTAVTT VCC_PSPLL/VCU_PLL	1.2V	±3%	2-4A	25%	10mV pk-pk ripple at FPGA pins. See UG578
6	VPS_MGTRAVCC	0.85V	±3%	0.3A	50%	10mV pk-pk ripple at FPGA pins. See UG578
7	VPS_MGTRAVTT VMGTVCCAUX	1.8V	±3%	0.1-0.5A	25%	10mV pk-pk ripple at FPGA pins. See UG578
8	VMGTAVCC	0.9V	±3%	1-2A	25%	10mV pk-pk ripple at FPGA pins. See UG578
9	ADC_AVCC	0.925V	±3%	1.7-2A	20%	50uV rms 0.1-100kHz, 0.25mV pk-pk ripple 0.1-15MHz
10	ADC_AVCCAUX	1.8V	±3%	1.2-1.3A	20%	10mV pk-pk 0.1-15MHz
11	DAC_AVCC	0.925V	±3%	1.1-2.2A	20%	50uV rms 0.1-100kHz, 0.4mV pk-pk ripple 0.1-15MHz
12	DAC_AVCCAUX	1.8V	±3%	0.25-0.5A	20%	2mV pk-pk ripple 0.1-15MHz
13	DAC_AVTT	2.5 or 3.0V	±3%	0.3-0.6A	20%	8mV pk-pk ripple 0.1-15MHz
14	VCCO	User	±5%			

Zynq UltraScale+ RFSoc Power Rail Consolidation



Zynq UltraScale+ RFSoc – PMIC solution



Note1: Validation ongoing. Alternate LDO based solutions available for ADC_AVCC and DAC_AVCC

Analog rails

MP5470 PMIC supports programmable power up/down sequencing



Key Features Zynq UltraScale+ RFSoc (using PMIC)

VIN 12V +/-5%									
Rail#	Rail	VOUT	Ripple	Load	Step Load	Seq Up/Dwn	MPS Part#	pcb Area (mm2)	Efficiency @ 50% load
	VCCINT	0.72/0.85/0.9V	+/-3%	30-45A	25%	1/4	MP2951 cntrl 2x MP86934	536	93.00%
2	VCCBRAM/INT_IO /INT_AMS/SDFEC	0.85/0.9V	+/-3%	10-20A	40-70%	3/2	MP8733B	216	89.00%
3	VCCAUX/ADC/IO VCC_PSAUX/DDR_PLL/ADC	1.8V	+/-3%	1.6-2A	90%	1/4	MP5470 PMIC1-buck1	462	88.69%
4	VCCO_PSDDR DDR_VDDQ	1.1-1.5V	+/-3%	3A	25%	4/1	MP5470 PMIC1-buck2		84.49%
5	VMGTAVTT VCC_PSPLL/VCU_PLL	1.2V	+/-3%	2-4A	25%	2/3	MP5470 PMIC1-buck3&4		82.93%
6	VPS_MGTRAVCC	0.85V	+/-3%	0.5A	50%	2/3	MP5470 PMIC2-buck3	462	82.50%
7	VPS_MGTRAVTT VMGTVCCAUX	1.8V	+/-3%	0.1-0.5A	25%	2/3	MP5470 PMIC2-buck4		80.96%
8	VMGTAVCC	0.9V	±3%	1-2A	25%	2/3	MP5470 PMIC2-buck2		86.00%
14	VCCO	User (1.8/2.5/3.3V)	±5%	3A max	25%	4/1	MP5470 PMIC2-buck1		92.00%
9	ADC_AVCC	0.925V	±3%	1.7-2A	20%	3/2	MPM3632C	55	80.00%
10	ADC_AVCCAUX	1.8V	±3%	1.2-1.3A	20%	3/2	MPM3632C	55	85.00%
11	DAC_AVCC	0.925V	±3%	1.1-2.2A	20%	3/2	MPM3632C	55	80.00%
12	DAC_AVCCAUX	1.8V	±3%	0.25-0.5A	20%	3/2	MPM3632C	55	82.00%
13	DAC_AVTT	2.5 or 3.0V	±3%	0.3-0.6A	20%	3/2	MPM3632C	55	88.00%
								sq mm	1951
								Total sq in	3.02
									90%



Efficiency 90%, size 3.0sqin

Overview – Zynq UltraScale+ RFSoc Proposals

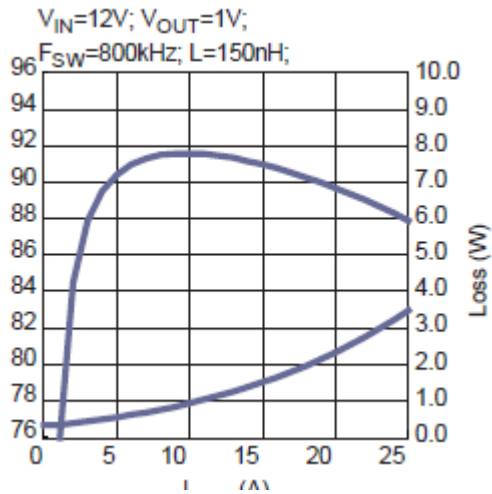
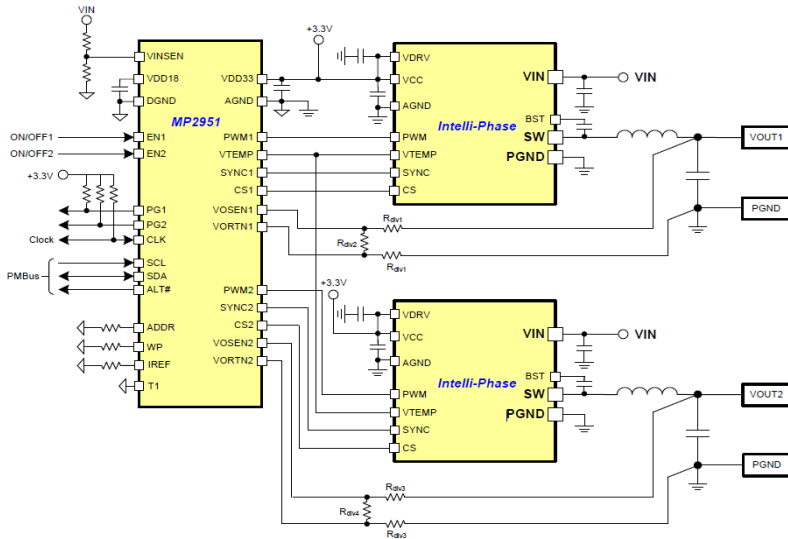
- 12Vin design (no intermediary regulator required)
- Design can be easily scaled/modified for customer requirements
- Common use of parts allow step and repeat for ease of design

- Low cost, High Efficiency
 - Discrete 2ph design (45A VCCINT) for high efficiency and fast transient response
 - Total system efficiency ~90%
 - Total solution size ~3.0 sqin including input & output Caps
 - PMIC includes built in power up/down sequencing and requires minimum number of external components

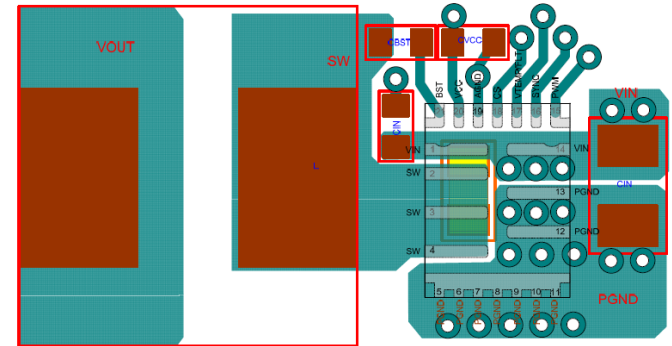
- PMIC based solution
 - MP2951 + MP86934 (45A, 2phase discrete)
 - MP8733B (20A discrete)
 - MP5470 PMIC (3A/3A/2A/2A)
 - MPM3732C (3A module)

MP2951 + MP86934 (VCCINT) 45A

Schematics



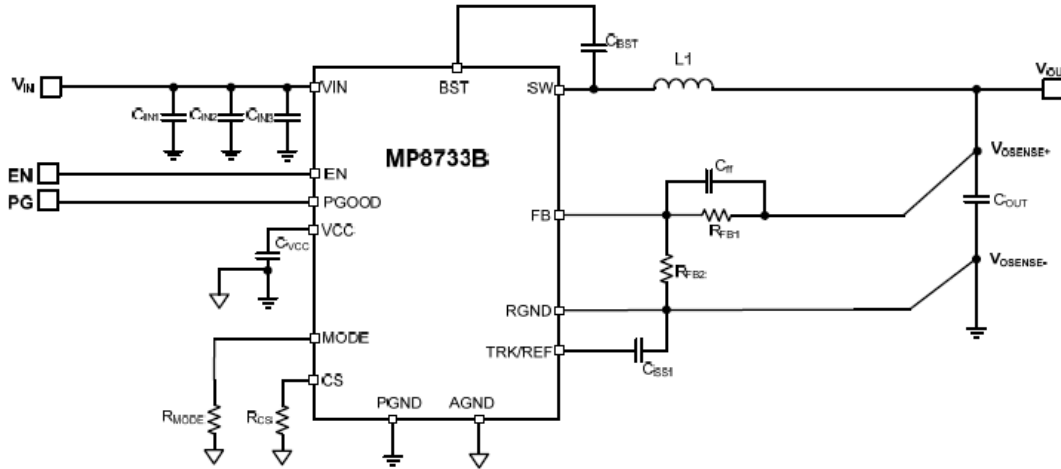
Layout guidelines



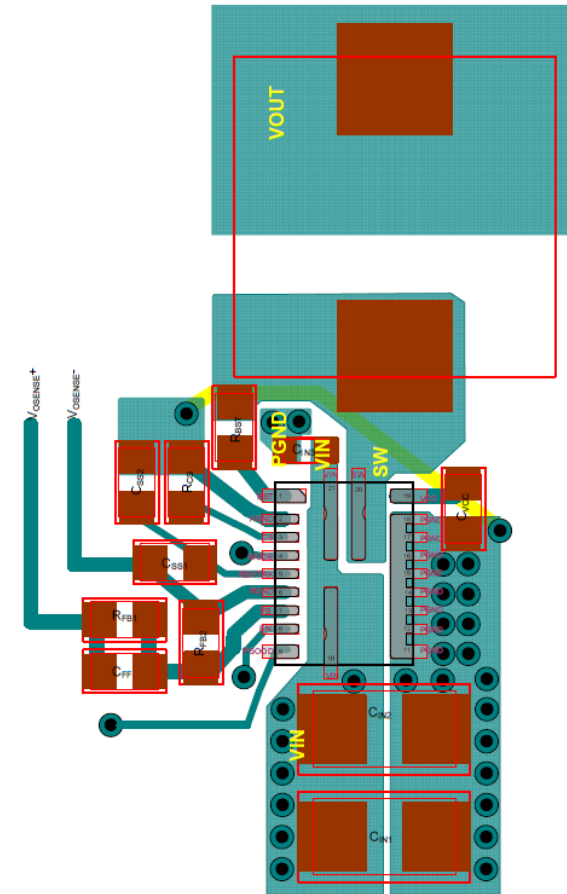
Solution size: 536mm²
 Controller: 110mm²
 Power Stages (2x153) = 306mm²
 Caps = 120mm²

MP8733A/B

Schematics

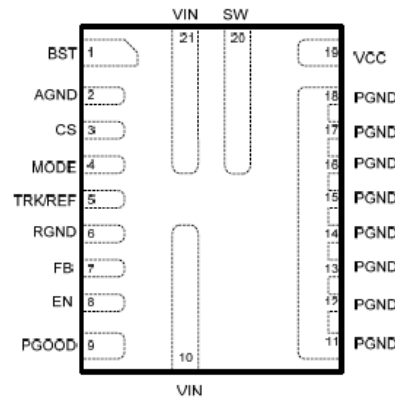
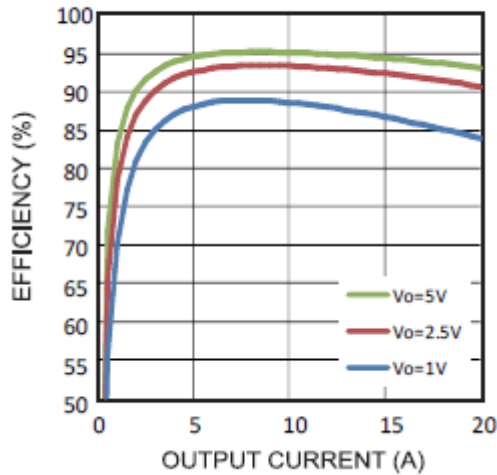


Layout guidelines



Efficiency

Forced CCM, 0.4uH, 800kHz

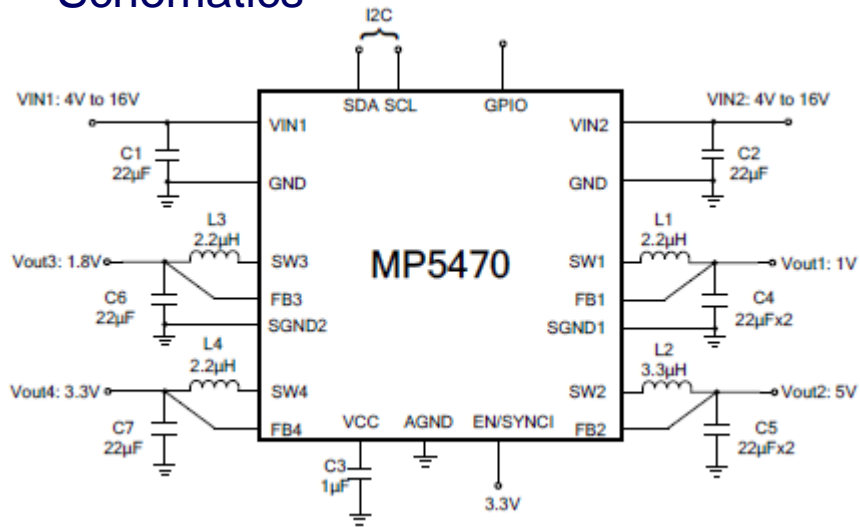


QFN-21 (3mmx4mm)

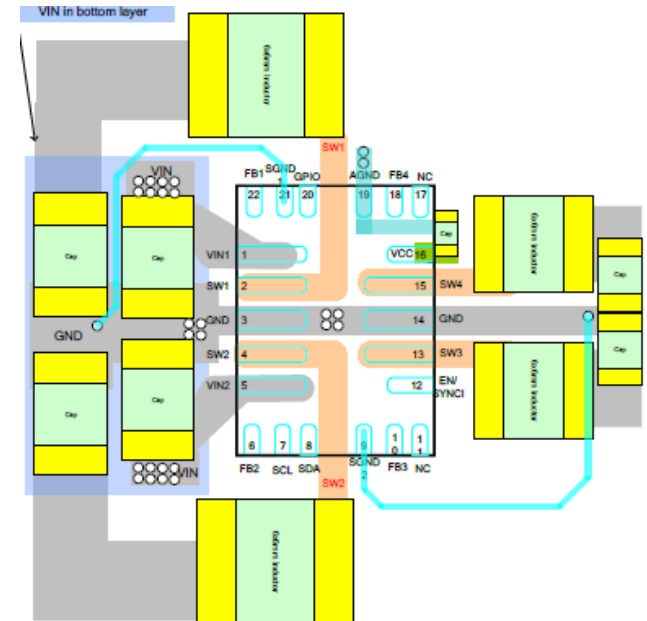
Solution size: 216mm²

MP5470 PMIC

Schematics

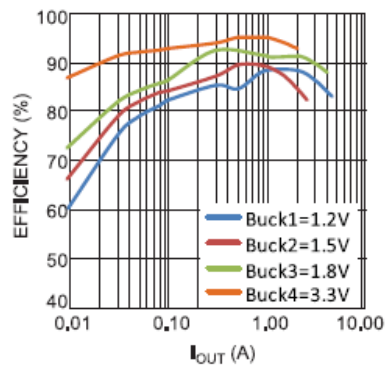


Layout guidelines



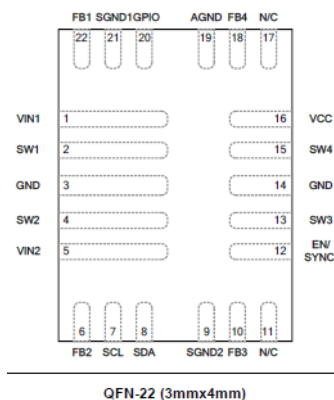
Solution size: 462mm²

Efficiency vs. Load Current
VIN=5V, Auto PFM/PWM Mode



PACKAGE REFERENCE

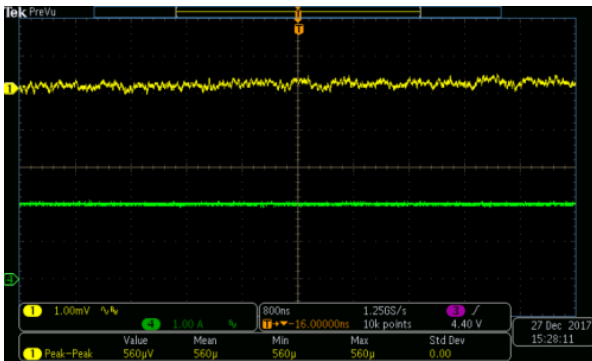
TOP VIEW



Analog rails – Expected ripple performance based on MPM3833C (EVREF102-A)

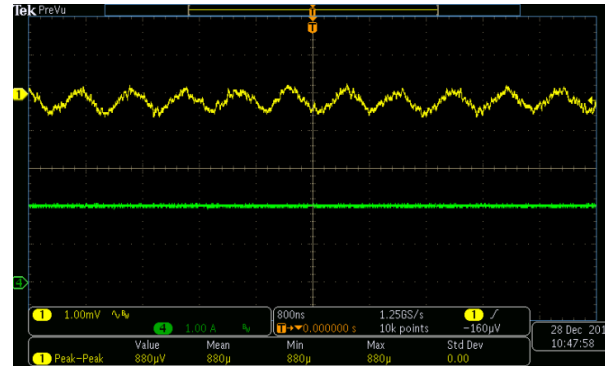
ADC_AVCC

$V_o=0.925V, I_o=2A$
 $V_{o,P-P}=0.56mV$



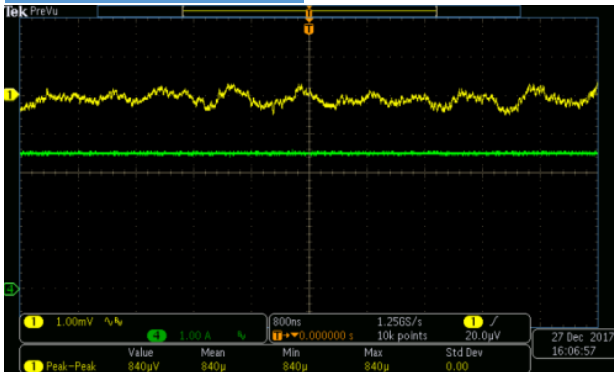
ADC_AVCCAUX

$V_o=1.8V, I_o=2A$
 $V_{o,P-P}=0.88mV$



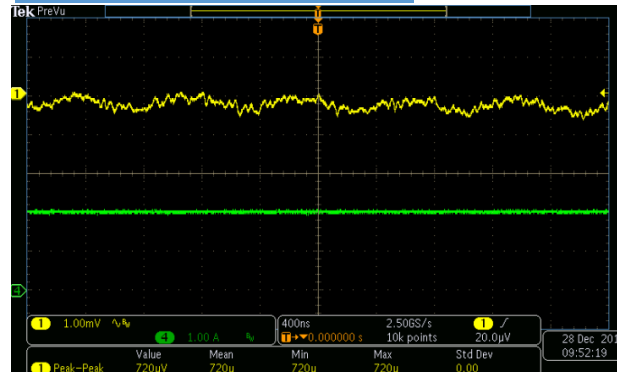
DAC_AVCC

$V_o=0.925V, I_o=3.5A$
 $V_{o,P-P}=0.84mV$



DAC_AVCCAUX

$V_o=1.8V, I_o=2A$
 $V_{o,P-P}=0.72mV$



MPS support for Xilinx customers

- Engineering support for design reviews, bring up and debug
- Our FAEs can assist with optimizing reference designs for customer's exact requirements
- MPS already working with leading SoC vendors and have support teams already in place for reference designs
- Power FAEs located in all major territories for world wide support

Simulation tools:

- Models available for predicting Efficiency, Power loss, Load step response, Phase margin and other key requirements.

Evaluation

- EVBs available
- MPS can provide free samples for evaluation and prototyping

MPS contact Thomas.fenn@monolithicpower.com

MPS Reference Design Team at referencedesign@monolithicpower.com

For general information

<http://www.monolithicpower.com>